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AN6068

Replacing 4-Mbit (256K x 16) MRAM with Cypress nvSRAM

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Associated Part Family: CY14x104NA

Related Application Notes: AN43593

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AN6068 discusses the key pinout differences between the Everspin 4-Mbit (256K x 16) MRAM and the Cypress 4-Mbit (256K x 16) nvSRAM devices. These differences should be taken into consideration when designing a PCB to use either MRAM or the high performance nvSRAM on the same footprint as true alternate source part number on the same bill of materials (BOM).

1 Introduction

Cypress offers the highest performance and most reliable nonvolatile RAM products available with its nvSRAM product line. The nvSRAM technology combines the performance characteristics of a high-speed SRAM with that of a nonvolatile memory. A similar nonvolatile solution is the Magnetoresistive RAM (MRAM) from Everspin in which magnetic polarization is used to store information. This application note discusses designing applications hardware with the option to use either MRAM or nvSRAM on the same socket without any hardware redesign.

The nvSRAM requires a storage capacitor (V_{CAP}) to execute AutoStore. The V_{CAP} pin on the nvSRAM package corresponds to either a DC (Do Not Connect) or a NC (No Connect) pin on the MRAM part depending upon package type. The MRAM recommends that NC or DC pins can be left either floating or tied to V_{SS}. Therefore, thestorage capacitor for nvSRAM can remain connected when nvSRAM or MRAM are interchangeably used.

The nvSRAM alsohas a $\overline{HSB}$ pin to monitor the device status or to initiate a hardware store. The $\overline{HSB}$ pin on the nvSRAM package corresponds to a NC (No Connect) pin onthe MRAM package. This allows using MRAM and nvSRAM interchangeably on the same footprint. In this case the NC pin corresponding to $\overline{HSB}$ can be either left floating or can be connected to the V_{CC}.

Additional on-demand nonvolatile features of nvSRAM such as hardware initiated STORE through a hardware pin ($\overline{HSB}$) or software initiated STORE and RECALL through soft sequences and so on, are specific to the nvSRAM device and need not be considered while migrating from MRAM to nvSRAM. However, an application can integrate these additional features of nvSRAM to enhance their application performance and flexibility. Refer to the Cypress nvSRAM datasheets for using additional nvSRAM features in your applications.

2 Replacing MRAM with Cypress nvSRAM

This section highlights pin and package differences between the Cypress nvSRAM and the MRAM devices for 4-Mbit (256K x 16) in 44-pin TSOP-II (Thin Small Outline Package - Type II) and 48-ball FBGA (Fine Pitch Ball Grid Array) package options respectively. This section also discusses about necessary design considerations which will enable you to create a common PCB footprint for using either nvSRAM or MRAM on the same footprint.

2.1 Replacing 44 TSOP-II Package Option

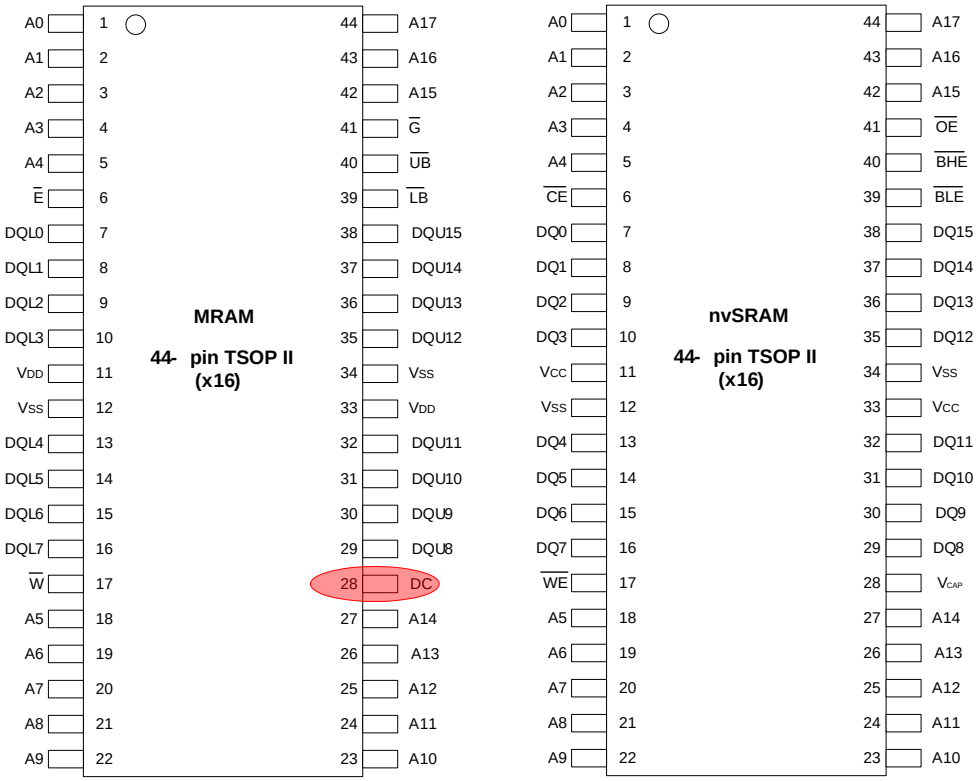
Figure 1 shows an example of replacing 4-Mbit (x16) MRAM by the 4-Mbit (x16) nvSRAM in a 44-pin TSOP-II package option on the same 44 pad PCB footprint. The dimensions of the 44-pin TSOP-II package of MRAM and nvSRAM devices are identical and shown in Table 1.

Table 1. 44-pin TSOP II Package Comparison

Package Dimensions (in mm)	MRAM	nvSRAM
Length	18.4	18.4
Width	10.16	10.16
Height	1.2	1.2
Pitch	0.8	0.8

The nvSRAM 44-pin TSOP-II pinout is similar to that of the MRAM 44-pin TSOP-II pinout except for the pin 28, which is designated as a DC (Do Not Connect) pin on the MRAM, whereas it is the V_{CAP} pin on the nvSRAM. By creating a footprint option for connecting an appropriate capacitor for nvSRAM V_{CAP}, the MRAM can be easily replaced by the nvSRAM, or the nvSRAM replaced by the MRAM, without any modification to the board. Refer to Figure 3 for the nvSRAM V_{CAP} connection.

Figure 1. MRAM and nvSRAM 44-pin TSOP II Package Comparison



2.2 Replacing 48-ball FBGA Package Option

Figure 2 shows an example of replacing 4-Mbit (x16) MRAM by a 4-Mbit (x16) nvSRAM in a 48-ball FBGA package option on the same 48 pad PCB footprint. The dimensions of 48-ball FBGA package of MRAM and nvSRAM devices differ in their length, width, and height. However the pitch of the 48-ball FBGA package remains identical which makes it possible to create a drop in replacement footprint for both package options. In this case, the package keep-out area on the PCB should be maintained such that either nvSRAM or MRAM 48-ball FBGA package can be mounted easily without obstructing other components on the PCB. The comparison of 48-ball FBGA package dimension for MRAM and nvSRAM are shown in Table 2.

Table 2. 48-ball FBGA Package Comparison

Package Dimensions (in mm)	MRAM	nvSRAM
Length	8	10
Width	8	6
Height	1.35	1.2
Pitch	0.75	0.75

The nvSRAM pinout is similar to that of the MRAM except for the three balls E3, G2, and H6 which are either designated as a DC (Do Not Connect) or NC (No Connect) pin for the MRAM. Whereas E3, G2, and H6 are the V_{CAP}, ($\overline{HSB}$), and NC pin for the nvSRAM respectively. By creating a footprint option for connecting an appropriate capacitor for nvSRAM V_{CAP}, the MRAM can be easily replaced by the nvSRAM, or the nvSRAM replaced by the MRAM, without any modification to the board. The nvSRAM $\overline{HSB}$ pin is pulled to HIGH internally by a weak pull up resistor (~100 KΩ). Therefore, if the nvSRAM ($\overline{HSB}$) pin functionality is not used in the design, the ($\overline{HSB}$) pin can be left as floating (NC). There is no restriction for nvSRAM NC pin connection. The nvSRAM NC pin can be biased to any logic level (HIGH or LOW) or can be left as floating (NC) in the design. Refer to Figure 3 for the nvSRAM VCAP and ($\overline{HSB}$) connection.

Figure 2. MRAM and nvSRAM 48-ball FBGA Package Comparison

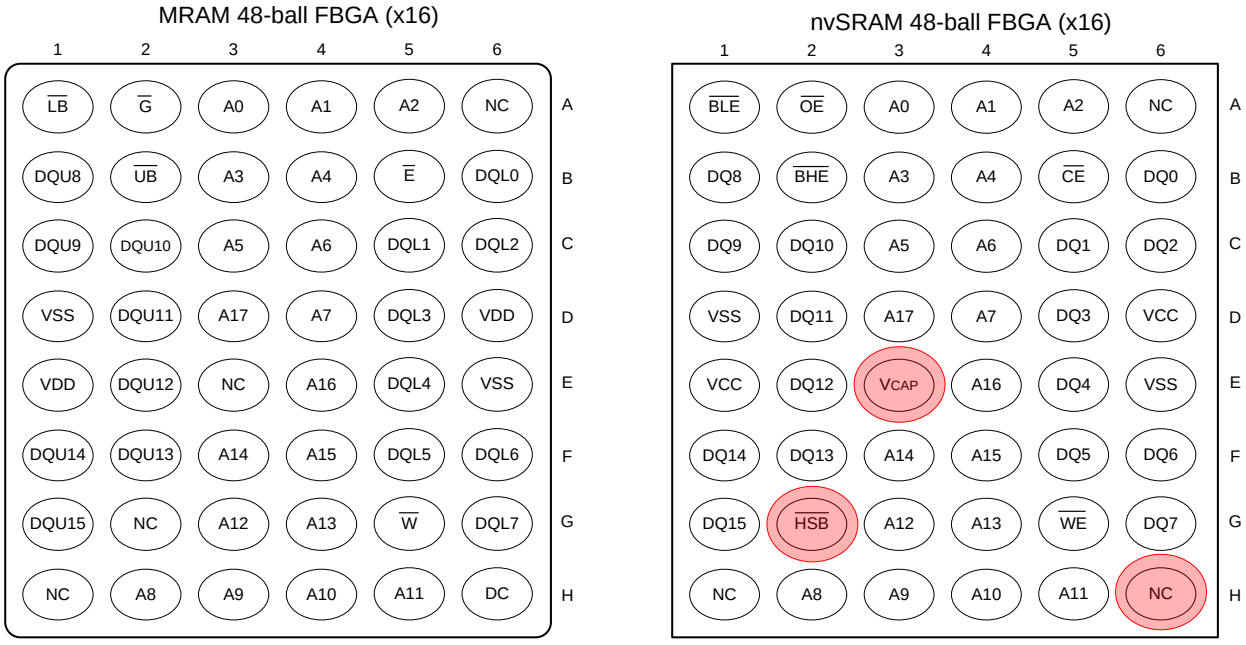
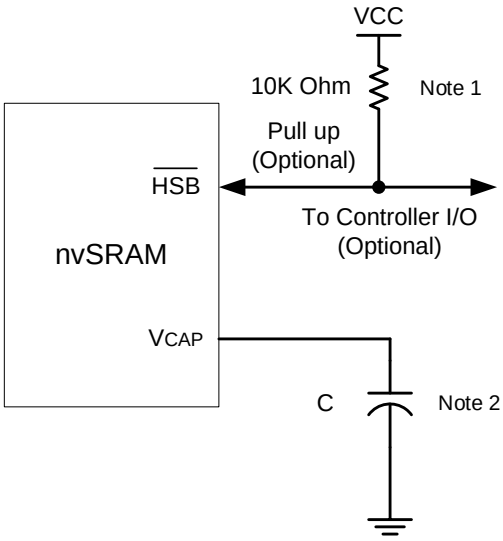


Figure 3. nvSRAM V_{CAP} and $\overline{HSB}$ Connection



Note 1: The nvSRAM $\overline{HSB}$ can be left floating (or NC) if its functionality is not used in the design. It is recommended to connect an external pull-up resistor of 4.7KΩ-10KΩ on the $\overline{HSB}$ pin if this pin is connected to a controller I/O for its control.

Note 2: The capacitor (C) on the nvSRAM V_{CAP} pin can be specified as DNI (Do Not Install) in the BOM while using MRAM instead of nvSRAM on the same footprint. The capacitor (C) should be installed when using the nvSRAM. Refer to AN43593 for selecting an appropriate V_{CAP}.

3 Other System Design Considerations

The nvSRAM's power circuitry is robustly designed to maintain its data integrity across all types of power supply ramp rates or brown out conditions which can be observed in a system setup. The nvSRAM does not put any condition on its power-up and power-down behavior. The following sections explain nvSRAM behavior during power-up and power-down cycles.

3.1 Power Up

When the nvSRAM V_{CC} power supply crosses an internal threshold (V_{SWITCH}) level, the device starts boot-up sequence followed by memory RECALL, which recalls user data from its nonvolatile memory cell to SRAM and becomes ready for the access. The nvSRAM takes maximum 20 ms ($t_{HRECALL}$) to complete its boot-up sequence before the controller can access the part. The nvSRAM's I/Os remains disabled during $t_{HRECALL}$ time therefore none of the I/Os require tracking to the power supply during power-up as in the case of MRAM. The MRAM requires its control signals ($\overline{E}$ and $\overline{W}$) to track the power supply during power-up and must be held high for a 2 ms start-up period after the power supply reaches the MRAM minimum operating voltage (V_{DD} min).

The nvSRAM recommends a 4.7 kΩ -10 kΩ pull-up resistor on its write enable ($\overline{WE}$) control line to avoid any unwanted write in case if controller is still booting-up and its I/Os remain tri-stated or floating while nvSRAM becomes ready after its boot-up cycle. This issueisalso applicable to MRAM if the device is not write-protected properly in case of floating controller I/Os. Data corruption due to unwanted write in MRAM is permanent and irreversible, whereas it is reversible in caseof nvSRAM. The nvSRAM retains a copy of the most recently stored user data in its nonvolatile memory which is recalled to the SRAM portion of the memory cell during power-up recall, therefore the host controller can easily recover the original data by executing software RECALL and replace the corrupted SRAM data with correct user data.

3.2 Power Down

When the nvSRAM V_{CC} power supply falls below (V_{SWITCH}) threshold, the device initiates the AutoStore operation internally using stored charge on the small capacitor connected to its V_{CAP} pin. When the nvSRAM loses V_{CC} power when a write cycle has been initiated and is still in progress, the write cycle will be allowed to complete before data transfer from the SRAM portion of the cells to nonvolatile elements begins. This ensures that the last data word successfully written to the nvSRAM is saved during AutoStore. Once an AutoStore cycle starts in the nvSRAM, the nvSRAM I/Os are disabled and internal circuitry automatically switches from V_{CC} power to the V_{CAP} power source.

4 Summary

Cypress nvSRAM's pinout is similar to the MRAM pinout except for the V_{CAP} pin which is typically a no connect (NC) pin in MRAM. Customers using a MRAM can easily migrate to nvSRAM by designing a provision on the PCB to connect a capacitor on the V_{CAP} pin. The capacitor can be left in place when MRAM is used on the board with no influence on the MRAM. Including V_{CAP} allows nvSRAM and MRAM to be used as alternate sources in applications requiring NVRAM performance. The remainders of the pins provide identical functionalities for both MRAM and nvSRAM.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1200303	ZSK	06/29/2007	Obtain spec# for note to be added to spec system. This note had no technical updates. Kindly replace existing .pdf file on http://www.cypress.com.
*A	3125574	ZSK	01/02/2011	Updated Introduction. Updated in new template.
*B	3756324	ZSK	09/27/2012	Added section “Other System Design Considerations”. Updated Summary. Updated template.
*C	3908795	ZSK	02/20/2013	Updated Abstract to include 4-Mbit specific description. Added package dimension tables (Table 1 and Table 2). Included 48-ball FBGA package option. Update the title to “Replacing 4-Mbit (256Kx16) MRAM with Cypress nvSRAM”.
*D	4677354	KAHA	03/03/2015	Updated the document as per new template. Corrected Figure 1.
*E	4758359	ZSK	05/07/2015	Update the application note landing page link: http://www.cypress.com/go/AN6068. Formatted the document as per new template.

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