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WHITEPAPER

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Addressing Serial SRAM Needs with F-RAM

Abstract

This white paper shows how F-RAM™ can be used to replace serial SRAM devices in new and existing designs. After highlighting the key attributes of the technologies, the similarities of both are provided. Any minor differences required to support F-RAM are listed for SRAM replacement. Finally, there are a number of advantages to systems that replace serial SRAM with F-RAM alternatives, and the end customer-visible advantages are discussed.

Introduction

Though Static RAMs and Ferro-Electric RAMs (F-RAM™) can have quite different purposes, with the advent of standard interfaces such as SPI, these technologies have large overlap in their capabilities.

This white paper details the common attributes of SRAM and F-RAM, which provided the primary motivation for the replacement of serial SRAM in the design. Considerations that need to be made in the replacement of SRAM with F-RAM are detailed. This document also provides the analysis required to make certain there are no issues. Finally, the paper describes the advantages of migrating to F-RAM, which directly result in customer-visible benefits.

Similarities Between SRAM and F-RAM

SRAM and F-RAM exhibit many similar properties in many designs. Serial SRAMs and F-RAMs have similar memory densities, can support completely random read-write access, and all results can be obtained without additional delays. Given that both parts have implementations using SPI interfaces, it is obvious to think that these parts can be used interchangeably in most designs. The following sections describe the common attributes of these technologies.

Memory Capacities

Serial SRAMs available in the market today support capacities from 64 Kbits to 1 Mbit. Today, F-RAM devices have capacities ranging from 4 Kbit to 4 Mbit. In addition, new versions of F-RAM, which support Ultra Low Energy, will support even higher capacities in the future, up to 16 Mbits.

Instant Read/Write Random Access

Both SRAM and F-RAM support instant read or write operations. Other technologies can experience long delays for either reads and/or writes. In addition, accesses can be made with SRAM and F-RAM to completely random addresses, without limitations of block sizes.

SPI Addressing Without Implementation-Specific Boundaries

In default operating modes, both F-RAM and SRAM allow access to the entire contents of the device in a single transfer, with either read or write operations.

SPI Standard Implementations

Both SRAM and F-RAM support SPI interfaces. Serial SRAM products support SPI at lower densities, and multibit Dual SPI (DSPI) and Quad SPI (QSPI) at densities of 512 Kbit and above. Current F-RAM parts support only SPI today, but ULE F-RAM devices support all SRAM interfaces. All these implementations are provided in some form of an 8-pin package.

Common Capabilities of SRAM and F-RAM Technologies Summary

At the highest level, base functions of SRAM and F-RAM are identical—capacities of random access memory from Kilobits to small number of Megabits that is instant-stored in memory. This memory is without special configuration or page boundaries, and standard SPI physical pinout is supported.

F-RAM Considerations

There are a few subtleties that need to be mentioned when F-RAM is used instead of SRAM. This section describes these minor differences, and highlights mitigation steps that can be taken.

When these preventative steps are taken, it is important to understand which version of F-RAM is being used. Legacy F-RAM parts implement only single-bit SPI interfaces, while ULE F-RAM has a number of different operating modes that can be used.

Register Access

Serial SRAM has a single status register, shown in the table below:

Description	Bit Position							
Bit Number	7	6	5	4	3	2	1	0
Permissions	R/W	R/W	RFU	RFU	RFU	RFU	RFU	RFU[1]
Use	Indicates or sets the part in byte, page, or sequential mode							

It should be noted that the SRAM use of the status register is rare—it contains no information of value at runtime. Accesses to this register are not compatible with either version of F-RAM.

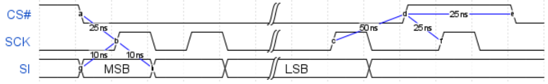
Additional Addressing Modes

SRAM has additional wrap-around modes not supported by either version of F-RAM. Byte mode allows only single-byte operations, but this mode would usually work in F-RAM if only a single byte of data is supplied in the read or write command. Page mode breaks the memory into aligned 32-byte pages, and operations within a page wrap around in the page. The only way to implement page mode with an F-RAM is to add code to the MCU to detect operations that would cross page boundaries, and break them into separate commands by the software. The default mode of SRAM is the sequential mode, which operates exactly in the same way as both versions of F-RAM, in which addresses wrap around only at the device capacity.

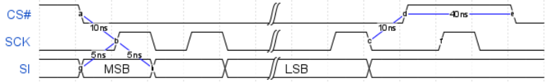
AC Timing

SRAM AC timing is subtly different from that of F-RAM, but is likely completely transparent to either device, or can be made so by the design. In the figures below, clock timings for SRAM and F-RAM are provided. The trailing edge of the CS# signal is measured differently between the two designs, but if all timing is met at the necessary clock speed, it is possible to have a single design support either SRAM or F-RAM.

[1] Used by some versions of the device to enable the HOLD function on the SPI interface.



SRAM Timing



F-RAM Timing

Command Differences

Serial SRAM has a limited command set. Legacy F-RAM commands are even more limited, when starting with the SRAM functions alone. ULE F-RAM implements all modes of serial SRAM with the fewest changes required. Command sets of each of these parts are described in the following sections.

Serial SRAM Command Set

Serial SRAM has seven total commands, as described in the following table:

Serial SRAM Commands

Command Name	Hex Opcode	Description
WRMR	0x01	Write Mode Register
WRITE	0x02	Write data to the memory array beginning at the selected address in the current data width
READ	0x03	Read data from the memory array beginning at the selected address in the current data width
RDMR	0x05	Read Mode Register
EQIO	0x38	Enter Quad I/O access mode (QSPI)
EDIO	0x3B	Enter Dual I/O access mode (DSPI)
RSTIO	0xFF	Enter Single I/O access mode (SPI)

Because the register issues have already been dealt with in the Register Access section, it will not be discussed in the command sets below.

Legacy F-RAM Command Set and Mitigation

Because legacy F-RAM supports only SPI mode, the command set is even smaller. Read commands with legacy F-RAM are completely compatible with serial SRAM.

However, all legacy F-RAM implementations require that a WREN (opcode 0x06) be prepended to the write command. This requires a software change for writing the device.

ULE F-RAM Command Set and Mitigation

ULE F-RAM supports all modes supported by serial SRAM. SPI and QSPI mode are completely compatible between the two technologies, as well as all read and write commands. The sole difference between serial SRAM and ULE F-RAM is the opcode to enter DSPI mode. For ULE F-RAM, this opcode is changed to 0x37.

Endurance

SRAM has infinite endurance—it can be read or written to indefinitely without limit. F-RAM has a high (number), limiting the application to reading or writing a single byte no more than a specified number of cycles. The best method of mitigation is knowing the implementation is correct by design. This can be done by knowing a few details about the software usage:

1. *What is the actual SPI implementation to be used (SPI data width and clock rate)?* Setting the clock and data width also affects the time between consecutive accesses.

2. *Is the product idle or inactive for a part of the time?* Periods of inactivity, such as a usage model that would use the product only 50% of the time, would allow the product lifetime goals to be met even with short access times.

3. *Can large sequential accesses be used to access the critical data structures?* SPI accesses allow sequential operations, which increment the address. It is possible that just by adding sequential transfers to these device accesses, the endurance problem is mitigated.

4. *What is the shortest time between operations to a single memory location in software?* This may depend on the data structures used (LIFO versus FIFO), or whether the memory is used as a scratchpad (time between uses as measure by the MCU). This also depends on whether the implementation's MCU uses the SPI interface as a peripheral or as a memory-mapped device. Peripherals require setup and teardown times for each command, lengthening the time between operations to the same location. Memory-mapped devices might require measurements of the calls and returns of the programs to determine the worst-case time between stack operations.

Let's use an example to show how the endurance of F-RAM in product design can be calculated. Let's start with the worst-case specifications for the design: 20-MHz QSPI operated continuously. If we look at the worst-case F-RAM endurance for 'malicious' software—that which only accesses a single byte at this rate forever—the specified endurance of the part would be about 1.71 years at 10^{14} cycles, which is too short for most implementations. If our goal is a 10-year product lifetime, any of the following mitigations could be used to achieve this. Use any of the following approaches to ensure that there are no F-RAM endurance problems, because all design requirements for product endurance would have been met.

- Reduce the clock rate to 3.2 MHz.
- Use the product only 4 hours per day.
- Make the transfer size 28 bytes or higher.
- Design the software to prevent accesses to the same location for 3.2 microseconds.

Benefits for F-RAM Products

There are several reasons that should be mentioned as to *why F-RAM may be better than serial SRAM* for a particular product design. Some of these considerations are described in the following sections.

Superior Frequency and Bandwidths

Both legacy and ULE F-RAMs support higher SPI clock frequencies than serial SRAM. In addition, ULE F-RAM supports DDR modes, making the best use of low-pinout MCUs. ULE F-RAM can provide five times the bandwidth of the currently available serial SRAMs.

ECC Data Protection

All F-RAM arrays are protected with ECC, and additional control registers are provided for monitoring ECC errors. SRAM does not have this capability. As a result, SRAM may be subject to corruption events, while these would be detected and corrected by the F-RAM.

Reduced Power

F-RAM, both legacy and ULE, uses less active power than serial SRAM in all operating conditions. If the product is dominated by active power of memory, F-RAM provides lower power.

If the design is dominated by idle power, serial SRAM has slightly lower standby power, but ULE F-RAM implements additional power modes which are lower. Software must be changed to enter these low-power states, but ULE F-RAM can be 10x lower idle power than serial SRAM if these states are used.

RoHS Compliant Non-Volatility

Non-volatility is inherent in F-RAM, but power must be provided to a serial SRAM to obtain this. This can mean the addition of a battery, which might violate RoHS requirements, or become a replacement issue in the design.

Command Options for Easier Use

ULE F-RAM has a much richer command set than SRAM, and these functions can be used to provide easier implementations. A few of these considerations are:

- Ability to use other modes for transfer, such as single-bit commands, but multibit data transfer
- Ability to write-protect portions of the memory array.
- Serial number identification

None of these provisions is available in serial SRAM.

Summary

We are used to the functions of SRAM and the benefits it provides to products today. However, it turns out that there is another technology that does the same things, better in many cases. With a bit of up-front thought, F-RAM can be used to replace serial SRAMs, and in many cases, provide better performance, lower power consumption, and a more reliable data storage environment.

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