



Application Note

AN2209

PSoC Designer™ Device Selection Guide – AN2209

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Associated Project: No

Associated Part Family: CY8C20x34, CY8C21x23, CY8C21x34, CY8C24x23A, CY8C24x94, CY8C27x43, CY8C29x66, CY7C603xx, CY7C64215, and CYWUSB6953

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Abstract

- View [Figure 1 – PSoC Device Decision Tree](#) for quick help on choosing a PSoC® device.
- View [Table 1 – User Modules](#) for help on understanding resource requirements related to specific functionality.
- There are several important PSoC specifications to be aware of when you are choosing a PSoC device. An explanation for each of these is provided below.
- PSoC Designer also supports the following Cypress devices: CY7C603xx, CY7C64215, and CYWUSB6953. An explanation for each of these is provided below.

Blocks

PSoC blocks allow the same part to be quickly and easily configured with literally hundreds of different function sets. These function sets can span both analog and digital. PSoC part families contain different numbers of PSoC blocks; every part within a specific family contains the same number of blocks. In the digital subsystem, the number of blocks ranges from four to sixteen. In the analog subsystem, the number of blocks ranges from three to twelve. For example, all parts within the CY8C24x23A family have exactly six analog blocks and four digital blocks.

The number of PSoC blocks a project requires depends on the type and number of required functions. These functions are analogous to on-chip peripherals. Functions implemented in PSoC blocks are called PSoC User Modules. There are dozens of User Modules accessible in PSoC Designer. They include ADCs, DACs, PWMs, filters, timers, counters, UARTs and more.

User Modules utilize different PSoC blocks. For example, a 14-bit Incremental ADC User Module requires 4 digital blocks and 1 analog block, where as an 8-bit PWM User Module requires only 1 digital block. Each PSoC User Module has its own data sheet that includes the number of PSoC blocks required to implement the User Module.

These User Module data sheets can be accessed from within PSoC Designer or downloaded from www.cypress.com/psoc.

There are two types of digital blocks: basic and communication. Digital blocks are arranged into rows; each row contains two basic blocks and two communication blocks. Communication User Modules, such as a UART, must be placed in communication blocks. Basic User Modules, such as a PWM, can be placed in either basic or communication blocks. Because of this, communication blocks are the more valuable resource.

There are four types of analog blocks: continuous time B, switched capacitor C, switched capacitor D, and continuous time type E. Continuous time B blocks utilize a traditional resistor approach to effect the movement of charge, while both switch capacitor C and D blocks utilize switched capacitors to effect the movement of charge.

For details on resource requirements associated with specific User Modules, see [Table 1 – User Modules](#).

Flash

The PSoC, as a programmable device, utilizes a unique Flash process (SONOS: Silicon Oxide Nitrous Oxide Silicon semiconductor) that is both reliable and cost effective as compared to competing Flash technologies.

The low cost is achieved because the SONOS process is built on a standard CMOS wafer and requires only three additional layers to create the NV cell.

The reliability is achieved because the SONOS "capacitor" stores the charge in a nitride memory layer making the memory cell much more tolerant of defects in the gate oxide. The Flash is guaranteed for 50,000 erase write cycles

PSoC device families have different amounts of Flash. Every part within a family contains the same amount of Flash. For instance, all parts within the CY8C29x66 family have 32K of Flash. Currently, families range from having 4K of Flash on up to 32K of Flash.

Program size will determine the amount of Flash required.

IO Count

The PSoC offers a great deal of flexibility in how the pins are used. Inputs/Outputs are arranged in ports; each port has 8 IOs (except in 8-pin devices). Depending on the specific PSoC, there are between 1 and 8 ports (6 to 64 IO). All ports can be used as digital IO. Only ports zero and 2 can be used as analog inputs.

There are eight different selectable drive modes for each IO (High Z, High Z Analog, Open Drain High, Open Drain Low, Pull Down, Pull Up, Strong, and Strong Slow). There are three different selectable interrupt triggers for each IO (Falling Edge, Rising Edge, and Change from Last Read).

The number of signals that the PSoC will need to interface will largely dictate the amount of IOs needed in a project.

FS USB

Full-speed USB (12 Mbps and USB 2.0 compliant) is available in the CY8C24x94 PSoC device family. (The CY8C24894 device is the recommended device for designs requiring up to 49 digital IO.) This includes four uni-directional endpoints, one bi-directional control endpoint, and a dedicated 256-byte buffer. No external crystal is required.

RAM

RAM is used to store project variables and the system stack. PSoC device families have different amounts of RAM. Every part within a specific family contains the same amount of RAM. For instance, all parts within the CY8C29x66 family have 2K of RAM. Currently, families range from having 128 bytes of RAM up to 2K of RAM.

The number of local and global variables a project contains and how the stack is used will dictate how much RAM is required.

Supply Voltage

The supply voltage range for PSoC can vary from 1.8V to 5.25V. Every part within a single family has the same supply voltage range. For example, all parts within the CY8C27x43 family have a 3.0V to 5.25V supply voltage range.

CPU speed is dependent upon the supply voltage. At 5.25V, the CPU speed can be set to 24 MHz, but at 3.0V, the maximum speed is 12 MHz. At 2.4V, the maximum speed is 3 MHz. It is therefore important to consider the desired CPU speed when choosing a supply voltage range.

Temperature

The temperature range classifications that are applicable to the PSoC are the Automotive, Commercial, Extended Commercial, and Industrial. The temperature range classification is from -40°C to 125°C.

Package

There are seven different package types available for the PSoC: PDIP, SSOP, SOIC, TQFP, TSSOP, QFN/MLF and VFBGA. Package dimensions are detailed in each data sheet. Packages have different sizes, but the number of pins that a specific device has also affects the device's size. A 32-Pin QFN/MLF (i.e., CY8C24423A-24LFXI) is 5x5 mm, where as a 48-Pin QFN/MLF (i.e., CY8C27643-24LFXI) is 7x7 mm.

PSoC emulation tools may require additional board space surrounding the chip footprint, especially a QFN/MLF package. For a description of the emulation board layout requirements, please consult the [PSoC Emulator Pods Dimensions](#) document.

Supported Non-PSoC Devices

Wireless enCoRe II CY7C603xx

The Wireless enCoRe II CY7C603xx device is based on the flexible PSoC architecture. A simple set of peripherals is supported that can be configured as required to match the requirements of each application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

enCoRe(TM) III Full-Speed USB Controller

The enCoRe III merges the USB performance of the enCoRe family with the superior flexibility of the PSoC family. It is a highly flexible, full-featured Full-Speed USB device that enables users with a high level of integration in consumer applications. The enCoRe III is powered by the powerful M8C processor and offers users 16KB of Flash. The enCoRe III allows the user to choose from a list of peripheral configurations for increased functionality. The peripherals available to the user are listed below:

- Pulse Width Modulators
- Full Duplex UARTs
- SPI Master and Slave
- Analog-to-Digital Converter
- I2C Master and Slave

WirelessUSB(TM) PRoC(TM) Flash Programmable MCU + Radio

The CYWUSB6953 WirelessUSB(TM) PRoC(TM) (Programmable Radio System-on-Chip) device is the world's first low-cost Flash programmable microcontroller with an integrated 2.4-GHz radio transceiver.

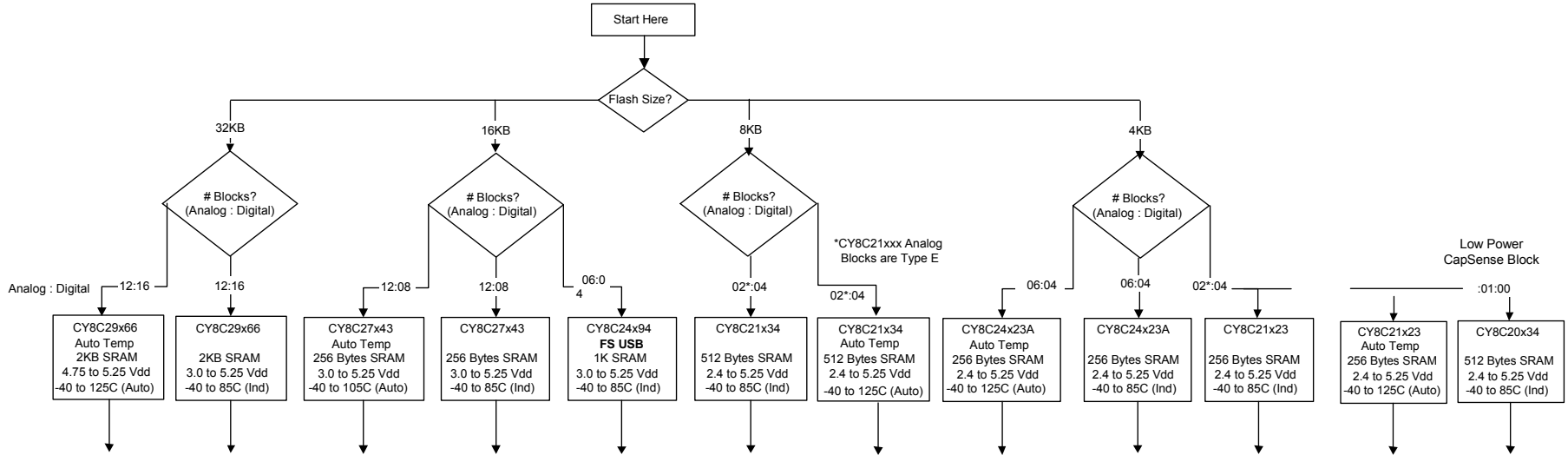
The CYWUSB6953 is a complete Radio System-on-Chip device, enabling many simple RF systems to be implemented with a single device and a handful of discrete components. It is designed to implement low cost wireless systems operating in the worldwide 2.4-GHz Industrial, Scientific, and Medical (ISM) frequency band (2.400 GHz–2.4835 GHz).

The microcontroller is a powerful mixed-signal array. It has highly reconfigurable and flexible digital and analog blocks. The microcontroller core is the M8C 8-bit engine that supports a rich instruction set. It contains 512 Bytes of data SRAM and 8 Kbytes code Flash memory.

Selecting a PSoC Device

To select a specific device, follow these steps:

1. Define your required functions by sketching a block diagram.
2. Use [Table 1 – User Modules](#) to determine what User Modules you will need to implement the functions detailed in your block diagram.
3. Use [Figure 2 – PSoC Worksheet](#) to sketch out the placement of User Modules and to determine routing and pin selection.
4. Define other resource requirements such as Flash, RAM and package.
5. Use [Figure 1 – PSoC Device Decision Tree](#) to pick your device based on your sketch and other resource requirements.



8 PDIP	6 IOs				CY8C27143-24PXI					CY8C24123A-24PXI			
8 SOIC	4/6 IOs									CY8C24123A-24SXI	CY8C21123-24SXI		
16 QFN	13 IOs												CY8C20234-12LKXI
16 SOIC	8/12 IOs							CY8C21234-24SXI				CY8C21223-24SXI	
16 TSSOP	10 IOs												
20 PDIP	16 IOs									CY8C24223A-24PXI			
20 SOIC	16 IOs									CY8C24223A-24SXI			
20 SSOP	16 IOs			CY8C27243-12PVXE	CY8C27243-24PVXI		CY8C21334-24PVXI	CY8C21334-12PVXE	CY8C24223A-12PVXE	CY8C24223A-24PVXI	CY8C21323-24PVXI	CY8C21323-12PVXE	
24 QFN	16/20 IOs										CY8C21323-24LFXI		CY8C20334-12LFXI
28 PDIP	24 IOs		CY8C29466-24PXI		CY8C27443-24PXI					CY8C24423A-24PXI			
28 SOIC	24 IOs		CY8C29466-24SXI		CY8C27443-24SXI					CY8C24423A-24SXI			
28 SSOP	24 IOs	CY8C29466-12PVXE	CY8C29466-24PVXI	CY8C27443-12PVXE	CY8C27443-24PVXI		CY8C21534-24PVXI	CY8C21534-12PVXE	CY8C24423A-12PVXE	CY8C24423A-24PVXI			
32 QFN	24/28 IOs						CY8C21434-24LFXI			CY8C24423A-24LFXI			CY8C20434-12LKXI
32 QFN	26 IOs						CY8C21634-24LFXI						
44 TQFP	40 IOs		CY8C29566-24AXI		CY8C27543-24AXI								
48 QFN	44 IOs		CY8C29666-24LFXI		CY8C27643-24LFXI								
48 SSOP	44 IOs	CY8C29666-12PVXE	CY8C29666-24PVXI	CY8C27643-12PVXE	CY8C27643-24PVXI								
56 QFN	50 IOs						CY8C24794-24LFXI						
56 QFN	49 IOs						CY8C24894-24LFXI						
68 QFN	56 IOs						CY8C24994-24LFXI						
100 TQFP	64 IOs		CY8C29866-24AXI										
100 VFBGA	56 IOs						CY8C24994-24BVXI						

Table 1. User Modules, All Supported Devices

Module	Analog	Digital	Flash	SRAM	Chip													Features		
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx		CY7C642xx	CYRF69xx3
ADCs																				
ADC8	2	1	209	2		•	•						•							8 bits, 8.8 ksps
ADC10	1CT, 1SC	1	209	4		•	•						•							10 bits, 7.35 ksps
ADCINC12	1	1	209	6				•	•	•	•									12 bits, 7.8 – 480 sps
ADCINC14	1	4	262	6				•	•	•	•									14 bits, 2 – 120 sps
ADCINCVR	1	3	309	5				•	•	•	•									7 – 13 bits, 4 – 10 ksps
ADCINC	1	1	-	8				•	•	•	•							•		6 – 15 bits, up to 46.8 ksps
DELSIG8	1	1	143	8				•	•	•	•									8 bits, 0.125 – 31.25 ksps
DELSIG11	1	1	208	12				•	•	•	•									11 bits, 125 – 7.8 ksps
DELSIG	1	1	89	2					•	•	•									6 – 14 bits, up to 65.5 ksps
DUALADC	2	4	455	8					•	•	•									7-13 bits, 4 – 10 ksps
DUALADC8	2	4	312	9					•	•	•									8 bits, 122 – 7600 sps
SAADC	1CT, 1SC	0	237	4															•	8 bits, 100 sps
SAR6	1	0	58	0				•	•	•	•									6 bits, 40 ksps
TRIADC	3	5	604	11																7 – 13 bits, 4 – 10 ksps
TRIADC8	3	5	416	11																8 bits, 4 – 10 ksps
Amplifiers																				
AMPINV	1CT	0	52	0				•	•	•	•									18 gain options, max gain of -47
CMP	1CT	0	17	0		•	•						•						•	2 input comparator
CMP		CS	141	0	•															2 comparators, 2 inputs each
CMPPRG	1CT	0	52	0				•	•	•	•									Programmable threshold & reference
INSAMP									•	•	•	•								
Two Opamp	1CT	0	57	0					•	•	•	•								Programmable gain from 2 to 16
Three Opamp	1CT	0	113	0					•	•	•	•								Programmable gain up to 93
PGA	1CT	0	52	0				•	•	•	•									30 gain options, max gain of 48

Module	Analog	Digital	Flash	SRAM	Chip													Features			
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx		CY7C642xx	CYRF69xx3	
Analog Comm																					
DTMFDialer																					
Background	1	1	766	16				•	•	•	•	•									System control while dialing
Foreground	1	1	761	2																	Minimize use of RAM
Cap Sensors																					
CSA		1CS	~1200	129	•																1 to 28 switches; 5 to 28 slider elements
CSD	1CT, 1SC	3	~900	23			•			•											1 to 28 switches; 5 to 48 slider elements
CSR	1CT	3	1392	198			•			•											1 to 28 switches; 5 to 48 slider elements
Counters																					
Counter8	0	1	67	0		•	•	•	•	•	•	•									8 bits, programmable pulse width
Counter16	0	2	88	0		•	•	•	•	•	•	•									16 bits, programmable pulse width
Counter24	0	3	129	0		•	•	•	•	•	•	•									24 bits, programmable pulse width
Counter32	0	4	147	0		•	•	•	•	•	•	•									32 bits, programmable pulse width
DACs																					
DAC6	1	0	61	0				•	•	•	•	•									6 bits, update rates up to 250 ksps
DAC8	2	0	147	0				•	•	•	•	•									8 bits, update rates up to 125 ksps
DAC9	2	0	151	0				•	•	•	•	•									9 bits, update rates up to 125 ksps
MDAC6	1	0	112	0				•	•	•	•	•									6 bits, update rates up to 250 ksps
MDAC8	2	0	205	0				•	•	•	•	•									8 bits, update rates up to 125 ksps

Module	Analog	Digital	Flash	SRAM	Chip													Features		
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx		CY7C642xx	CYRF69xx3
Digital Comm																				
CRC16	0	2	54	0		•	•	•	•	•	•	•	•							2 – 16 bits, data clocking to 48 MHz
EzI2CS					•	•	•	•	•	•	•	•								Slave, 100/400 kbits/s
RAM Read/Write Buffers	0	0	264	6																
Additional for Flash Read Buffer Support	0	0	379	2																
I2CHW						•	•	•	•	•	•	•					•		•	50, 100, 400 kbits/s; 7- & 10-bit addressing
Slave	0	0	243 – 564	6 – 9																
Master	0	0	1021 – 1668	7 – 9																
Multi Master Slave	0	0	1311 – 2313	13 – 17																
I2CHW (Slave only)		I2C	279 – 440	8	•															50, 100, 400 kbits/s; 7- & 10-bit addressing
I2Cm	0	0	597	4		•	•	•	•	•	•	•							•	100 kbits/s
I2Cm		I2C	736	4	•															
IrDARX	0	2CB	66	0		•	•	•	•	•	•	•								Max receive rate of 115.2 kbits/sec
IrDATX	0	2CB	53	0		•	•	•	•	•	•	•								Max transmit rate of 115.2 kbits/sec
RX8	0	1CB	34	0		•	•	•	•	•	•	•								Burst rates up to 6 Mbits/sec
SPIM	0	1CB	37	0		•	•	•	•	•	•	•					•	•	•	0, 1, 2, & 3 SPI clocking modes supported
SPIM		I2C	27	0	•															
SPIS	0	1CB	43	0		•	•	•	•	•	•	•								0, 1, 2, & 3 SPI clocking modes supported
SPIS		I2C	43	0	•															
TX8	0	1CB	34	0		•	•	•	•	•	•	•								8 bits, clocking up to 48 MHz, 6 Mbits data rate max
UART						•	•	•	•	•	•	•								RS-232-compliant, burst rates up to 6 Mbits/sec
Low Level API	0	2CB	66	0																Max supported data rate 115.2 kbits/second

Module	Analog	Digital	Flash	SRAM	Chip													Features			
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx		CY7C642xx	CYRF69xx3	
enCoRe II User Modules																					
E2PROM	0	0	727	varies										•	•	•	•			•	Full byte-oriented EEPROM emulation
MSTIMER	0	0	19	0										•	•	•	•			•	12-bit interval timer
PITIMER12	0	0	57	0										•	•	•	•			•	12-bit programmable interval timer
PS2D														•	•	•	•				PS/2 device interface integrated with the USB SIE for USB-PS/2 combo
Mouse Support	0	0	935	17																	SRAM value includes 4 byte transfer
Keyboard Support	0	0	810	17																	SRAM value includes 4 byte transfer
SPIM														•	•	•	•				
USB	0	0	1499	41																•	USB Device Interface Driver
HID Class Driver (opt)	0	0	461	27																	
String Descriptor (opt)	0	0	~40	0																	9 Flash overhead for each String Descriptor
Filters																					
BPF2	2	0	109	0				•	•	•	•										Programmable mid-b& gain, center frequency, & Q; sampling rates up to 1.0 MHz
LPF2	2	0	109	0					•	•	•	•									Programmable gain, corner frequency, & damping ratio; sampling rates up to 1.0 MHz
Generic																					
SCBLOCK	1	0	20	0				•	•	•	•										Fully parameterized for custom development

Module	Analog	Digital	Flash	SRAM	Chip													Features	
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx		CY7C642xx
Misc. Digital																			
DigBuf	0	1	9	0		•		•	•	•	•	•							
DigInv	0	1	36	0		•		•	•	•	•	•							
E2PROM	0	0	439 + Size	13		•	•	•	•	•	•	•			•	•	•		
LCD					•	•	•	•	•	•	•	•			•		•		
Bar Graph Enabled	0	0	622	0															
Bar Graph Disabled	0	0	442	0															
SleepTimer	0	0	150	4 to 7		•	•	•	•	•	•	•							
MUXs																			
AMUX4	0	0	25	0		•		•	•	•	•	•							
AMUX8	0	0	44	0		•		•	•	•	•	•							
RefMux	1CT	0	32	0				•	•	•	•	•							
Protocols																			
Bootloader I2C	0	0				•	•	•	•	•	•	•				•	•		
Bootloader USBFS	0	0	1911	46					•	•	•	•					•	•	
USBFS	0	0	500	10						•	•	•						•	•
USBUART	0	0	1900	60						•	•	•							•
PWMs																			
PWM8	0	1	67	0		•	•	•	•	•	•	•			•		•		
PWM16	0	2	89	0		•	•	•	•	•	•	•							
PWMDB8	0	2	35	0		•	•	•	•	•	•	•							
PWMDB16	0	3	44	0		•	•	•	•	•	•	•							

Module	Analog	Digital	Flash	SRAM	Chip													Features			
					CY8C20x34	CY8C21x23	CY8C21x34	CY8C22x13	CY8C24x23A	CY8C24x94	CY8C27x43	CY8C29x66	CYWUSB6953	CY7C601xx	CY7C602xx	CY7C603xx	CY7C63xxx	CY7C642xx	CYRF69xx3		
Random Sequence																					Data input clocking up to 48 MHz, serial output bit stream
PRS8	0	1	41	0		•	•	•	•	•	•	•									2 – 8 bits
PRS16	0	2	54	0		•	•	•	•	•	•	•									2 – 16 bits
PRS24	0	3	82	0		•	•	•	•	•	•	•									2 – 24 bits
PRS32	0	4	93	0		•	•	•	•	•	•	•									2 – 32 bits
Temperature																					
FlashTemp	1	0	74	3					•	•	•	•									Measures Flash temp., accuracy of $\pm 20^{\circ}\text{C}$ with no cal
Timers																					Source clock rates up to 48 MHz, capture up to 24 MHz
Timer8	0	1	70	0		•	•	•	•	•	•	•									8 bits
Timer13		TI	41	0	•																13 bits
Timer16	0	2	93	0		•	•	•	•	•	•	•									16 bits
Timer24	0	3	141	0		•	•	•	•	•	•	•									24 bits
Timer32	0	4	158	0		•	•	•	•	•	•	•									32 bits
WirelessUSB																					
WirelessUSBLS												•									2.4 GHz radio transceiver, 62.5 Kbits/sec
Non-Blocking Calls Enabled	0	0	1320	10																	
Non-Blocking Calls Disabled	0	0	1150	2																	

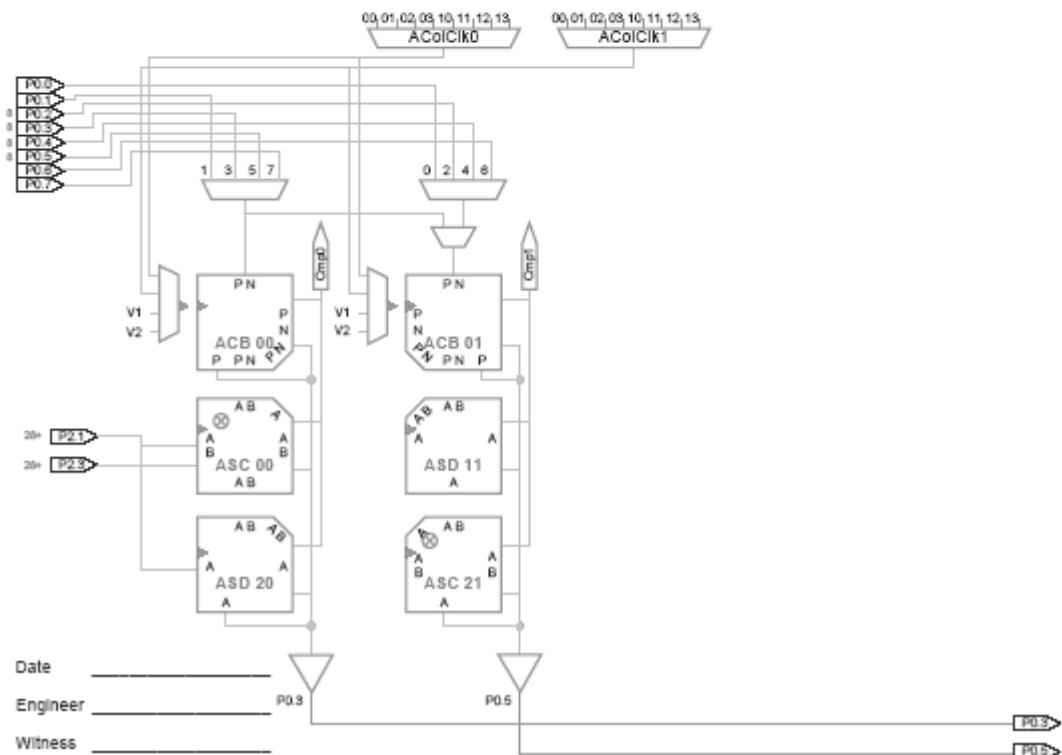
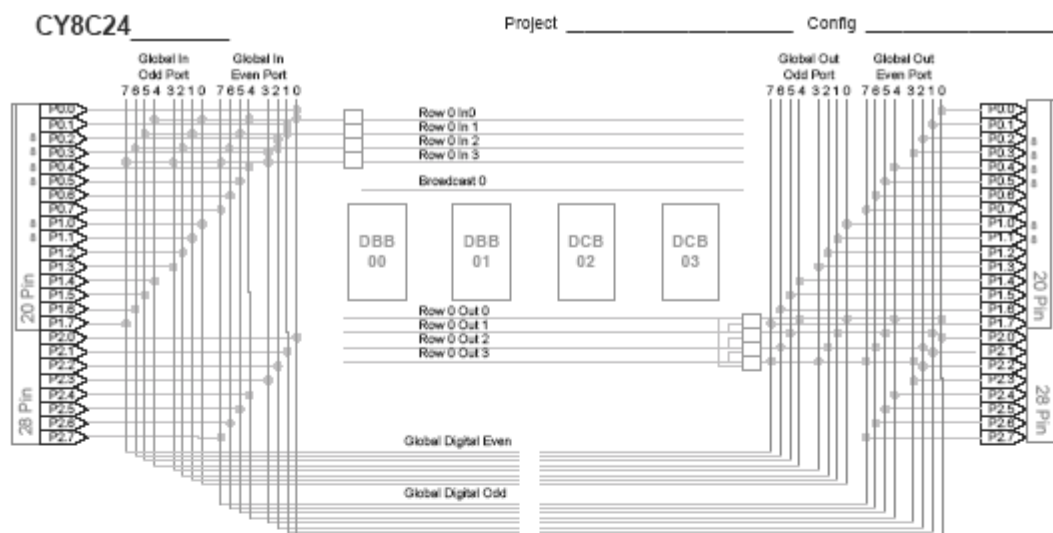
Note:

- CB – Communication block requirements
- CT – Continuous time block requirements
- CS – CapSense block requirements
- I2C – I2C/SPI block requirements
- SC – Switched capacitor block requirements
- TI – Timer block requirements

All other digital block requirements can be either basic blocks or communication blocks.

- The CY8C22x13 device family is not supported for new designs. Instead, try CY8C24x34A.

Figure 2. PSoC Worksheet – this worksheet is also accessible from within PSoC Designer’s \Documentation\PSoC Diagrams folder.



In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

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