

# S70GL02GS

## CS Q100082

Qualification of S70GL02GS, Two 1 Gigabit, 3.0 Volt-only Page Mode Flash Memories featuring 65 nm MirrorBit® process technology in LSH064 Package.



### Reliability Qualification Summary

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NOTICE: The material in this report is confidential. It is prepared to assist in the qualification of our product. It is declassified for the internal use of our customers only, and may be modified to meet the needs of specific customers. It also serves as a record of full qualification according to JESD47 and AEC-Q100 requirements.

Additionally, the package details (material set, assembly location, etc.) are specific to the qual vehicle used for the qualification. Alternate material sets and assembly locations may be qualified for the product. Production material can be assembled with any qualified material set and at any qualified assembly location. Tests are performed in accordance with AEC-Q100 and relevant JEDEC specifications.

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## I. Product Information

**Product Description:** S70GL02GS

Two 1 Gigabit, 3.0 Volt-only Page Mode Flash Memories featuring 65 nm MirrorBit® process technology

<b>Package:</b> LSH064	<b>Qualification:</b> Q100082
<b>Description:</b> (13 x 11 x 1.4mm) 64 Ball, Multi-Chip Fine Pitch Ball Grid Array Package (MCP)	
<b>Theta Ja:</b> 35 °C/W	<b>Psi Jt:</b> 11 °C/W
<b>Assembly Location:</b> Cypress Thailand	<b>Molding Compound:</b> RoHS Compliant Epoxy Resin
<b>Substrate/Leadframe:</b> Laminate Substrate	<b>Die Attachment:</b> Paste & Film
<b>Lead Finish:</b> 96.5Sn3.0Ag0.5Cu Spheres	<b>Bond Wire:</b> Gold
<b>Comments:</b>	

<b>Est. Field Temperature:</b> 55 °C	<b>Life Test Temperature:</b> 125 °C
<b>Est. DC Field Current:</b> 25 mA	<b>Life Test Dynamic Current:</b> 10 mA
<b>Est. Field Voltage:</b> 3.0 V	<b>Life Test Voltage:</b> 3.6 V
<b>Est. Field Power Dissipation:</b> 75 mWatts	<b>Est. Stress Power Dissipation:</b> 36 mWatts
<b>Est. Field Tj:</b> 57.6 °C	<b>Est. Stress Tj:</b> 126.2 °C

**Number of Dies:** 2

<b>Die #1:</b>	<b>Die:</b> 98661A	<b>Die Size:</b> 6.80 x 7.45 mm
<b>(Bottom)</b>	<b>Process:</b> CS239LS (65nm)	<b>Fab:</b> Cypress Fab25
	<b>Type:</b> MirrorBit Eclipse	<b>Density:</b> 1G
<b>Die #2:</b>	<b>Die:</b> 98661A	<b>Die Size:</b> 6.80 x 7.45 mm
	<b>Process:</b> CS239LS (65nm)	<b>Fab:</b> Spansion Fab25
	<b>Type:</b> MirrorBit Eclipse	<b>Density:</b> 1G



## II. CS239LS Life Test Failure Rate Calculation

### HTOL Stress Temperature - 125 °C

Failure Mechanism	Read Points / Test Results				Modeling Parameters @ 55 °C					Avg. Failure Rate FITS @ 55 °C, 60% Conf.	
	24 hrs	168 hrs	1000 hrs	2000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
<b>PLASTIC</b>											
Sample Size	4950	4615	842	50							
Zero fails, Process ave. Ea	0	0*	0	0	0.66	53	1	53		48	11
<b>Totals</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>					<b>10378</b>	<b>48</b>	<b>11</b>

\* Contributes to early life FITS

### Data Retention Bake - 150 °C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate %	Failure Mechanism
500 hrs	0	1735	0.00	No Failures
1000 hrs	0	1208	0.00	No Failures

### III. Summary of Stress Test Results

Stress Test	Stress Condition	Package Type	Sample Size	Num. of Lots	Num. of Fails	Failure Rate %	Comments
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**Data From Qualification Q100082:**

<b>ESD CDM</b>	N/A	LSH064 <sup>1</sup>	3	1		Passed 1.0kV	
<b>Preconditioning</b>	(PC1/260°C, +0°C/-5°C)	LSH064 <sup>1</sup>	154	1		Passed Jedec L3 / Jeita Rank E	
<b>Precon+Temp Cycle</b>	(PC1/260°C, -55°C/125°C)	LSH064 <sup>1</sup>	77	1	0	0.00	500 cycles
<b>Precon+uHAST</b>	(PC1/260°C, Unbiased, 130°C/85% RH)	LSH064 <sup>1</sup>	77	1	0	0.00	96 hours

**Generic Reference Data:**

<b>HTOL (EL)</b>	(3.6V, 125°C)	LAE064 <sup>2</sup>	288	4	0	0.00	168 hours
<b>Data Retention Bake</b>	(150°C)	LAE064 <sup>2</sup>	120	1	0	0.00	168 hours
<b>ESD CDM</b>	N/A	LAE064 <sup>2</sup>	15	1		Passed 1.0kV	
<b>ESD HBM</b>	(100pF, 1500 Ohms)	LAE064 <sup>2</sup>	84	1		Passed 2.0kV	
<b>Latch Up</b>	(125°C, +/- 100mA)	LAE064 <sup>2</sup>	6	1		Passed	
<b>Endurance (10k)</b>	(-40°C, 3.6V)	LAE064 <sup>2</sup>	100	2	0	0.00	10k cycles
	(90°C, 3.6V)	LAE064 <sup>2</sup>	100	2	0	0.00	10k cycles
<b>Preconditioning</b>	(PC1/260°C, +0°C/-5°C)	LAE064 <sup>2</sup>	385	2		Passed Jedec L3 / Jeita Rank E	
<b>Precon+Temp Cycle</b>	(PC1/260°C, -40°C/150°C)	LAE064 <sup>2</sup>	154	2	0	0.00	1000 cycles
<b>Precon+HAST</b>	(PC1/260°C, Biased, 110°C/85% RH)	LAE064 <sup>2</sup>	154	2	0	0.00	264 hours
<b>Precon+uHAST</b>	(PC1/260°C, Unbiased, 130°C/85% RH)	LAE064 <sup>2</sup>	77	1	0	0.00	96 hours

**Notes / Justification:** 1) Results from Qual Q100082, S70GL02GS, 1G CS239LS (65nm) MirrorBit Eclipse + 1G CS239LS (65nm) MirrorBit Eclipse in 64 Ball MCP (13 x 11 x 1.4mm)  
 2) Results from Qual Q99891, S29GL01GS in 64 Ball fBGA (9 x 9 x 1.4mm) - Same Flash in BGA Package

**Preconditioning Flows:** PC1 (Exceeds JEDEC L3 and JEITA Rank E): Bake 125°C, 24hr => Soak @ 30°C/70%RH, 216hr => 3x Reflow

## IV. Revision History

Section	Description
<b>Revision A - 8/12/2011</b>	
	Initial Release.
<b>Revision B - 12/19/2012</b>	
Cover Page, Section I: Packaging Details Section II: Technology Information Section III: Summary of Stress Test Data	Corrected typo of 90nm to 65nm. Updated technology to most recent data. Corrected Stress Data for same product.

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