# Cypress Roadmaps Slide Index

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Cypress Roadmap: Module Solutions
## Cypress Bluetooth Module Portfolio

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</tbody>
</table>

### Notes:
1. Extended range power
2. Power amplifier/Low-noise amplifier
3. Universal digital block
4. No shield
5. No certifications
6. Bluetooth SIG Mesh Qualified
7. Pre-programmed with Cypress' EZ-Serial Firmware
8. Concept
9. Development
10. Sampling
11. Production
12. Availability
### EZ-BLE™ Creator Modules CYBLE-x220xx-0x

**Space-Optimized Bluetooth Low-Energy (BLE) Modules**

**Applications**
- Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

**Features**
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, KC\(^2\), MIC\(^3\), and ISED\(^4\)
- **Small Footprint**
  - 10 mm x 10 mm x 1.8 mm, 21/22-pad SMT with 16 GPIOs
- **Bluetooth Smart Connectivity with BLE 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
- **1.3-µA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes**
- **Highly Integrated Solution**
  - Two crystals, chip antenna, passives, shield
  - 128KB and 256KB flash sizes
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-x220xx-EVAL Evaluation Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense®, buttons, GPIOs, over-the-air (OTA)

**Availability**
- **Sampling (4.1/128KB, 4.1/256KB, 4.2):** Now
- **Production (4.1/128KB, 4.1/256KB, 4.2):** Now

### EZ-BLE Creator Module Family: CYBLE-x220xx-0x

**EZ-BLE Creator Module**
- 32.768-kHz Crystal
- 24-MHz Crystal
- Chip Antenna

**Collateral**

**Datasheets**
- CYBLE-022001-00 Datasheet
- CYBLE-222005-00 Datasheet
- CYBLE-222014-01 (BT 4.2) Datasheet
- BLE Silicon Datasheet

**App Notes/Evaluation Kit User Guides**
- *Getting Started With EZ-BLE™ Module* (AN96841)
- PSoC Creator
- PSoC Programmer
- CySmart\(^7\) Windows Host Emulation Tool
- CySmart iOS and Android Apps

---

1 Bluetooth Special Interest Group Qualification Design ID
2 Korea certification
3 Ministry of Internal Affairs and Communications (Japan)
4 Innovation, Science and Economic Development Canada
5 Serial wire debug communication protocol
6 VREF only available on 256KB module
7 A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

---

5 Cypress Roadmap: Modules – SHNG
**EZ-BLE Creator Modules CYBLE-x140xx-0x**

**BLE Modules Designed to Maximize System Integration with Integrated Analog Functionality**

### Applications

- Sports and fitness monitors, medical devices, wearable electronics, home automation solutions, and game controllers

### Features

- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, KC\(^2\), MIC\(^3\), and ISED\(^4\)
- **Small Footprint**
  - 11 mm x 11 mm x 1.8 mm, 32-SMT, 25 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
- **Highly Integrated Solution**
  - Two crystals, trace antenna, passives, shield
  - 128KB and 256KB flash sizes, with over-the-air (OTA) firmware upgrades
  - Preprogrammed with EZ-Serial firmware
- **Programmable Analog Blocks**
  - Four opamps and one 12-bit, 1-Msps SAR\(^5\) ADC
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable TCPWM\(^6\) blocks: 16-bit timer, counter, or PWM
  - Two configurable serial communication blocks for i²C/SPI/UART
- **1.3-μA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes**
- **CYBLE-x140xx-EVAL Kit for Fast Evaluation and Development**

### Availability

- **Sampling (4.1/128KB, 4.1/256KB, 4.2):** Now
- **Production (4.1/128KB, 4.1/256KB, 4.2):** Now

### Collateral

- **Datasheets**
  - CYBLE-014008-00 Datasheet
  - CYBLE-214009-00 Datasheet
  - CYBLE-214015-01 (BT 4.2) Datasheet
  - BLE Silicon Datasheet

- **App Notes/Evaluation Kit User Guides**
  - Getting Started With EZ-BLE™ Module (AN96841)

- **Tools**
  - PSoC Creator
  - PSoC Programmer
  - CySmart® Windows Host Emulation Tool
  - CySmart iOS and Android Apps

---

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Korea Certification
\(^3\) Ministry of Internal Affairs and Communications (Japan)
\(^4\) Innovation, Science and Economic Development Canada
\(^5\) Successive approximation register
\(^6\) Timer/counter/pulse-width modulator
\(^7\) Serial wire debug communication protocol
\(^8\) A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE Creator Modules CYBLE-x120xx-xx
Cost-Optimized Bluetooth Low-Energy (BLE) Modules

Applications
Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features
• Qualification and Certification
  - Bluetooth SIG QDID\(^1\) (CYBLE-012011-00/CYBLE-212019-00), FCC, CE, KC\(^2\), MIC\(^3\), and ISED\(^4\)
• Small Footprint
  - 14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 23 GPIO
• Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
• Power Modes
  - 1.3-\(\mu\)A Deep Sleep, 150-nA Hibernate, and 60-nA Stop
• Highly Integrated Solution
  - Two crystals, trace antenna, passives, shield\(^5\)
  - Preprogrammed with EZ-Serial firmware
• CYBLE-x120xx-EVAL Adapter Board Interface
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

Availability
Sampling (4.1/128KB, 4.1/256KB, 4.2): Now
Production (4.1/128KB, 4.1/256KB, 4.2): Now

Collateral
Datasheets
CYBLE-012011-00 Datasheet
CYBLE-212019-00 Datasheet
CYBLE-212020-01 (BT 4.2) Datasheet
BLE Silicon Datasheet
App Notes/Evaluation Kit User Guides
Getting Started With EZ-BLE™ Module (AN96841)
PSoC Creator
PSoC Programmer
CySmart® Windows Host Emulation Tool
CySmart iOS and Android Apps

1 Bluetooth Special Interest Group Qualification Design ID
2 Korea Certification
3 Ministry of Internal Affairs and Communications (Japan)
4 Innovation, Science and Economic Development Canada
5 CYBLE-012012-10 does not include metal shield
6 Serial wire debug communication protocol
7 A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications

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\(\text{Cypress Roadmap: Modules – SHNG}\)
EZ-BLE Creator XR\(^1\) Modules CYBLE-2x20xx-x1
Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna

**Applications**
BLE connectivity, lighting, industrial, and medical

**Features**

- **Qualification and Certification**
  - Bluetooth SIG QDID\(^2\), FCC, CE, MIC\(^3\), KC\(^4\), and ISED\(^5\)
- **Small Footprint**
  - 15.0 mm x 23.0 mm x 2.0 mm, 30-pad SMT with 19 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.2**
  - 2.4-GHz BLE radio and baseband
- **Industrial Temperature Range**
  - Operating temperature range from -40°C to +85°C
- **Long Range**
  - +7.5-dBm Tx output power, 400 meters line-of-sight range
  - -93-dBm Rx sensitivity
- **Highly Integrated Solution**
  - Two crystals, trace antenna (optional), power amplifier, passives
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-2x20xx-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

**Availability**
Sampling: Now  
Production: Now

---

1. Extended range
2. Bluetooth Special Interest Group Qualification Design ID  
3. Ministry of Internal Affairs and Communications (Japan)
4. Korea Certification
5. Innovation, Science and Economic Development Canada
6. Serial wire debug communication protocol
7. A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE Creator XT/XR1 Modules CYBLE-22411x-0x
Long-Range Bluetooth Low-Energy (BLE) Modules Supporting Extended Temperatures

**Applications**
Connectivity, lighting, industrial, and medical

**Features**

- **Qualification and Certification**
  - Bluetooth SIG QDID, FCC, CE, MIC, KC, and ISED

- **Small Footprint**
  - 9.5 mm x 15.4 mm x 1.8 mm, 32-pad SMT with 25 GPIOs

- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband

- **Extended Industrial Temperature Range**
  - Operating temperature range from -40°C to +105°C

- **Long Range**
  - +9.5-dBm Tx output power, 400 meters line-of-sight range
  - -95-dBm Rx sensitivity

- **Highly Integrated Solution**
  - Two crystals, trace antenna, power amplifier, passives, shield
  - Preprogrammed with EZ-Serial firmware

- **CYBLE-22411x-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

**Availability**

- Sampling (4.1/128KB, 4.2/256KB): Now
- Production (4.1/128KB, 4.2/256KB): Now

**Collateral**

- **Datasheet**
  - CYBLE-224110-00 Datasheet
  - BLE Silicon Datasheet
  - CYBLE-224116-01 (BT 4.2) Datasheet

- **App Notes/Evaluation Kit User Guides**
  - Getting Started With EZ-BLE™ Module (AN96841)
  - PSoC Creator
  - PSoC Programmer
  - CySmart™ Windows Host Emulation Tool
  - CySmart iOS and Android Apps

1 Extended temperature/extended range
2 Bluetooth Special Interest Group Qualification Design ID
3 Ministry of Internal Affairs and Communications (Japan)
4 Korea Certification
5 Innovation, Science and Economic Development Canada
6 Serial wire debug communication protocol
7 A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE Creator Modules CYBLE-416045-02
Ultra-Low-Power Bluetooth Low-Energy (BLE) Module

Applications
BLE connectivity, lighting, industrial, and medical

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 14.0 mm x 18.5 mm x 2.0 mm, 43-pad SMT with 36 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 5.0**
  - 2.4-GHz BLE radio and baseband
  - +4.0-dBm Tx output power, -95-dBm Rx sensitivity
- **Industrial Temperature Range**
  - Operating temperature range from -40°C to +85°C
- **Power Modes**
  - 5.7-mA TX (0 dBm) and 6.7-mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
  - Deep Sleep mode current with 64K SRAM retention is 7 µA with 3.3-V external supply and internal buck
  - On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 µA quiescent current
- **Highly Integrated Solution**
  - One crystal, trace antenna, passives

Availability
- **Sampling:** Now
- **Production:** Now

EZ-BLE Creator Module Family: CYBLE-416045-02

Datasheets
- CYBLE-416045-02 Datasheet
- BLE Silicon, PSoC 6 MCU: PSoC 63 with BLE Datasheet

App Notes/Evaluation Kit User Guides
- Getting Started With EZ-BLE™ Module (AN96841)
- PSoC Creator
- PSoC Programmer
- CySmart® Windows Host Emulation Tool
- CySmart iOS and Android Apps

Collateral

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada
4 Serial wire debug communication protocol
5 A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE WICED Modules CYBLE-0130xx-00
Cost-Optimized Bluetooth Low-Energy (BLE) WICED Modules

Applications
Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features

- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 16/18 GPIO
- Bluetooth Smart Connectivity with Bluetooth 4.1
  - 2.4-GHz BLE radio and baseband
  - -93-dBm Rx sensitivity, +4-dBm Tx output power
- Highly Integrated Solution
  - One crystal, 128KB flash (CYBLE-013025-00), PCB antenna, shield
  - Simultaneous multiple Master and Slave (1M, 3S)
  - Security engine
  - Secure over-the-air (OTA) firmware upgrade (CYBLE-013025-00)
  - Preprogrammed with EZ-Serial firmware
- CYBLE-013025-EVAL Arduino Evaluation Board

Availability
Sampling: Now
Production: Now

Collateral

Datasheets
CYBLE-0130xx-00 Datasheet
Evaluation Kit User Guide
CYBLE-013025-EVAL Evaluation Board
WICED SMART SDK (Software)
WICED SMART SDK 2.x (Quick Start Guide)

Notes:
\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
**EZ-BT WICED Module CYBT-343026-01**  
Cost-Optimized Bluetooth Smart Ready WICED Modules

### Applications

Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

### Features

- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power  
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna  
  - Two-wire Global Coexistence Interface (GCI)  
  - PCM/IFS audio interface with wideband speech support  
  - Simultaneous multiple Master and Slave  
  - Secure over-the-air (OTA) firmware upgrade  
  - Preprogrammed with EZ-Serial firmware

### Availability

**Sampling:** Now  
**Production:** Now

---

\(^1\) Bluetooth Special Interest Group Qualification Design ID  
\(^2\) Ministry of Internal Affairs and Communications (Japan)  
\(^3\) Innovation, Science and Economic Development Canada

**EZ-BT WICED Module Family: CYBT-343026-01**

**EZ-BT WICED Module**

- **Power/Ground**
  - 4
- **XRES**
  - 4
- **24-MHz Crystal**
- **Serial flash**
  - 512 KB
- **Filter / Antenna**

**Collateral**

- **Datasheets**
  - CYBT-343026-01 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-343026-EVAL Evaluation Board  
  - WICED Studio
**EZ-BT WICED Module CYBT-3330xx-02**

**Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna**

### Applications
- Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

### Features

**Qualification and Certification**
- Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)

**Small Footprint**
- 12.0 mm \(\times\) 15.5 mm \(\times\) 1.95 mm, 24-pad SMT with 11 GPIOs

**Bluetooth Smart Ready with Bluetooth 5.0**
- BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
- BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power

**Bluetooth SIG Mesh Supported**

**Highly Integrated Solution**
- One crystal, 512KB flash, PCB antenna
- Two-wire Global Coexistence Interface (GCI)
- PCM/I2S audio interface with wideband speech support
- Secure over-the-air (OTA) firmware upgrade
- Preprogrammed with EZ-Serial firmware

### Availability
- **Sampling:** Now
- **Production:** Now

---

1. Bluetooth Special Interest Group Qualification Design ID
2. Ministry of Internal Affairs and Communications (Japan)
3. Innovation, Science and Economic Development Canada

**Collateral**

- **Datasheets**
  - [CYBT-333032-01 Datasheet](#)
  - [CYBT-333047-01 Datasheet](#)

- **Evaluation Kit User Guide**
  - [CYBT-343047-EVAL Evaluation Board](#)
  - [WICED Studio](#)
**EZ-BT WICED Module CYBT-343151-02**

Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting Extended Temperatures

### Applications
- Connectivity, lighting, industrial, and medical

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
  - Drop-in compatible with CYBT-343026-01
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Extended Industrial Temperature Range**
  - Operating temperature range from -30°C to +105°C
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/PS audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

### Availability
- **Sampling:** Now
- **Production:** Now

---

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada

---

**Collateral**

**Datasheets**
- CYBT-343151-02 Datasheet

**Evaluation Kit User Guide**
- CYBT-343026-EVAL Evaluation Board
- WICED Studio
EZ-BT WICED Module CYBT-353027-02
Size-Optimized Bluetooth 5.0 WICED Module

Applications
Bluetooth speaker, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 9 mm x 9 mm x 1.75 mm, 19-pad SMT with 8 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/IFS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability
- **Sampling:** Now
- **Production:** Now

Datasheets
- CYBT-353027-02 Datasheet
- CYBT-353027-EVAL Board
- WICED Studio

Collateral

1. Bluetooth Special Interest Group Qualification Design ID
2. Ministry of Internal Affairs and Communications (Japan)
3. Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-4230xx-02
Ultra-Low-Power Size-Optimized Bluetooth 5.0 WICED Module

Applications
Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 11 mm x 11 mm x 1.70 mm, 28-pad SMT with 17 GPIOs
- Bluetooth Smart Ready with Bluetooth 5.0
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- Bluetooth SIG Mesh Supported
- Highly Integrated Solution
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/IFS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2019)

Availability
Sampling: Now
Production: Now

Collateral
Datasheets
CYBT-4230xx-02 Datasheet
Evaluation Kit User Guide
CYBT-423028-EVAL Board
WICED Studio

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\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-4130xx-02
Ultra-Low-Power Cost-Optimized Bluetooth 5.0 WICED Module

**Applications**
Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

**Features**
- **Qualification and Certification**
  - Bluetooth SIG QDID, FCC, CE, MIC, and ISED
- **Small Footprint**
  - 12 mm x 16.3 mm x 1.70 mm, 30-pad SMT with 17 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 1MB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/IF audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2019)

**Availability**
Sampling: Now
Production: Now

---

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada

---

Collateral
Datasheets
CYBT-4130xx-02 Datasheet
Evaluation Kit User Guide
CYBT-413034-EVAL Board
WICED Studio
EZ-BT WICED Module CYBT-213043-02
Ultra-Low-Power Cost-Optimized Bluetooth 5.0 WICED Module

Applications
- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12 mm x 16.61 mm x 1.70 mm, 35-pad SMT with 22 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 256KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/FS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2019)

Availability
- **Sampling:** Now
- **Production:** Q1 2020

Collateral
- **Datasheets**
  - CYBT-213043-02 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-213043-MESH Kit
  - WICED Studio

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada

Sampling: Now
Production: Q1 2020
EZ-BT WICED Module CYBT-4830xx-02
Ultra-Long Range Bluetooth 5.0 WICED Module

Applications
- Bluetooth audio, mesh, sensor hubs, and industrial

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 12.75 mm x 18.59 mm x 1.8 mm, 34-pad SMT with 15 GPIOs
- Bluetooth Smart Ready with Bluetooth 5.0
  - BLE Tx output power up to 20 dBm for U.S. (FCC)
- Bluetooth SIG Mesh Supported
- Highly Integrated Solution
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/PS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2019)

Availability
- Sampling: Now
- Production: Now

Collateral
- Datasheets
  CYBT-4830xx-02 Datasheet
- Evaluation Kit User Guide
  CYBT-483039-EVAL Board
  WICED Studio

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-343052-02
Long Range Low Power Bluetooth 5.0 WICED Modules

Applications
- Remoter, Keyboard, Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 13.31 mm x 22.4 mm x 1.95 mm, 42-pad SMT with 24 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR: -91.5-dBm Rx sensitivity, +1-dBm Tx output power
  - BLE: -94.5-dBm Rx Sensitivity, +12-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - 1x Microphone interface
  - Programmable key-scan matrix interface, up to 8 × 20 key scanning matrix
  - 6x 16-bit PWMs
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade

Availability
- **Sampling**: Now
- **Production**: Q1 2020

Collateral
- **Datasheets**
  - CYBT-343052-01 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-343052-EVAL Evaluation Board
  - WICED Studio

---
\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-243053-02
Ultra-Low-Power Cost-Optimized Long Range Bluetooth 5.0 WICED Module

Applications
- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12 mm x 16.61 mm x 1.70 mm, 35-pad SMT with 22 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - -94.5-dBm Rx sensitivity, 10.5-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 256KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/IFS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2019)

Availability
- **Sampling:** Now
- **Production:** Q1 2020

Collateral
- **Datasheets**
  - CYBT-243053-02 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-243053-EVAL Evaluation Board
  - WICED Studio

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BLE/EZ-BT Module Product Selector Guide

EZ-BLE Module Part Numbering Decoder

<table>
<thead>
<tr>
<th>CY</th>
<th>BT</th>
<th>-</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>N</th>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

- **Bluetooth Version:**
  - 0 = Bluetooth 4.1
  - 1 = Bluetooth 4.2
  - 2 = Bluetooth 5.0

- **Integration Type:**
  - 0 = Full Integration with Shield
  - 1 = No Shield

- **Device Identification #:** Unique sequential product number for each module

- **Temperature Range:**
  - 0 = Industrial
  - 1 = Extended Industrial

- **EZ-BT Module Type:**
  - 2/4 = PSoC 4 Module
  - 3 = WICED Module
  - 6 = PSoC 6 Module

- **Antenna Type:**
  - 0 = No Antenna, Standard Range
  - 1 = PCB Antenna, Standard Range
  - 2 = Chip Antenna, Standard Range
  - 3 = No Antenna, Long Range (internal PA)
  - 4 = PCB Antenna, Long Range (internal PA)
  - 5 = Chip Antenna, Long Range (internal PA)
  - 6 = No Antenna, Long Range (external PA/LNA)
  - 7 = PCB Antenna, Long Range (external PA/LNA)
  - 8 = Chip Antenna, Long Range (external PA/LNA)

- **Flash Size:**
  - 0 = 128KB
  - 2 = 256KB
  - 3 = 512KB
  - 4 = 1024KB

- **Marketing Code:**
  - BLE = BLE Only Product
  - BT = Dual-Mode BT/LE Product

- **Company ID:**
  - CY = Cypress
MCU Portfolio Roadmap
MCU Portfolio

<table>
<thead>
<tr>
<th>8-Bit</th>
<th>32-Bit Arm® Cortex®-M0/M0+</th>
<th>32-Bit Arm Cortex-M3</th>
<th>32-Bit Arm Cortex-M4/M33(next generation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Analog Integration</td>
<td>8-/16-Bit Replacement</td>
<td>Mid-Range Performance</td>
<td>Ultra-Low-Power High Performance</td>
</tr>
</tbody>
</table>

**PSoC** is a brand of Cypress MCUs for the broad-based embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing.

**FM** is a portfolio of high-performance Arm Cortex-M-based MCUs for industrial and consumer applications.

---

1. A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters.

2. A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic.

---

**PSoC 1**
- M8C CPU
- 24 MHz, 32KB Flash
- 16 PAB, 16 PDB, 64 I/Os

**PSoC 3**
- 8051 CPU
- 67 MHz, 64KB Flash
- Up to 19 PAB, 30 PDB, 72 I/Os

**FM0+ MCUs**
- Cortex®-M0+
- 40 MHz, 512KB Flash, 102 I/Os

**PSoC 4**
- Cortex®-M0/M0+
- 48 MHz, 256KB Flash
- Up to 13 PAB, 20 PDB, 98 I/Os

**FM3 MCUs**
- Cortex-M3
- 144 MHz, 1.5MB Flash, 154 I/Os

**PSoC 5LP**
- Cortex-M3
- 80 MHz, 256KB Flash
- 20 PAB, 30 PDB, 72 I/Os

**PSoC 6**
- 150 MHz Cortex-M4/100 MHz M0+
- up to 2MB Flash
- 7 PAB, 56 PDB, 104 I/Os

**FM4 MCUs**
- Cortex-M4
- 200 MHz, 2MB Flash, 190 I/Os

---

**Status**
- Concept
- Development
- Sampling
- Production

**Availability**
- Q0YQ
- Q0YQ
# PSoC 6 MCU Portfolio

**Ultra-Low-Power | Flexibility | Hardware-Based Security and Root of Trust**

## PSoC 61 Line
**Ultra-Low-Power and High-Performance MCU Series**

<table>
<thead>
<tr>
<th>Device</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C61x8</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C61x7</td>
<td>New</td>
<td>Q120</td>
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<tr>
<td>CY8C61x6</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C61x5</td>
<td>New</td>
<td>Q120</td>
</tr>
</tbody>
</table>

### Key Features
- Arm Cortex-M4
- 2MB/1MB
- DAC, QSPI, FS-USB, SDHC, DC-DC

## PSoC 62 Line
**Ultra-Low-Power, Dual-Core, and High-Performance MCU Series**

<table>
<thead>
<tr>
<th>Device</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C62x8</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C62x7</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C62x6</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C62x5</td>
<td>New</td>
<td>Q120</td>
</tr>
</tbody>
</table>

### Key Features
- Arm Cortex-M4 & Arm Cortex-M0+
- 1MB/512KB
- DAC, QSPI, FS-USB, SDHC, DC-DC

## PSoC 63 Line
**High-Integration Wired/Wireless Connectivity MCU Series**

<table>
<thead>
<tr>
<th>Device</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C63x7</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8C63x6</td>
<td>New</td>
<td>Q120</td>
</tr>
</tbody>
</table>

### Key Features
- Arm Cortex-M4 & Arm Cortex-M0+
- 1MB/288KB
- DAC, QSPI, UDB, BLE, DC-DC

## PSoC 64 Line
**Ultra-Low-Power, Dual-Core, “Just Works” Secure Host MCU Series**

<table>
<thead>
<tr>
<th>Device</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8B064x5</td>
<td>New</td>
<td>Q120</td>
</tr>
<tr>
<td>CY8B064x6</td>
<td>New</td>
<td>Q120</td>
</tr>
</tbody>
</table>

### Key Features
- Arm Cortex-M4 & Arm Cortex-M0+
- Secure Boot MCU
- CY Secure Bootloader

---

1. Flash KB/SRAM KB
2. Digital to analog converter
3. Quad-SPI
4. Full-Speed USB
5. Secure Digital Host Controller
6. Universal digital block – programmable logic
7. Mobile Industry Processor Interface
8. Controller Area Network

---

**Roadmap**

- Concept
- Development
- Sampling
- Production

**Status**

- Availability
- Status
<table>
<thead>
<tr>
<th>PSoC® 4 Portfolio (NDA)</th>
<th>Flexibility</th>
<th>CapSense®</th>
<th>Ease-of-Use</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PSoC MCU</strong></td>
<td><strong>Intelligent Analog</strong></td>
<td><strong>Programmable Digital</strong></td>
<td><strong>Analog Coprocessor</strong></td>
</tr>
<tr>
<td><strong>PSoC 4000</strong></td>
<td><strong>PSoC 4100</strong></td>
<td><strong>PSoC 4200</strong></td>
<td><strong>PSoC 4A00</strong></td>
</tr>
<tr>
<td>BL = BLE-Series</td>
<td>S = S-Series</td>
<td>M = M-Series</td>
<td>L = L-Series</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C4124-9</td>
<td>24-MHz M0, 32K/4K</td>
<td>CY8C4Axx Motor Control 48-MHz M0+, 256K/32K</td>
</tr>
<tr>
<td>CY8C4124-10</td>
<td>24-MHz M0, 64K/8K</td>
<td>CY8C4Axx Inductive Sensing 48-MHz M0+, 32K/4K</td>
</tr>
<tr>
<td>CY8C4124-11</td>
<td>24-MHz M0+, 128K/16K</td>
<td>CY8C4Axx Universal analog block 48-MHz M0, 128K/16K</td>
</tr>
<tr>
<td>CY8C4124-12</td>
<td>24-MHz M0+, 256K/32K</td>
<td>CY8C4Axx Controller area network 48-MHz M0, 256K/32K</td>
</tr>
<tr>
<td>CY8C4124-13</td>
<td>24-MHz M0+, 32K/4K</td>
<td>CY8C4Axx Multi-sense converter 48-MHz M0, 32K/4K</td>
</tr>
</tbody>
</table>

1 Flash KB/SRAM KB  4 Serial communication block  7 Bluetooth Low Energy
2 Comparator  5 Current-output DAC  8 Universal digital block  10 Universal analog block
3 Analog-to-digital converter  6 Embedded programmable digital logic in the I/O subsystem  9 Motor Control Accelerator

Cypress Roadmaps

27
# FM4® and FM0+® MCU Portfolio

**Arm® Cortex®-M4 and Arm Cortex-M0+**

<table>
<thead>
<tr>
<th>Ultra-Low-Power 8-Bit/16-Bit Replacement</th>
<th>High Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S6E2D-Series</strong>&lt;br&gt;160 MHz, 540 CoreMark®, 2.7–3.6 V&lt;br&gt;2M/36K₁, 612KB Video RAM&lt;br&gt;120/176 Pins</td>
<td><strong>S6E2C-Series</strong>&lt;br&gt;200 MHz, 675 CoreMark, 2.7–5.5 V&lt;br&gt;2M/256K, 144/176/216 Pins</td>
</tr>
<tr>
<td><strong>MB9BFx6xM/N/R-Series</strong>&lt;br&gt;160 MHz, 540 CoreMark, 2.7–5.5 V&lt;br&gt;1M/128K, 32KB Work Flash&lt;br&gt;80/100/120 Pins</td>
<td><strong>S6E2G-Series</strong>&lt;br&gt;180 MHz, 608 CoreMark, 2.7–5.5 V&lt;br&gt;1M/192K, 144/176 Pins</td>
</tr>
<tr>
<td><strong>S6E2H-Series</strong>&lt;br&gt;160 MHz, 540 CoreMark, 2.7–5.5 V&lt;br&gt;512K/64K, 32KB Work Flash&lt;br&gt;80/100/120 Pins</td>
<td></td>
</tr>
<tr>
<td><strong>MB9BFx6xK/L-Series</strong>&lt;br&gt;160 MHz, 540 CoreMark, 2.7–5.5 V&lt;br&gt;512K/64K, 32KB Work Flash&lt;br&gt;48/64 Pins</td>
<td></td>
</tr>
</tbody>
</table>

1. Flash KB/SRAM KB
2. Independent flash memory available to store data or additional firmware
3. Active power consumption

---

Flash KB/SRAM KB

## Status

- Concept
- Development
- Sampling
- QOY
- QOY

CPU Speed

- 40 MHz, 1.7–3.6 V<br>128K/16K, 26/32/48/64 Pins, 40 µA/MHz

- 40 MHz, 2.7–5.5 V<br>8K/8K, 32/48 Pins, 70 µA/MHz

---

1 Flash KB/SRAM KB
2 Independent flash memory available to store data or additional firmware
3 Active power consumption
<table>
<thead>
<tr>
<th>Flash KB/SRAM KB</th>
<th>Independent flash memory available to store data or additional firmware</th>
</tr>
</thead>
<tbody>
<tr>
<td>512K/32K, 80/100 Pins</td>
<td>MB9AF2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>512K/32K, 32KB Work Flash</td>
<td>MB9AFx2K/L-Series 512K/32K, 80/100 Pins</td>
</tr>
<tr>
<td>512K/64K, 32KB Work Flash</td>
<td>MB9AFx5xM/N/R-Series 40 MHz, 1.7–3.6 V</td>
</tr>
<tr>
<td>48/64/80/100 Pins</td>
<td>MB9AFx4xL/M/N-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>256K/32K, 64KB Work Flash</td>
<td>MB9AFx1xL/M/N-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64/80/100 Pins</td>
<td>MB9AFx3xK/L-Series 20 MHz, 1.8–5.5 V</td>
</tr>
<tr>
<td>128K/16K, 64/80/100 Pins</td>
<td>MB9AFxAxL/M/N-Series 20 MHz, 1.8–5.5 V</td>
</tr>
<tr>
<td>256K/32K, 64/80/100 Pins</td>
<td>MB9AFx1xK-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>128K/16K, 32KB Work Flash</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>48 Pins</td>
<td>MB9AFx1xK-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>128K/16K, 32KB Work Flash</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64/48/64 Pins</td>
<td>MB9AFx1xK-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64/48/64 Pins</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>128K/16K, 32KB Work Flash</td>
<td>MB9AFxAxL/M/N-Series 20 MHz, 1.8–5.5 V</td>
</tr>
<tr>
<td>64KB Work Flash</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64/48/64 Pins</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64KB Work Flash</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
<tr>
<td>64/48/64 Pins</td>
<td>MB9AFx2xK/L-Series 40 MHz, 2.7–5.5 V</td>
</tr>
</tbody>
</table>

1 Flash KB/SRAM KB
2 Independent flash memory available to store data or additional firmware

**Midrange Performance**

- **MB9BFx1S/T-Series**
  - 60 MHz, 2.7–5.5 V
  - 15M/192K, 64KB Work Flash
  - 144/176 Pins

- **MB9BFx1S/T-Series**
  - 144 MHz, 2.7–5.5 V
  - 1M/128K, 144/176 Pins

- **MB9BFx1N/R-Series**
  - 144 MHz, 2.7–5.5 V
  - 512K/64K, 32KB Work Flash
  - 100/120 Pins
# Cypress Roadmaps

## PSOC® 3 Portfolio

| 8051 CPU | CapSense® | DMA | LCD | RTC | TCPWM |

### Programmable Digital PSOC 3200
- Analog: ΔΣ ADC, 1x DAC, 2x CMP, 0.9% $V_{REF}$
- Interfaces: FF/I²C

### Intelligent Analog PSOC 3400
- Analog: ΔΣ ADC, 2x DAC, 4x CMP, 2x Opamps, 2x SC/CT PAB, 0.9% $V_{REF}$
- Interfaces: FF/I²C

### Performance Analog PSOC 3600
- Analog: ΔΣ ADC, 2x/4x DAC, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% $V_{REF}$
- Interfaces: USB, FF/I²C

### Precision Analog PSOC 3800
- Analog: ΔΣ ADC, 2x/4x DAC, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% $V_{REF}$
- Interfaces: USB, FF/I²C

---

### CPU Speed and Flash

<table>
<thead>
<tr>
<th>Model</th>
<th>CPU Speed</th>
<th>Flash</th>
<th>SRAM</th>
<th>EEP</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C3246</td>
<td>50 MHz</td>
<td>64K</td>
<td>2K</td>
<td>0</td>
<td>Production</td>
<td>QQYY</td>
</tr>
<tr>
<td>CY8C3245</td>
<td>50 MHz</td>
<td>32K</td>
<td>4K</td>
<td>2</td>
<td>Sampling</td>
<td>QQYY</td>
</tr>
<tr>
<td>CY8C3244</td>
<td>50 MHz</td>
<td>16K</td>
<td>2K</td>
<td>0.5</td>
<td>Development</td>
<td>Concept</td>
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<tr>
<td>CY8C3445</td>
<td>50 MHz</td>
<td>20x UDB</td>
<td>USB, 72-CSP</td>
<td></td>
<td></td>
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<tr>
<td>CY8C3446</td>
<td>50 MHz</td>
<td>12b ADC</td>
<td>24x UDB, USB, CAN</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>CY8C3447</td>
<td>50 MHz</td>
<td>12b ADC</td>
<td>24x UDB, USB, CAN</td>
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<tr>
<td>CY8C3448</td>
<td>50 MHz</td>
<td>12b ADC</td>
<td>24x UDB, USB, CAN</td>
<td></td>
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<td></td>
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<tr>
<td>CY8C3666</td>
<td>67 MHz</td>
<td>64K</td>
<td>8K</td>
<td>2K</td>
<td>Production</td>
<td>QQYY</td>
</tr>
<tr>
<td>CY8C3665</td>
<td>67 MHz</td>
<td>32K</td>
<td>4-8K</td>
<td>1K</td>
<td>Sampling</td>
<td>QQYY</td>
</tr>
<tr>
<td>CY8C3865</td>
<td>67 MHz</td>
<td>32K</td>
<td>4-8K</td>
<td>1K</td>
<td>Production</td>
<td>QQYY</td>
</tr>
</tbody>
</table>

**Legend:**
- 1: Delta-Sigma analog-to-digital converter
- 2: Digital-to-analog converter
- 3: Comparator
- 4: Fixed function
- 5: Switched capacitor/continuous time programmable analog block
- 6: Flash KB/SRAM KB/EEPROM KB
- 7: Digital filter block
- 8: Universal digital block
- 9: Controller area network
- 10: Chip-scale package

---

### Status
- Concept
- Development
- Sampling
- Production

### Availability
- QQYY
- QQYY

---

30 Cypress Roadmaps
<table>
<thead>
<tr>
<th>CY8C24x93</th>
<th>CY8C24x94</th>
<th>CY8C28xxx</th>
<th>CY8C27xxx</th>
<th>CY8C21x34</th>
<th>CY8C23x33</th>
<th>CY8C21x23</th>
<th>CY8C24x23</th>
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<tbody>
<tr>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
<td>CY8C29xxx</td>
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<tr>
<td>32K/2K</td>
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<td>32K/2K</td>
<td>32K/2K</td>
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<td>32K/2K</td>
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<tr>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
<td>64 GPIOs</td>
</tr>
<tr>
<td>2x CMP, 1x10-bit Incremental ADC</td>
<td>2x CMP, 1x14-bit SAR ADC, 6x SC/CT PAB</td>
<td>2x CMP, 1x10-bit SAR ADC, 6x SC/CT PAB</td>
<td>2x CMP, 1x14-bit SAR ADC, 6x SC/CT PAB</td>
<td>2x CMP, 1x10-bit Single-Slope ADC, 4x SC/CT PAB</td>
<td>1x 8-bit SAR ADC, 4x SC/CT PAB</td>
<td>4x PDB, 2x CMP</td>
<td>4x PDB, 2x CMP</td>
</tr>
</tbody>
</table>

- **Flash**: 32K/2K
- **General purpose input/output pins**: 2x, 4x
- **Programmable digital block**: 28 GPIOs
- **Intelligent Analog**: CapSense, 4x PDB, 2x CMP
- **Performance Analog**: CapSense, 8x PDB, 4x CMP
- **Comparator**: 1x10-bit
- **Delta-Sigma ADC**: 1x14-bit
- **Switched capacitor/continuous time programmable analog block**: 1x14-bit

1. Flash KB/SRAM KB
2. General purpose input/output pins
3. Programmable digital block
4. Comparator
5. Delta-Sigma ADC
6. Switched capacitor/continuous time programmable analog block
7. Successive approximation register ADC

<table>
<thead>
<tr>
<th>Flash</th>
<th>General purpose input/output pins</th>
<th>Programmable digital block</th>
<th>Status</th>
<th>Availability</th>
<th>Concept</th>
<th>Development</th>
<th>Sampling</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>Production</td>
<td>QQYY</td>
<td>Concept</td>
<td>Development</td>
<td>Sampling</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
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</table>
### 8FX® MCU Portfolio

#### 8-Bit RISC CPU

<table>
<thead>
<tr>
<th>CPU Speed and Flash</th>
<th>8-/16-Pin</th>
<th>20-Pin</th>
<th>24-Pin</th>
<th>32-Pin</th>
<th>48-/52-Pin</th>
<th>64-Pin</th>
<th>80-Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 MHz, 2.4–5.5 V</td>
<td>MB95570H</td>
<td>MB95560H</td>
<td>MB95650L</td>
<td>MB95630H</td>
<td>MB95690K</td>
<td>MB95810K</td>
<td>MB95610H</td>
</tr>
<tr>
<td>16 MHz, 2.4–5.5 V</td>
<td>16 MHz, 1.8–5.5 V</td>
<td>16 MHz, 2.4–5.5 V</td>
<td>16 MHz, 1.8–5.5 V</td>
<td>16 MHz, 2.8–5.5 V</td>
<td>16 MHz, 2.8–5.5 V</td>
<td>16 MHz, 2.8–5.5 V</td>
<td>16 MHz, 2.4–5.5 V</td>
</tr>
<tr>
<td>16 MHz, 1.8–5.5 V</td>
<td>16/0.5/4</td>
<td>32/1/4</td>
<td>32/1/4</td>
<td>32/1/4</td>
<td>56/2/4</td>
<td>56/2/4</td>
<td>32/1/4</td>
</tr>
</tbody>
</table>

### Notes

1. Flash KB/SRAM KB/work flash KB; work flash is independent flash memory available to store data or additional firmware.

### Status Availability

- **Concept**
- **Development**
- **Sampling**
- **Production**

*QQYY*
## CapSense® Portfolio

### CapSense Express™

<table>
<thead>
<tr>
<th>Controller</th>
<th>Buttons</th>
<th>LEDs</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8CMBR3106S</td>
<td>11</td>
<td>2</td>
<td>Proximity, Liquid Tolerance</td>
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<tr>
<td>CY8CMBR3108</td>
<td>8</td>
<td>4</td>
<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8CMBR3110</td>
<td>10</td>
<td>5</td>
<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8CMBR3112</td>
<td>2</td>
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<td>Proximity</td>
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<tr>
<td>CY8CMBR2044</td>
<td>4</td>
<td>4</td>
<td>SmartSense Auto-tuning</td>
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<tr>
<td>CY8CMBR3002</td>
<td>2</td>
<td>2</td>
<td>SmartSense EMCPlus</td>
</tr>
<tr>
<td>CY8CMBR3116</td>
<td>16</td>
<td>8</td>
<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8CMBR3110</td>
<td>10</td>
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<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8CMBR2110</td>
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<td>SmartSense Auto-tuning</td>
</tr>
<tr>
<td>CY8CMBR2010</td>
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<td>SmartSense Auto-tuning</td>
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<tr>
<td>CY8CMBR2011</td>
<td>10</td>
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<td>SmartSense Auto-tuning</td>
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<tr>
<td>CY8CMBR2016</td>
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</table>

### CapSense Plus™

<table>
<thead>
<tr>
<th>Controller</th>
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<th>LEDs</th>
<th>Features</th>
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<tbody>
<tr>
<td>CY8CMBR2016</td>
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<td>SmartSense Auto-tuning</td>
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<tr>
<td>CY8CMBR2110</td>
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<td>SmartSense Auto-tuning</td>
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<tr>
<td>CY8C20xx7</td>
<td>31</td>
<td></td>
<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8C20xx6A/S</td>
<td>33</td>
<td>6</td>
<td>16, 32KB Flash, 2KB SRAM</td>
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<tr>
<td>CY8C20xx6H</td>
<td>25</td>
<td>5</td>
<td>8, 16KB Flash</td>
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<tr>
<td>CY8C20xx6A/S</td>
<td>33</td>
<td>6</td>
<td>16, 32KB Flash, 2KB SRAM</td>
</tr>
<tr>
<td>CY8C20xx6H</td>
<td>24</td>
<td>4</td>
<td>8KB Flash</td>
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<tr>
<td>CY8C20xx36A</td>
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<tr>
<td>CY8C20xx34</td>
<td>25</td>
<td>6</td>
<td>8KB Flash</td>
</tr>
</tbody>
</table>

1. Standard products that are configured for target applications with a graphical user interface
2. Microcontroller-based products that can be freely programmed to implement additional functions
3. SmartSense Electromagnetic Compatible = SmartSense Auto-tuning + high noise immunity
PSoC® 4000S-Series
PSoC 4 MCU Entry Line

**Applications**
Consumer devices (wearable, mobile, personal care) and small home appliances (coffee machine, juicer)

**Features**
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - 32KB flash (maximum)
  - 4KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope ADC\(^1\)
  - Two low-power comparators (CMPs)
  - One CapSense® block that supports low-power operation and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) that are configurable as I\(^2\)C, SPI, or UART

- **Packages**
  - 25-ball WLCSP, 24-pin QFN, 32-pin QFN, 48-pin TQFP

- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os\(^2\)

**Collateral**
Datasheet: [PSoC 4000S](#)

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem

**Availability**
**Production:** Now

---

[Diagram showing PSoC 4 One-Chip Solution]
**PSoc® 4100S-Series**

**PSoc 4 MCU Base Line**

**Applications**

Home appliances (washing machine, dishwasher) and industrial applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB flash
  - 8KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - One 10-bit, 46.8-kmps single-slope ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART

- **Packages**
  - 35-ball WLCSP, 32-pin QFN, 40-pin QFN, 48-pin TQFP

- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os

**Collateral**

Datasheet: PSoC 4100S

---

1 A simple ADC used to measure slow-moving signals  
2 Embedded programmable digital logic in the I/O subsystem

---

**Availability**

**Production:** Now

---

**PSoc® 4 One-Chip Solution**

**MCU Subsystem**

- Arm Cortex®-M0+ 48 MHz
- Flash (16KB to 64KB)
- SRAM (4KB to 8KB)
- WCO
- Serial Wire Debug
- Advanced High-Performance Bus (AHB)

**Programmable Analog Blocks**

- Opamp x2
- SAR ADC
- CMP x2
- 7-bit IDAC x2
- Single-Slope ADC
- CapSense

**Programmable Digital Blocks**

- TCPWM x5
- SCB x3

**I/O Subsystem**

- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x4

---

35 Cypress Roadmaps
PSoC® 4100S Plus-Series
PSoC 4 MCU Base Line

Main control and user interface for home appliance, consumer, and industrial applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 128KB flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)
  - True random number generator (TRNG)

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I2C, SPI, or UART
  - Segment LCD

- **One Controller Area Network (CAN) Controller**

- **Packages**
  - 44-pin TQFP, 64-pin LQFP (0.5-mm and 0.8-mm pitch)

- **I/O Subsystem**
  - Up to 57 GPIOs, including 24 Smart I/Os

**Collateral**

Datasheet: PSoC 4100S Plus

---

1 Embedded programmable digital logic in the I/O subsystem
PSoc® 4100PS-Series
PSoc 4 MCU Base Line

Applications
Consumer products and industrial applications

Features

- 32-bit MCU Subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 32KB flash, 4KB SRAM, RTC capability with a watch crystal oscillator (WCO)

- Programmable Analog Blocks
  - One 12-bit/1-Mspss SAR ADC
  - One 10-bit/1.6-kspss single-slope ADC
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIAs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 13-bit voltage output digital-to-analog converters (VDACs)
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC

- Programmable Digital Blocks
  - Eight 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART

- Packages
  - 28-pin SSOP, 45-ball WLCSP, 48-pin QFN, 48-pin TQFP

- I/O Subsystem
  - Up to 38 GPIOs, including 8 Smart I/Os

Collateral

Datasheet: PSoC 4100PS

Availability

Production: Now

PSoc® 4 One-Chip Solution

Summary:

- MCU Subsystem
- Programmable Analog Blocks
- Programmable Digital Blocks
- I/O Subsystem

Notes:

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem
PSoc® 4200DS-Series
PSoc 4 MCU Programmable Line

Main system control with programmable communications, subsystem control with programmable digital functions, digital sensor hub, low-end field oriented control (FOC) motor control, CPLD SoC, and any other embedded control without ADC/DAC.

Features
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller
  - Up to 64KB flash, 8KB SRAM
- **Programmable Analog Blocks**
  - Two low-power comparators (CMPs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): customized digital functions for flexible designs
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - One Smart I/O1 supporting programmable digital logic in the I/O subsystem that works even in deep sleep mode
- **Packages**
  - 25-pin WLCSP, 28-pin SSOP, 24-pin QFN
- **I/O Subsystem**
  - Up to 25 GPIOs

Collateral
- Datasheet: PSoC 4200DS

Availability
- Production: Now

---

1 Embedded programmable digital logic in the I/O subsystem
PSoC® 4A00-Series
PSoC 4 Analog Coprocessor

Applications
Industrial sensors (photoelectric sensors, displacement sensors), instrumentation and measurement (photometers, pH meters), and consumer products (wearables, grooming products)

Features
- Programmable Analog Blocks
  - One universal analog block (UAB) configurable as a programmable analog filter, 14-bit Delta-Sigma ADC, or 13-bit voltage-output DAC (VDAC)
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIA), etc.
  - One 12-bit/1-Mspses SAR ADC
  - One 10-bit/11.6-kspses single-slope ADC
  - 38-channel analog multiplexer (AMUX)
  - One CapSense® block configurable as a capacitive-sensing controller, two 7-bit current-output DACs (IDACs), or two low-power CMPs
- Signal Processing Engine
  - 48-MHz Arm® Cortex®-M0+ with a DMA controller and watch crystal oscillator (WCO)
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) configurable as I²C, SPI, or UART
- Packages
  - 28-pin SSOP, 45-pin CSP, 48-pin QFN, 48-pin TQFP
- I/O Subsystem
  - Up to 38 GPIOs

Collateral
Datasheet: CY8C4Axx Datasheet

Availability
Production: Now

Notes:
1 A simple ADC used to measure slow-moving signals
PSoC® 4100BLE-Series
PSoC 4 MCU Base Line with BLE

Features

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM
- **Programmable Analog Front Ends (AFEs)**
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry’s No. 1 capacitive-sensing solution with one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability
- **Programmable Digital Logic**
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 56-pin QFN and 68-pin CSP
- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

Collateral

- **Datasheet**: PSoC 4 BLE (CY8C4XX7 BLE)

1 Bluetooth 4.2 is only available in the 256KB flash option device

PSoC® 4 BLE One-Chip Solution

Datasheet: PSoC 4 BLE (CY8C4XX7 BLE)
**Applications**
Sports and fitness monitors, wearable electronics, medical devices, home automation solutions, game controllers, and sensor-based low-power systems for the Internet of Things (IoT)

**Features**
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM
- **Programmable Analog Front Ends (AFEs)**
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry’s No. 1 capacitive-sensing solution including one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability
- **Programmable Digital Logic**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 56-pin QFN and 68-pin CSP
- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

**Availability**
- **Datasheet:** PSoC 4 BLE (CY8C4XX7 BLE)
- **Production:** Now

1 Bluetooth 4.2 is only available in the 256KB flash option device
**Applications**

User interface and host processor for home appliances, digital and analog sensor hubs, MCU and discrete analog replacement

**Features**

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 128KB flash and 16KB SRAM

- **CapSense® with SmartSense™ Auto-Tuning**
  - Cypress Capacitive Sigma-Delta™ (CSD) controller
  - CapSense supported on up to 55 pins

- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)

- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM ) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART

- **Packages**
  - 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN

**Datasheet**:

[PSoc 4 M-Series (CY8C4100)](https://www.cypress.com)
**PSoc® 4200M-Series**

**PSoc 4 MCU Programmable Line**

<table>
<thead>
<tr>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>User interface and host processor for home appliances, digital and analog sensor hubs, LED control and communication for lighting systems</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>32-bit MCU Subsystem</strong></td>
</tr>
<tr>
<td>- 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC</td>
</tr>
<tr>
<td>- Up to 128KB flash and 16KB SRAM</td>
</tr>
<tr>
<td><strong>CapSense® with SmartSense™ Auto-Tuning</strong></td>
</tr>
<tr>
<td>- One Cypress capacitive Sigma-Delta™ (CSD) controller</td>
</tr>
<tr>
<td>- CapSense supported on up to 55 pins</td>
</tr>
<tr>
<td><strong>Programmable Analog Blocks</strong></td>
</tr>
<tr>
<td>- Two comparators (CMPs)</td>
</tr>
<tr>
<td>- Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.</td>
</tr>
<tr>
<td>- One 12-bit/1-Msps SAR ADC</td>
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<tr>
<td>- Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)</td>
</tr>
<tr>
<td><strong>Programmable Digital Blocks</strong></td>
</tr>
<tr>
<td>- Four universal digital blocks (UDBs): custom digital peripherals</td>
</tr>
<tr>
<td>- Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks</td>
</tr>
<tr>
<td>- Four serial communication blocks (SCBs) configurable as I^2C master or slave, SPI master or slave, or UART</td>
</tr>
<tr>
<td><strong>Two Controller Area Network (CAN) Controllers</strong></td>
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<tr>
<td><strong>Packages</strong></td>
</tr>
<tr>
<td>- 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN</td>
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<table>
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<tr>
<th>Collateral</th>
</tr>
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<tbody>
<tr>
<td>Datasheet: PSoC 4 M-Series (CY8C4200)</td>
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</table>

**PSoc® 4 One-Chip Solution**

**MCU Subsystem**
- Arm® Cortex®-M0
- 48 MHz

**Programmable Analog Blocks**
- Opamp x4
- SAR ADC

**Programmable Digital Blocks**
- TCPWM x8
- SCB x4
- CAN x2
- RTC
- DMA

**I/O Subsystem**
- CAN x2
- Segment LCD Drive

**Availability**
- Production: Now

---

Cypress Roadmaps
PSoc® 4200L-Series
PSoc 4 MCU Programmable Line

Applications
User interface and host processor for home appliances, digital and analog sensor hub, MCU and discrete analog replacement, and LED control and communication for lighting systems

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 256KB flash and 32KB SRAM
  - Up to 98 GPIOs supporting analog and digital interfaces

- **CapSense® With SmartSense™ Auto-Tuning**
  - Two Cypress Capacitive Sigma-Delta™ (CSD) controllers

- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)

- **Programmable Digital Blocks**
  - Eight universal digital blocks (UDBs): custom digital peripherals
  - Eight configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I2C master or slave, SPI master or slave, or UART

- **Full-Speed USB 2.0 Controller and Transceiver**

- **Two Controller Area Network (CAN) Controllers**

- **Packages**
  - 48-pin TQFP, 64-pin TQFP, 68-pin QFN, and 124-pin VFBGA

Collateral

Datasheet: [PSoc 4 L-Series](#)

PSoc® 4 One-Chip Solution

**MCU Subsystem**

- Arm Cortex®-M0
- 48 MHz

**Programmable Analog Blocks**

- Opamp x4
- SAR ADC
- CSD x2
- 8-bit IDAC x2
- 7-bit IDAC x2

**Programmable Digital Blocks**

- UDB x4
- TCPWM x8
- SCB x4
- DMA
- Segment LCD Drive

**I/O Subsystem**

- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8

Availability

Production: Now
**PSoC® 63 Line with Bluetooth Low Energy (BLE)**

### Applications
- Wearables, portable medical, industrial IoT, and smart home

### Features

- **MCU Subsystem**
  - Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 1MB Flash, 288KB SRAM with a DMA controller

- **Analog Blocks**
  - Two opamps, two low-power comparators (CMPs), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block

- **Digital Blocks and Communication Interfaces**
  - Twelve universal digital blocks (UDBs): custom digital peripherals
  - Twenty-four 16-bit and eight 32-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Eight serial communication blocks (SCBs)², deep sleep SCB
  - I²S and PDM-PCM² converter, SMIF⁴

- **Bluetooth Smart Connectivity**
  - Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput

- **Security Features**
  - Advanced cryptographic coprocessor (Crypto), true random number generator
  - One-time programmable eFuse⁵ for secure key storage
  - Secure over-the-air (OTA) firmware update with read-while-write flash technology for firmware updates

- **I/O Subsystem**
  - Up to 78 GPIOs

- **Packages**
  - 104-M-WLCSP, 116-BGA, 124-BGA, 68-QFN

### Datasheet:
- PSoC 6 Product Page

### Availability

**Sampling:** Now  
**Production:** Now

---

1. Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM
2. Configurable as a UART, SPI or I²C interface
3. Digital microphone interface
4. Serial memory interface for execute-in-place, encrypted Quad-SPI
5. One-time programmable bits for secure key storage
6. Single-precision floating-point unit
**Applications**
IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

**Features**

- **MCU Subsystem**
  - Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA
- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 2 x 12-bit SAR ADC (1 Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block
- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)¹
  - 12 x serial communication blocks (SCBs)², deep-sleep SCB
  - 2 x I²S and PDM-PCM³ converter, SMIF⁴, 2 x CAN⁵
  - 2 x SDHC blocks
  - USB 2.0 (Host and Device)
- **Security Features**
  - Advanced cryptographic coprocessor (Crypto)
  - True random number generator
  - One-time programmable eFUSE⁶ for secure key storage
  - Secure over-the-air (OTA) firmware update with read-while-write Flash technology for firmware updates
- **I/O Subsystem**
  - Up to 104 GPIOs
- **Packages**: 124-BGA, 100-WLCSP, 128-TQFP, 80-TQFP, 80-WLCSP, 68-QFN, 64-TQFP, 49-WLCSP

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**Collateral**

Preliminary Datasheet: [PSoC 6 Product Page](#)

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**Availability**

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¹ Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
² Configurable as a UART, SPI, or PC interface
³ Digital microphone interface
⁴ Serial memory interface for execute-in-place, encrypted Quad-SPI
⁵ Controller Area Network
⁶ One-time programmable bits for secure key storage
⁷ Single-Precision Floating-Point Unit

---

**Diagram**

- **MCU Subsystem**
  - Arm Cortex-M4 with VP FPU
  - 150-MHz
  - 128 Kbyte I-Cache

- **Analog Blocks**
  - Opamp x2
  - CMP x2
  - 12-bit DAC
  - 12-bit SAR ADC x2
  - CapSense

- **Digital Blocks**
  - TCPWM x32
  - UDB x12

- **Communication Interfaces**
  - SDHC x2
  - SCB x13
  - CAN x2
  - PS x2
  - PDM-PCM
  - SMIF (Quad-SPI)
  - USB 2.0

- **Programmable Interconnect and Routing**
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x8
  - GPIO x12
  - GPIO x12

---

**IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators**

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**Cypress Roadmaps**

46
**PSoC® 61 Line**

**Applications**
- Wearables, portable medical, smart home, and general embedded control

**Features**
- **MCU Subsystem**
  - 120-MHz Arm® Cortex®-M4
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 512KB flash, 128KB SRAM with a DMA controller
- **Analog Blocks**
  - Two low-power comparators (CMPs), 12-bit SAR ADC (1-Msps)
- **Digital Blocks and Communication Interfaces**
  - Ten 16-bit and two 32-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs), deep sleep SCB
  - One Secure Digital High Capacity (SDHC), two controller area networks (CANs)
- **I/O Subsystem**
  - Up to 76 GPIOs
- **Packages**
  - 100-LQFP

**Collateral**
- Preliminary Datasheet: [PSoC 6 Community](#)

---

1 Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM  
2 Configurable as a UART, SPI or I²C interface  
3 Single-precision floating-point unit
PSoC® 64 Secure Boot MCU Line with BLE

Features

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9-V) and low-power (1.1-0V) operation mode
  - Up to 1MB Flash, 288KB SRAM with DMA
- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Advanced hardware cryptographic acceleration and TRNG
- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block
- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)1
  - 8 x serial communication blocks (SCBs)2, deep-sleep SCB
  - I2S and PDM-PCM3 converter, SMIF4
- **Bluetooth Smart Connectivity**
  - Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput
- **I/O Subsystem**: Up to 78 GPIOs

Collateral

- Preliminary Datasheet: PSoC 6 Product Page

Applications

- Wearables, portable medical, industrial IoT, and smart home

Availability

- Sampling: Q3 2019
- Production: Q4 2019

Notes:

1 Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2 Configurable as a UART, SPI, or PC interface
3 Digital microphone interface
4 Serial memory interface for execute-in-place, encrypted Quad-SPI
5 One-time programmable bits for secure key storage
6 Single-Precision Floating-Point Unit
**PSoC® 64 Secure Boot MCU Line**

### Applications
- IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

### Features
- **MCU Subsystem**
  - 150-MHz Arm Cortex®-M4 with ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA
- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
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- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)
  - 8 x serial communication blocks (SCBs), deep-sleep SCB
  - I²S and PDM-PCM³ converter, SMIF⁴
  - USB 2.0 (Host and Device)
- **I/O Subsystem**
  - Up to 104 GPIOs

### Collateral
- Preliminary Datasheet: [PSoC 6 Product Page](#)

---

1 Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2 Configurable as a UART, SPI, or PC interface
3 Digital microphone interface
4 Serial memory interface for execute-in-place, encrypted Quad-SPI
5 One-time programmable bits for secure key storage
6 Single-Precision Floating-Point Unit
PSoC® 64 Standard Secure MCU Line with BLE

Features

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9-V) and low-power (1.1-0V) operation mode
  - Up to 1MB Flash, 288KB SRAM with DMA
- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Cypress ‘Just Works’ trusted O/S integrated with AFR/others cloud tool-kits (TLS, PKCS11 and FOTA)
  - Advanced hardware cryptographic acceleration and TRNG
- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block
- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)1
  - 8 x serial communication blocks (SCBs)2, deep-sleep SCB
  - I2S and PDM-PCM3 converter, SMIF4
- **Bluetooth Smart Connectivity**
  - Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput
- **I/O Subsystem**
  - Up to 78 GPIOs

Collateral

- Preliminary Datasheet: PSoC 6 Product Page

Applications

- Wearables, portable medical, industrial IoT, and smart home

Availability (AWS Version)

- **Sampling:** Q1 2020
- **Production:** Q2 2020

Notes:

1. Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2. Configurable as a UART, SPI, or PC interface
3. Digital microphone interface
4. Serial memory interface for execute-in-place, encrypted Quad-SPI
5. One-time programmable bits for secure key storage
6. Single-Precision Floating-Point Unit
PSoC® 64 Standard Secure MCU Line

Applications
IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

Features

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA

- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Cypress ‘Just Works’ trusted O/S integrated with AWS/others cloud tool-kits (TLS, PKCS11 and FOTA)
  - Advanced hardware cryptographic acceleration and TRNG

- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Mspss)
  - 12-bit DAC, CapSense® capacitive-sensing block

- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)¹
  - 8 x serial communication blocks (SCBs)², deep-sleep SCB
  - I²S and PDM-PCM³ converter, SMIF⁴
  - USB 2.0 (Host and Device)

- **I/O Subsystem**: Up to 104 GPIOs

Collateral

- **Preliminary Datasheet**: [PSoC 6 Product Page](#)

Availability (AWS Version)

- **Sampling**: Q1 2020
- **Production**: Q2 2020

Notes:

1. Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2. Configurable as UART, SPI, or PC interface
3. Digital microphone interface
4. Serial memory interface for execute-in-place, encrypted Quad-SPI
5. One-time programmable bits for secure key storage
6. Single-Precision Floating-Point Unit
S6E1C-Series
FM0+ MCU Portfolio

Applications
Industrial, healthcare, sensor hubs, wearable electronics, and mobile, battery-powered devices

Features

- **Ultra-Low-Power MCU Subsystem**
  - Up to 40-MHz Arm® Cortex®-M0+ CPU, 40-µA/MHz active current with 1.65–3.6-V operating voltage
  - Low-power 1.2-µA RTC operating current
  - Up to 128KB flash and 16KB SRAM
  - Near-zero wait-state flash access at up to 40 MHz
  - Fast 540-µs startup from power-on reset and 40 µs from standby

- **Analog and Digital Subsystems**
  - Two base timers, dual timer, CRC, and watch counter
  - Six channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I^2^C, LIN, USB, and I^2^S
  - Two HDMI-CEC^1^ channels
  - Two Smart Card interface channels
  - 12-bit, 1-Msps ADC with a 24-channel multiplexer input

- **Packages**
  - 32-pin LQFP, 48-pin LQFP, 64-pin LQFP, 32-pin QFN, 48-pin QFN, 26-pin CSP (2.35-mm x 2.72-mm)

Collateral

- Datasheet: S6E1C1-Series, S6E1C3-Series

Availability

Production: Now

---

1. HDMI consumer electronics control signal
2. Low-voltage detect
3. Descriptor system transfer controller
4. Watchdog timer

---

S6E1C-Series

MCU Subsystem

- Arm® Cortex®-M0+ 40 MHz
- Flash (64KB to 128KB)
- SRAM (12KB to 16KB)
- LVD^2^
- DSTD^2^
- DSTC^3^
- Internal Main Oscillator
- Clock Supervisor
- Serial Wire Debug

Digital Subsystem

- Advanced High-Performance Bus (AHB)
- MFS x6
- USB (Host + Device)
- Base Timer x8
- Dual Timer
- RTC
- PS
- Watch Counter
- HDMI x2
- WDT^4^)
- Smart Card
- CRC

Analog Subsystem

- 12-bit ADC

I/O Subsystem

- GPIO x8
- GPIO x12
- GPIO x3
- GPIO x12
- GPIO x9
- GPIO x4
- GPIO x2
- GPIO x2

---
**Applications**

Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

**Features**

- **High-Performance MCU Subsystem**
  - 675 CoreMark®, 200-MHz Arm® Cortex®-M4 CPU, 365-μA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low-power 1.0-μA RTC operating current
  - Up to 2MB flash and 256KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications

- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, four quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Sixteen channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
  - Two USB interfaces, two controller area network (CAN), CAN with flexible data rate (CAN-FD), IEEE 1588 Ethernet¹, high-speed Quad-SPI (HS-QSPI), I²S, and external bus interfaces
  - Three 12-bit/2-Msp ADCs with a 32-channel multiplexer input
  - Two 12-bit DACs
  - Built-in Cryptographic Assist hardware coprocessor for encryption

- **Packages**
  - 144-pin LQFP, 176-pin LQFP, 216-pin LQFP, 192-pin BGA

**Collateral**

Datasheet: [S6E2C-Series](#)

---

*S6E2C-Series*

**FM4 MCU Portfolio**

**Datasheet:** S6E2CC-Series

**Production:** Now

---

1. Ethernet communications solution that supports the Precision Time Protocol (PTP) standard
2. Memory protection unit
3. Descriptor system transfer controller
Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

### Features

**High-Performance MCU Subsystem**
- 608 CoreMark® 180-MHz Arm® Cortex®-M4 CPU, 244-µA/MHz active current with 2.7–5.5-V operating voltage
- Up to 1MB flash and 192KB SRAM with 16KB flash accelerator
- Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications

**Analog and Digital Subsystems**
- Two multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, two quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
- Ten channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
- Two USB interfaces, controller area network (CAN), IEEE 1588 Ethernet\(^1\), I²S, two SD Card interfaces, and an external bus interface
- Three 12-bit/2-Msps ADCs with a 32-channel multiplexer input
- Built-in Cryptographic Assist hardware coprocessor for encryption

**Packages**
- 144-pin LQFP and 176-pin LQFP

### Collateral

**Datasheet:** [S6E2G-Series](#)

---

\(^1\) Ethernet communications solution that supports the Precision Time Protocol (PTP) standard

\(^2\) Memory protection unit

\(^3\) Descriptor system transfer controller

---

Cypress Roadmaps
S6E2H-Series
FM4 MCU Portfolio

Applications
Motor control, factory automation, industrial, IoT, DSLR lens MCU and home appliance

Features
- **High-Performance MCU Subsystem**
  - 540 CoreMark®, 160-MHz Arm® Cortex®-M4 CPU, 188-µA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low power 1.3-µA RTC operating current
  - Up to 512KB flash and 64KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications
- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), eight base timers, three quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Eight channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
  - Two controller area network (CAN), SD Card, and external bus interfaces
  - Three 12-bit/2-Msps ADCs with a 24-channel multiplexer input
  - Two 12-bit DACs
- **Packages**
  - 80-pin LQFP, 100-pin LQFP, 120-pin LQFP, 121-pin BGA

Collateral
Datasheet: [S6E2H-Series](#)

Availability
Production: Now

1 Memory protection unit
2 Descriptor system transfer controller
## MCU Development Kits

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<tr>
<th>Kit Number</th>
<th>Key Features</th>
<th>Price</th>
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<tbody>
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<td>CY8CKIT-049 or CY8CKIT-059</td>
<td>Ultra-low-cost prototyping Breadboard-compatible Serial wire debug (SWD) or bootloader for program/debug</td>
<td>$4–$10</td>
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<td>CY8CKIT-042-BLE</td>
<td>Arduino form factor compatible Access to all PSoC 4 BLE I/Os Full SWD program and debug</td>
<td>$49</td>
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<td>DEV-13229</td>
<td>Arduino form factor compatible Access to all PSoC 5LP I/Os Full SWD program and debug</td>
<td>$55</td>
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<td>Arduino form factor compatible Full SWD program and debug</td>
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<td>CY8CKIT-062-WIFI-BT</td>
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Learn more or buy a kit today at [www.cypress.com/kits](http://www.cypress.com/kits)
# MCU Packages

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USB Portfolio
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<td>32-Bit Bus to USB 3.1 Gen 1 ARM9, 512KB RAM</td>
<td>USB 3.1 Gen 1, Shared Link™</td>
<td>16-Bit Bus to USB 3.1 Gen 1</td>
<td>USB Type-C Port Controller</td>
<td>30V, PPS, QC4, 64KB Flash</td>
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</table>

**Notes:**
1. Simultaneous USB 2.0 and SuperSpeed traffic on the same port.
2. Battery Charging specification v1.2.
3. Enables USB charging without host connection.
4. Camera Serial Interface v2.0.
5. Redundant array of independent disks.
6. SD extended capacity.
7. Embedded Multimedia Card.
8. Status:
   - **Production**
   - **Sampling**
   - **Development**
9. **NEW**
10. **Q419**
11. **Q419**
12. **Q419**
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### EZ-PD ACG1F

**Single Port Type-C controller with BC1.2, Load Switch**

#### Applications

- Desktops, Notebooks

#### Features

- **Type-C 1.2 Controller**
- **V_{BUS} to CC/SBU short protection**
- **Integrated Analog Blocks**
  - Configurable V_{BUS} over-voltage protection and over-current protection
  - High-side current sense amplifier across 5mohms
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
  - VCONN FET per CC with VCONN OCP limit of up to 550 mA
- **Integrated Digital Blocks**
  - 4x GPIOs
  - One SCB for configurable master/slave I2C, SPI, or UART
- **Arm® Cortex®-M0 with MCU Subsystem and 16KB flash**
- **Power System**
  - Integrated 15-W provider load switch capable of 5 V, 3A
  - VBUS over-voltage protection and Reverse Current Protection on provider path
- **Packages**
  - 24-QFN (4x4 mm)

#### Collateral

- **Datasheet:** [ACG1F Datasheet](#)

#### Availability

- **Sampling:** Now
- **Production:** Q4 2019

---

**ACG1: Single-Chip USB-C Controller**

**MCU Subsystem**

- Arm Cortex-M0 48 MHz

**Integrated Digital Blocks**

- SCB (I2C, SPI, UART)

**I/O Subsystem**

- Programmable IO Matrix
- 4x GPIO Port

**System Resources**

- USB-C Subsystem
- CC-Detection
- VCONN FET
- V_{BUS} to CC Short Protection
- 1x 8-bit SAR ADC
- V_{BUS} OVP, RCP, SCP Protection
- Provider Load Switch 5 V, 3A

**USB Legacy (BC v1.2, QC3.0, AFC Apple Charging)**

**Datasheet:** [ACG1F Datasheet](#)
PAG1S
USB-C Power Delivery Secondary-Side Controller

Applications
USB PD chargers, power adapters

Features
- PPS/PD3.0/QC4.0 integrated flyback controller for mobile chargers
- Works with both primary side-controlled and secondary-side-controlled flyback designs
- Integrated secondary-side regulation, synchronous rectifier, and charging port controller offering a single-chip secondary-side controller
- Supports Quasi-Resonant (QR)/Critical Conduction (CrCM), valley switching, discontinuous conduction (DCM), and Burst Modes
- Integrated digital blocks
  - One timer/counter/pulse-width modulator (TCPWM) block, 6x GPIOs
- Integrated analog blocks
  - Configurable V_BUS overvoltage protection (OVP), overcurrent (OCP) protection, undervoltage protection (UVP), and short-circuit protection (SCP)
  - Integrated 2xV_BUS discharge FETs and a NFET gate driver to drive the load switch
  - Low-side current sense\(^1\) capable of detecting 100-mA change
  - One legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^2\))
- Low-Power Operation
  - High-voltage (3–30 V, 30-V maximum) V_BUS voltage inputs
  - No load power consumption of less than 20 mW
- Package
  - 24 QFN (16 mm\(^2\))

Collateral
Preliminary Datasheet: [PAG1S Datasheet](#)

Availability
Sampling: Now

---

\(^1\) Circuit to measure the current flowing on the V_BUS

\(^2\) Adaptive Fast Charging

\(^3\) Termination resistors: R_P read as a DFP, R_D as a UFP
PAG1P
USB-C Power Delivery Primary Start Up Controller

**Applications**
USB PD chargers, power adapters

**Features**
- Works across universal AC mains input 85 VAC to 265 VAC
- Operates with PWM inputs from a secondary-side controller
- Low-side gate driver to drive primary FET (1-A Source)
- Soft-start with duty-cycle clamping
- Integrates high-voltage start-up and shunt regulator
- Line undervoltage and overvoltage protection
- Overcurrent protection against load short-circuit
- Operates over a temperature range of -40 ºC to 105 ºC
- Package
  - 10-pin SOIC (4.9 x 3.9 mm²)

**Collateral**
Preliminary Datasheet: [PAG1S Datasheet](#)

**Availability**
- **Sampling:** Now
- **Production:** Q4 2019

---

**PAG1P: USB-C PD Primary Start Up Controller**
- Gate Driver
- Start-up power supply
- Low-Side Current Sense
- Soft-Start
- LDO
- Line UV/OV, OCP Protection
**EZ-USB HX3PD**

**USB 3.1 Gen 2 Type-C Hub with Power Delivery**

### Applications
- Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

### Features
- **USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD**
  - Upstream (US) ports:
    - 10 Gbps; Type-A or Type-C plus PD (UFP)
  - Downstream (DS) ports:
    - 7 ports: 5x 10 Gbps, 2x 480 Mbps
    - 3 Type-C ports: 1 PD port (DFP), 2 Type-C only
- **Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction**
  - Integrated termination resistors (R_P and R_D)^1
  - Integrated USB Billboard Controller^2, USB Type-C Bridge Controller
  - Integrated VCONN FETs and ADC for overvoltage and overcurrent protection
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- **Ghost Charge™**: Charging DS without US connection
- **Dock Management Controller** for secured firmware download
  - Firmware upgradable over USB
- **System-Level ESD on Configuration Channel (CC) Pins**: 8 kV Contact, 15 kV Air
- **Package**: 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

### Collateral
- **Datasheet**: [HX3PD Datasheet](#)
- **Kit**: [HX3PD Evaluation Kit](#)

### Availability
- **Samples**: Now
- **Production**: Q1 2020

---

^1 Termination resistors: R_P read as a DFP, R_D as a UFP

^2 A USB Device controller that is used to implement the USB Billboard Device Class

^3 Transaction Translator informs the USB Host of the supported Alternate Modes as well as any failures
EZ-PD BCR
USB Type-C Power-Sink Port Controller

Applications
Portable electronics – cameras, camcorders, smart speakers, toys, gaming, shavers, powered tools and any battery-powered devices.
Industrial – LED lighting, scanner, printer, drones, IoT
Any electronics device consuming less than 100W

Features
- Integrated Type-C and Power Delivery (PD) Transceiver
  - Integrated high-voltage 30-V–tolerant LDO to power the BCR controller
  - One serial communication blocks (SCB) for slave I2C
- Integrated Analog
  - \( V_{BUS} \) overvoltage (OVP) and undervoltage (UVP) protection
  - Fault detection for PDO mismatch
  - Slew rate-controlled PMOS FET gate driver
  - Minimum 25-V–tolerant CC pins and FET control pins
- Low-Power Operation
  - High-voltage (5–30 V, 30 V maximum) \( V_{BUS} \) voltage inputs
  - Sleep: \(~3.5\) mA; Deep Sleep: \(~50\) µA with wake-on-I2C or CC
- System-Level ESD on CC, and \( V_{BUS} \)
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- Package
  - 24-QFN (16 mm\(^2\)), supporting extended Industrial temp (-40 °C to 105 °C)

Collateral
Datasheet: CY3177 Datasheet
Evaluation Kit: CY4533 Kit
Product Brochure: EZ-PD Barrel Connector Replacement Product Overview

Availability
Production: Now

EZ-PD BCR: USB Type-C Power-Sink Port Controller

I/O Subsystem
- CC
- 1x SCB (I2C)
- Fault Detection

USB PD Subsystem
- Baseband MAC
- Baseband PHY
- 30-V Regulator
- Integrated Resistors \((R_D, R_{DB})\)
- OVP and UVP
- 1x 9-bit SAR ADC
- VBus-CC Short Protection
- VBus Discharge

1 Analog feedback voltage control circuit to control \( V_{BUS} \)
2 Circuit to measure the current flowing on the \( V_{BUS} \)
3 Termination resistors: \( R_D \) as a UFP, \( R_{DB} \) as a UFP supporting dead battery
## EZ-PD CCG6
### Single-Port USB Type-C Port Controller With PD

### Applications
- Thunderbolt / USB-C Notebook, Desktop PCs

### Features
- **USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode and USB platforms**
- **VBUS to CC/SBU short protection**
- **Integrated high-voltage 20V-regulator to power CCG6**
- **Integrated Analog Blocks**
  - 2x1 SBU analog mux, 2x2 USB analog mux
  - Configurable VBUS over-voltage protection and over-current protection
  - High-side current sense amplifier across 5 mΩ
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- **Integrated Digital Blocks**
  - Two timers, counters, and pulse-width modulators, 17x GPIOs
  - Four SCBs for configurable master/slave I2C, SPI, or UART
- **Arm® Cortex®-M0 with MCU Subsystem and 128KB flash**
- **Power System**
  - High-voltage (4 - 21.5 V, 26 V Max) VBUS voltage inputs
  - 2x VCONN FETs supporting up to 500 mA, Supports Dead Battery mode operation
  - Integrated PFET gate drivers and Slew Rate Control
  - VBUS over-voltage protection and Reverse Current Protection on provider path
- **Packages**
  - 40 QFN (6x6 mm)

### Collateral
- **Datasheet:** [CCG6 Datasheet](#)

### Availability
- **Production:** Now

---

1 Serial communication block configurable as UART, SPI or I²C

---

![Diagram of CCG6 Single-Port USB Type-C Port Controller With PD](#)

- **MCU Subsystem**
  - Cortex-M0 48 MHz
  - Flash (128KB)
  - SRAM (12KB)
  - Advanced High-Performance Bus (AHB)

- **Integrated Digital Blocks**
  - 2x TCPWM
  - SCB (I²C, SPI, UART)
  - SCB (I²C, SPI, UART)
  - SCB (I²C, SPI, UART)

- **I/O Subsystem**
  - Programmable IO Matrix
  - CC, VCONN, 17x GPIO Port

- **USB PD Subsystem**
  - Baseband MAC
  - Hi-Voltage PHY (21.5V)
  - System Resources
  - 1x SBU Analog Pass through / Mux
  - 2x USB Analog Switch
  - 1x 8-bit SAR ADC

- **Programmable I/O Matrix**
  - VBUS OVP, RCP, SCB Protection
  - 2x VCONN FETs
  - 2x PFETs Gate Driver with Slew rate control
**EZ-PD CCG6F**

Single-Port USB Type-C Port Controller With PD

**Applications**

Thunderbolt / USB-C Notebook, Desktop PCs

**Features**

- USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode, and USB platforms
- **V_{BUS}** to CC/SBU short protection
- Integrated high-voltage 20V-regulator to power CCG6
- **Integrated Analog Blocks**
  - 2x1 SBU analog mux, 2x2 USB analog mux
  - Configurable **V_{BUS}** over-voltage protection and over-current protection
  - High-side current sense amplifier across 5 mΩ
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- **Integrated Digital Blocks**
  - Two timers, counters, and pulse-width modulators, 17x GPIOs
  - Four SCBs\(^1\) for configurable master/slave I2C, SPI, or UART
- **Arm® Cortex®-M0** with MCU Subsystem and 128KB flash
- **Power System**
  - High-voltage (4 - 21.5 V, 26 V Max) **V_{BUS}** voltage inputs
  - 2x **V_{CONN}** FETs supporting up to 500 mA, Supports Dead Battery mode operation
  - Integrated PFETs for provider path
  - **VBUS** over-voltage protection and Reverse Current Protection on provider path
- **Packages**
  - 96 BGA (6x6 mm)

**Collateral**

Datasheet: [CCG6F Datasheet](#)

\(^1\) Serial communication block configurable as UART, SPI or PCI

**Availability**

Production: Now
EZ-PD CMG1
USB Type-C Passive EMCA Controller

Features

- USB-C PD Controller, PD 3.0 Transceiver
- \( V_{BUS} \)-to-CC Short Protection
- \( V_{BUS} \)-to-\( V_{CONN} \) Short Protection
- Power from \( V_{CONN} \) range 3.0 to 5.5-V
- Termination Resistor \( R_A \)
- Supports \( R_A \) Weakening to Reduce Power Consumption
- Configurable 32-byte Storage for Configuration Over Type-C Interface
- Integrated oscillator eliminating the need for external clock
- Power Operation
  - 2.7-V to 5.5-V operation (\( V_{CONN} \) pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, \( V_{CONN} \) Pins
  - ±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm²)
  - Supports industrial temperature range (-40°C to +85°C)

Collateral

Preliminary Datasheet: [CMG1 Datasheet](#)

Availability

Production: Now

CMG1: USB Type-C Passive EMCA Controller

USB PD Subsystem
- \( V_{BUS} \)-to-CC Short Protection
- \( V_{BUS} \)-to-\( V_{CONN} \) Short Protection, \( R_A \)
- \( V_{BUS} \)-to-\( V_{CONN} \) Short Protection, \( R_A \)
- USB PD & Type-C PHY
- EMCA Protocol Engine

Storage
- 32-Byte Storage for Configuration

System Resources
- Oscillator
- Reset
- VREF
- IREF

Product Overview
# EZ-PD CCG3PA2
## USB Type-C and PD Port Controller

### Applications
- Power adapters, chargers, power banks

### Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable V_BUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier\(^1\) with analog out for V_BUS control
  - Low side current sense\(^2\) capable of detecting 100-mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^3\))
- **32-bit Arm® Cortex®-M0 CPU with 128KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_BUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 μA with wake-on-I²C or CC
- **System-Level ESD on CC / V_CONN, V_BUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm\(^2\)), 30-ball CSP (7.5 mm\(^2\))

### Collateral
- Datasheet: [Contact Sales](#)

### Availability
- **Production:** Now

---

\(^1\) Analog feedback voltage control circuit to control V_BUS
\(^2\) Circuit to measure the current flowing on the V_BUS
\(^3\) Adaptive Fast Charging
\(^4\) Termination resistors: R_P as a DFP, R_D as a UFP, R_A as an EMCA

---

## CCG3PA2: USB Type-C Port Controller

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<th>Integrated Digital Blocks</th>
<th>I/O Subsystem</th>
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<td>4x TCPWM</td>
<td>1x 9-bit SAR ADC</td>
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<td><strong>Flash</strong> (128KB)</td>
<td>2x SCB (I²C, SPI, UART)</td>
<td><strong>CC</strong></td>
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<td><strong>SRAM</strong> (8KB)</td>
<td>2x V_CONN FETs</td>
<td><strong>Baseband PHY</strong></td>
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<td><strong>Advanced High-Performance Bus (AHB)</strong></td>
<td>OCP and OVP</td>
<td><strong>30-V Regulator</strong></td>
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<tr>
<td><strong>System Resources</strong></td>
<td><strong>Error Amplifier</strong></td>
<td><strong>2x V_CONN FETs</strong></td>
</tr>
</tbody>
</table>

- **Baseband MAC**
- **Low-Side Current Sense**
- **Integrated Resistors (R_P, R_D, R_A)**

---

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EZ-PD CCG3PA
USB Type-C and PD Port Controller

**Applications**
- Power adapters, chargers, power banks

**Features**

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART

- **Integrated Analog**
  - Configurable V_BUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for V_BUS control
  - Low side current sense² capable of detecting 100-mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC v1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)

- **32-bit Arm® Cortex®-M0 CPU with 64KB Flash**

- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_BUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC

- **System-Level ESD on CC / V_CONN, V_BUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C

- **Packages**
  - 24-QFN (16 mm²), 16-SOIC (60 mm²)

**Availability**

- Production: Now

---

¹ Analog feedback voltage control circuit to control V_BUS
² Circuit to measure the current flowing on the V_BUS
³ Adaptive Fast Charging
⁴ Termination resistors: R_p as a DFP, R_d as a UFP, R_h as an EMCA

**Collateral**

- Datasheet: [CCG3PA Datasheet](#)

---

**CCG3PA: USB Type-C Port Controller**

**MCU Subsystem**
- Cortex®-M0
- 48 MHz

**Integrated Digital Blocks**
- 4x TCPWM
- 2x SCB (I²C, SPI, UART)

**I/O Subsystem**
- Programmable I/O Matrix
- CC

**USB PD Subsystem**
- Baseband MAC
- 2x V_CONN FETs
- 30-V Regulator
- OCP and OVP
- Low-Side Current Sense
- 2x Charge-Detect (BC v1.2, AC, QC, AFC)

**System Resources**
- Flash (64KB)
- SRAM (4KB)
- 1x 9-bit SAR ADC

**Integrated Resistors (R_p, R_d, R_h)**

**Error Amplifier**
- 1x 9-bit SAR ADC
**EZ-PD CCG5**

**Dual-Port USB Type-C and PD Port Controller**

### Features

- **Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports**
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI-compliant Interface with WHQL2-certified driver
  - Support for UEFI2 driver with Microsoft capsule firmware download
- **Integrated Analog**
  - Integrated high-voltage LDO and 4x \(V_{\text{CONN}}\) FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC4)
  - Integrated Type-C termination resistors (\(R_P\), \(R_D\), \(R_{DB}\))
  - 25-V tolerance on CC1/2 and SBU pins
- **Arm® Cortex®-M0 CPU with 128KB Flash and 12KB SRAM**
  - 4x serial communication blocks (SCB) - I²C, SPI or UART
  - Firmware upgradable over SWD/I²C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2μs response time; integrated \(V_{\text{BUS}}/V_{\text{CONN}}\) overcurrent protection (OCP)
- **System-Level ESD on CC/V_{\text{CONN}}, V_{\text{BUS}}, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Discharge IEC61000-4-2 Level 4C
- **Packages**
  - 2-Port in 96-BGA (6 mm²), 1-Port in 40-QFN (6 mm²)

### Collateral

**Datasheet:** [CCG5 Datasheet](#)

---

1. USB Type-C Connector System Software Interface
2. Unified Extensible Firmware Interface
3. Windows Hardware Quality Labs
4. Adaptive Fast Charging
5. Termination resistors: \(R_P\) read as a DFP, \(R_D\) as a UFP, \(R_{DB}\) as UFP in Dead-Battery scenario
### EZ-PD CCG4/4M

**Dual-Port USB Type-C and PD Port Controller**

#### Applications
- Notebooks, tablets, monitors, docking stations

#### Features
- **Integrated USB Type-C Transceivers Support Two Type-C Ports**
  - Integrated 2x 1-W VCONN FETs and 2x FET control signals, per port programmable Rp and removable Rp, and R0 terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- **Increased Flash Enables Fail-Safe Bootup**
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- **Integrated Digital Blocks for Inter-Chip Communications**
  - Four serial communication blocks (SCBs) master or slave configurable to I2C, SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- **Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)**
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- **Low-Power Operation**
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA;
  - Deep Sleep: 2.5 µA with wake-on-I2C or wake-on-configuration channel (CC)
- **System-Level ESD on CC Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
  - 32-bit Arm® Cortex®-M0 CPU with MCU Subsystem
  - 128KB Flash, upgradable over CC lines or I2C interface
- **Packages**
  - 40-pin QFN, 96-ball BGA (CCG4M)

#### Collateral
- **Datasheet:** [CCG4 Datasheet](#)

---

### CCG4/4M: USB Type-C Port Controller

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<th>Integrated Digital Blocks</th>
<th>I/O Subsystem</th>
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<td><strong>arm® Cortex®-M0</strong> 48 MHz</td>
<td>4 x TCPWM</td>
<td><strong>PORT1</strong></td>
</tr>
<tr>
<td><strong>Flash</strong> (128KB)</td>
<td>4 x SCB (I2C, SPI, UART)</td>
<td><strong>PORT2</strong></td>
</tr>
<tr>
<td><strong>SRAM</strong> (8KB)</td>
<td>2 x Baseband MAC</td>
<td>2x VCONN FETs (PORT1)</td>
</tr>
<tr>
<td><strong>Serial Wire Debug</strong></td>
<td>2 x Baseband PHY</td>
<td>2x VCONN FETs (PORT2)</td>
</tr>
<tr>
<td><strong>Profiles and Configurations</strong></td>
<td>Integrated Rp and Rp</td>
<td>GPIOs</td>
</tr>
<tr>
<td><strong>4 x 8-bit SAR ADC</strong></td>
<td><strong>Programmable I/O Matrix</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Availability**

**Production:** Now

---

1. Termination resistor read as a DFP
2. Termination resistor read as a UFP
EZ-PD CCG3
USB Type-C and PD Port Controller

Applications
Accessories and power adapters

Features
- One Type-C Port with Integrated Transceiver
  - Alternate Modes\(^1\), Crypto Engine\(^2\) for USB Authentication\(^3\)
- Power Delivery (PD) Support for Standard Power Profiles
- Integrated Digital Blocks for \(V_{BUS}\) Power and MUX Interface
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave \(\text{I}^2\text{C}, \text{SPI}\) or UART
  - USB Billboard Controller\(^4\) with Billboard Device Class\(^5\) support
- Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - 21.5-V OVP and OCP; 2:2 cross-bar switch
- 32-bit Arm® Cortex®-M0 CPU with MCU Subsystem
  - 2x64KB Flash for fail-safe updates over CC, \(\text{I}^2\text{C}\) or USB interfaces
- Low-Power Operation
  - 2x \(V_{BUS}\) Gate Drivers\(^6\), for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) \(V_{BUS}\) voltage inputs
  - Sleep: 2.0 mA; Deep Sleep: 2.5 \(\mu\text{A}\) with wake-on-\(\text{I}^2\text{C}\) or wake-on-CC
- System-Level ESD on CC/\(V_{CONN}\), \(V_{BUS}\), and SBU Pins
  - \(\pm8\text{-kV}\) Contact, \(\pm15\text{-kV}\) Air Gap IEC61000-4-2 Level 4C
- Packages
  - 42-ball (8.38 mm\(^2\)) CSP, 40-pin (36 mm\(^2\)) QFN and 32-pin (25 mm\(^2\)) QFN

Collateral
Datasheet: CCG3 Datasheet

Availability
Production: Now

*Mode of operation in which the data lines are repurposed to transmit non-USB data
*The encryption hardware and software required to implement USB Authentication
*A USB-F header that defines the authentication protocol for Type-C accessories
*A USB Device controller that informs the USB Host of the supported Alternate Modes
*A specification that defines the method for a USB Device to communicate the supported Alternate Modes
*Circuits to control the gates of external power Field-Effect Transistors (FETs) on \(V_{BUS}\) (5-20 V)
*Termination resistors: \(R_P\) read as a DFP, \(R_D\) as a UFP, \(R_A\) as an EMCA
EZ-PD CCG2
USB Type-C and PD Port Controller

Applications
USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

Features
- 32-bit MCU Subsystem
  - 48-MHz Arm® Cortex®-M0 CPU with 32KB Flash and 4KB SRAM
- Integrated Digital Blocks
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs\(^1\) configurable to I\(^2\)C, SPI or UART modes
- Type-C Support
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (\(R_P, R_D, R_A\))\(^2\)
- Power Delivery (PD) Support
  - Standard power profiles
- Low-Power Operation
  - Two independent \(V_{CONN}\) rails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation; Sleep: 2.0 mA; Deep Sleep: 2.5 \(\mu\)A
- System-Level ESD on CC and VDD Pins
  - \(\pm8\)-kV Contact, \(\pm15\)-kV Air Gap IEC61000-4-2 Level 4C
- Packages
  - 20-ball CSP (3.3 mm\(^2\)) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm\(^2\)) with 0.55-mm pin pitch

Collateral
Datasheet: [CCG2Datasheet](#)
Reference Design Kit: [CCG2 RDK](#)
Evaluation Kit: [CCG3 EVK](#)

**Datasheet:**
- **CCG2 Datasheet**

**Reference Design Kit:**
- **CCG2 RDK**

**Evaluation Kit:**
- **CCG3 EVK**

**C Yug: USB Type-C Port Controller With PD**

**MCU Subsystem**
- Arm® Cortex-M0
- 48 MHz

**Integrated Digital Blocks**
- TCPWM
- SCB (PC, SPI, UART)

**I/O Subsystem**
- CC
- VCONN1
- VCONN2
- VDDIO
- GPIO
- Port

**Features**
- Serial communication block configurable as UART, SPI or I\(^2\)C
- Termination resistors: \(R_P\) read as a DFP, \(R_D\) as a UFP, \(R_A\) as an EMCA

**Availability**
Production: Now
EZ-USB FX3
USB 3.1 Gen 1 Peripheral Controller

Applications
Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras, document and fingerprint scanners, video conferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz Arm® 926EJ Core
  - 512KB of embedded SRAM for code space and buffers
- 32-bit, 100-MHz, flexible GPIF II Interface
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
Datasheet: FX3 Datasheet
Development Kit: FX3 SuperSpeed Explorer Kit
Software Development Kit: EZ-USB FX3 SDK

Availability
Production: Now
EZ-USB FX3S
USB 3.1 Gen 1 RAID\(^1\)-on-Chip

**Applications**
Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders, and data logging devices

**Features**
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz Arm\(^\circ\) 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I\(^2\)C, I\(^2\)S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
- **Two SDXC\(^2\)/eMMC\(^3\) 4, 4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations
- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Packages**
  - 121-ball BGA (10 mm\(^2\)), 131-ball WLCSP (4.7 x 5.1 mm)

**Collateral**
- Datasheet: [FX3S Datasheet](#)
- Kit: [FX3S RAID\(^1\)-on-Chip Boot Disk Kit](#)
- Software Development Kit: [EZ-USB FX3 SDK](#)

**Availability**
- Production: Now

---

\(^1\) Redundant array of independent disks
\(^2\) SD extended capacity
\(^3\) Embedded Multimedia Card
EZ-USB CX3
MIPI¹ CSI-2 to USB 3.1 Gen 1 Bridge

Applications
- Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz Arm® 926EJ core
  - 512KB of embedded SRAM for code space and buffers
- Four-Lane MIPI¹ Camera Serial Interface v2.0 (CSI-2) Input
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I²C, UART, SPI, and 12 GPIOs
- Supports Industry-Standard Video Data Formats
  - RAW8/10/12, YUV422/444³, RGB888/666/565⁴
- Supports Uncompressed Streaming Video
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- Packages
  - 121-ball BGA (10 x 10 x 1.7 mm)

Collateral
- Datasheet: CX3 Datasheet
- Reference Design Kit: CX3 Reference Design Kit
- Software Development Kit: EZ-USB FX3 SDK

Availability
- Production: Now

1 Mobile Industry Processor Interface ² Video format for luminance and chrominance components
³ Video format for raw video data ⁴ Video format for red, green and blue pixel components
EZ-USB GX3
USB 3.1 Gen 1 to GigE\(^1\) Bridge

**Applications**
USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs, and other embedded systems

**Features**
- One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC\(^2\)
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- IEEE 802.3az\(^3\) Support for Low-Power Idle State
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN\(^4\) features
- Supports Optional EEPROM to Store USB Descriptors
  - Integrates on-chip power-on-reset (POR) circuitry
- Packages
  - 68-QFN (8 x 8 x 0.85 mm)

**Collateral**
- Datasheet: [GX3 Datasheet](#)
- Reference Design Kit: [GX3 Reference Design Kit](#)
- Software & Drivers: [GX3 Drivers](#)

**Availability**
- Production: Now

---

\(^1\) Gigabit Ethernet

\(^2\) Media access controller that provides the address to an Ethernet node

\(^3\) A new-energy efficient Ethernet standard

\(^4\) An Ethernet standard that allows a computer to be turned on by a network message
EZ-USB HX3
USB 3.1 Gen 1 Hub

Applications
Docking stations for notebook PCs and tablets, PC motherboards, servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

Features
- USB 3.1 Gen 1-Compliant Four-Port Hub Controller
  - USB-IF certified (Test ID: 330000047)
  - WHQL certified for Windows 7, Window 8, Windows 8.1
- Shared Link™
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- Ghost Charge™
  - Enables USB charging while the hub is disconnected from a USB Host
- Charging Standard support
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- Programming of External EEPROM via USB
- Configurable USB SS and USB 2.0 PHY (drives 11” trace)
- Packages
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Datasheet: HX3 Datasheet
Kit: CY4609, CY4603, CY4613
Configuration Utility: Blaster Plus¹
App Notes: HX3 Hardware Design Guide (AN91378)

1 A Cypress GUI-based PC application for setting HX3 configuration parameters

Availability
Production: Now
EZ-USB HX3C
USB 3.1 Gen 1 Type-C PD Hub

Applications
USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features
- **USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD**
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- **Integrated Type-C Transceivers, Supporting Two Type-C Ports**
  - Integrated termination resistors (R_P and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\)
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- **Ghost Charge™**
  - Charging DS without US connection
- **Firmware Upgradable Over USB**
- **System-Level ESD on Configuration Channel (CC) Pins**
  - 8 kV Contact, 15 kV Air
- **Configurable USB SS and USB 2.0 PHY (drives 11" trace)**
- **Packages**
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral
- **Datasheet:** HX3C Datasheet
- **Reference Design:** HX3C Type-C Monitor/Dock Reference Design

Availability
- **Production:** Now

---
\(^1\) Termination resistors: R_P read as a DFP, R_D as a UFP  
\(^2\) A USB Device controller that is used to implement the USB Billboard Device Class  
\(^3\) Transaction Translator  
Informs the USB Host of the supported Alternate Modes as well as any failures
Cypress Roadmap: RAM Solutions
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Nonvolatile RAM

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<td>FM25V20A 2Mb; 2.0–3.6 V 40-MHz SPI; Ind</td>
<td>Excelon F-RAM</td>
<td>FM22L16/LS16 4Mb; 2.7–3.6 V 55 ns; x8; Ind</td>
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<tr>
<td>CY15B104O 4Mb; 2.0–3.6 V 40-MHz SPI; Ind</td>
<td>FM24V10/VN10 1Mb; 2.0–3.6 V 3.4-MHz FC; Ind, Auto A</td>
<td>FM28V102A 1Mb; 2.0–3.6 V 60 ns; x16; Ind</td>
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<tr>
<td>FM25V10/VN10 1Mb; 2.0–3.6 V 25-MHz SPI; Auto E</td>
<td>PM24V05 512Kb; 2.0–3.6 V 3.4-MHz FC; Ind, Auto A</td>
<td>FM25V02A 2Mb; 2.0–3.6 V 60 ns; x16; Ind</td>
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<tr>
<td>FM25V05 512Kb; 2.0–3.6 V 40-MHz SPI; Ind</td>
<td>FM24V02A/W256 256Kb; V02A; 2.0–3.6 V 3.4-MHz FC; Ind, Auto A</td>
<td>FM3256 256Kb; 3.3 V; 16-MHz SPI Ind; RTC; Ind, Auto A</td>
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<td>128Kb; 3.3, 5.0 V 20-MHz SPI; Ind</td>
<td>FM24V01A 128Kb; 2.0–3.6 V 3.4-MHz FC; Ind, Auto A</td>
<td>FM28V020 256Kb; 2.0–3.6 V 70 ns; x8; Ind</td>
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<td>FM25640B/CL64B 54Kb; 3.3, 5.0 V 20-MHz SPI; Ind</td>
<td>FM24C64/CL64 64Kb; 3.3, 5.0 V 1-MHz FC; Ind, Auto E</td>
<td>FM28V08 256Kb; 2.7–5.5 V 70 ns; x8; Ind</td>
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<tr>
<td>FM25C160/L16 16Kb; 3.3, 5.0 V 20-MHz SPI; Ind</td>
<td>FM24C16/CL16 16Kb; 3.3, 5.0 V 1-MHz FC; Ind, Auto E</td>
<td>FM1800B 256Kb; 5.0 V 70 ns; x8; Ind</td>
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<tr>
<td>FM25040/L04 4Kb; 3.3, 5.0 V 20-MHz SPI; Ind</td>
<td>FM24C04/CL04 4Kb; 3.3, 5.0 V 1-MHz FC; Ind, Auto A</td>
<td>FM16W08 64Kb; 2.7–5.5 V 70 ns; x8; Ind</td>
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</table>

1 Low-pin-count
2 Industrial grade -40 °C to +85 °C
3 Ultra-low-energy
4 Quad serial peripheral interface
5 AEC-Q001 -40 °C to +85 °C
6 AEC-Q001 -40 °C to +125 °C
7 Real-time clock

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F-RAM™ Portfolio
Low Power | High Endurance

---

84 Cypress Roadmap: RAM Solutions – DMIT
### Excelon™ F-RAM Portfolio

**Ultra Low Power | High Speed | High Endurance**

<table>
<thead>
<tr>
<th>Excelon Auto</th>
<th>Excelon Ultra</th>
<th>Excelon LP</th>
</tr>
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<tbody>
<tr>
<td><strong>CY15B102QN</strong>&lt;br&gt;2Mb; 1.8–3.6 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI; Auto E&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>CY15V102QN</strong>&lt;br&gt;2Mb; 1.71–1.89 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI; Auto E&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>CY15B116QI/N</strong>&lt;br&gt;16Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;108-MHz QSPI, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<td><strong>CY15B104QN</strong>&lt;br&gt;4Mb; 1.8–3.6 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI; Auto E&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>CY15V104QN</strong>&lt;br&gt;4Mb; 1.71–1.89 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI; Auto E&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>CY15B108QI/N</strong>&lt;br&gt;8Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<tr>
<td><strong>CY15B102QN</strong>&lt;br&gt;2Mb; 1.8–3.6 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI; Auto E&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>CY15V102QSN</strong>&lt;br&gt;2Mb; 1.8–3.6 V&lt;br&gt;8-pin SOIC&lt;br&gt;108-MHz QSPF, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<td><strong>CY15V104QSN</strong>&lt;br&gt;4Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN, SOIC&lt;br&gt;108-MHz QSPI, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15B104QI/N</strong>&lt;br&gt;4Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<td><strong>CY15B108QI/N</strong>&lt;br&gt;8Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI, Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15B108QSN</strong>&lt;br&gt;8Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI, Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15B108QN</strong>&lt;br&gt;8Mb; 1.8–3.6 V&lt;br&gt;8-pin SOIC&lt;br&gt;50-MHz SPI, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<td><strong>CY15V108QI/N</strong>&lt;br&gt;8Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15V108QI/N</strong>&lt;br&gt;8Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15V108QSN</strong>&lt;br&gt;8Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI, Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<td><strong>CY15V108QI/N</strong>&lt;br&gt;8Mb; 1.71–1.89 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15V116QI/N</strong>&lt;br&gt;16Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/40-MHz SPI Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
<td><strong>CY15B116QI/N</strong>&lt;br&gt;16Mb; 1.8–3.6 V&lt;br&gt;8-pin GQFN&lt;br&gt;20/50-MHz SPI, Comm&lt;sup&gt;1&lt;/sup&gt;, Ind&lt;sup&gt;2&lt;/sup&gt;</td>
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<sup>1</sup>Commercial grade 0°C to +70°C  
<sup>2</sup>AEC-Q100 -40°C to +85°C  
<sup>3</sup>Industrial grade -40°C to +85°C  
<sup>4</sup>AEC-Q100 -40°C to +125°C  

<sup>1</sup>Quad serial peripheral interface

<table>
<thead>
<tr>
<th>Concept</th>
<th>Development</th>
<th>Sampling</th>
<th>Production</th>
</tr>
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<td><img src="image2.png" alt="Automotive" /></td>
<td><img src="image3.png" alt="Sampling" /></td>
<td><img src="image4.png" alt="Production" /></td>
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</table>
## Cypress Roadmap: RAM Solutions — DMIT

### nvSRAM Portfolio

#### High Density | High Speed

<table>
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<tr>
<th>Parallel nvSRAM</th>
<th>LPC&lt;sup&gt;1&lt;/sup&gt; nvSRAM</th>
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<tbody>
<tr>
<td>CY14B116R/S 16Mb; 3.0 V 25, 45 ns; x32; Ind&lt;sup&gt;2&lt;/sup&gt; RTC&lt;sup&gt;3&lt;/sup&gt;</td>
<td>CY14B256PA 256Kb; 3.0 V 40-MHz SPI; Ind RTC</td>
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<td>CY14B116K/L 16Mb; 3.0 V 25, 45 ns; x8; Ind RTC</td>
<td>CY14B256I 256Kb; 3.0 V 3.4-MHz PC; Ind RTC</td>
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<td>CY14V116F/G 16Mb; 3.0, 1.8 V IO 30 ns; ONFI&lt;sup&gt;1&lt;/sup&gt; 1.0 x8, x16; Ind</td>
<td>CY14B064PA 64Kb; 3.0 V 40-MHz SPI; Ind RTC</td>
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<tr>
<td>CY14B104NA 4Mb; 3.0 V 25, 45 ns; x16 Auto E&lt;sup&gt;4&lt;/sup&gt;, RTC</td>
<td>CY14B064I 64Kb; 3.0 V 3.4-MHz PC; Ind RTC</td>
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<tr>
<td>CY14B104K/LA 4Mb; 3.0 V 25, 45 ns; x8; Ind RTC</td>
<td>CY14V101PA 1Mb; 3.0 V 40-MHz SPI; Ind RTC</td>
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<td>CY14B101KA/LA 1Mb; 3.0 V 25, 45 ns; x8; Ind RTC</td>
<td>CY14B101P5 1Mb; 3.0, 1.8 V IO 108-MHz QSPI; Ind Ext. Ind&lt;sup&gt;8&lt;/sup&gt;; RTC</td>
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<tr>
<td>CY14V101LA 1Mb; 3.0, 1.8 V IO 25, 45 ns; x8; Ind RTC</td>
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<td>CY14B101MA/NA 1Mb; 3.0 V 25, 45 ns; x16; Ind RTC</td>
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<td>CY14VU256LA 256Kb; 3.0, 1.8 V IO 35 ns; x8; Ind RTC</td>
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<td>CY14E256LA 256Kb; 5.0 V 25, 45 ns; x8; Ind RTC</td>
<td>CY14B101Q5S 1Mb; 3.0, 1.8 V IO 108-MHz QSPI; Ind Ext. Ind&lt;sup&gt;8&lt;/sup&gt;; RTC</td>
</tr>
</tbody>
</table>

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1. Low-pin-count
2. Industrial grade -40 °C to +85 °C
3. Real-time clock
4. Open NAND flash interface
5. Error-correcting code
6. AEC-Q100 -40 °C to +125 °C
7. Quad serial peripheral interface
8. Extended Industrial grade -43 °C to +105 °C
9. Military grade -55 °C to +125 °C

Industrial
- Automotive
- Concept
- Development
- Sampling
- Production
Nonvolatile RAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(ES) [EOL]</th>
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<th>2020</th>
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<th>2022</th>
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2Mb-to-16Mb Excelon™ F-RAM Family

Applications
Medical devices, wearables, industrial control and automation, and automotive

Features
- **Excelon-Ultra**
  - 2Mb to 16Mb
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - Industrial temperature range: -40 °C to +85 °C
- **Excelon-Auto**
  - 2Mb to 8Mb Auto “E”, 4Mb to 16Mb Auto “A”
  - 50-MHz Serial Peripheral Interface (SPI)
  - Automotive temperature range grade “A”: -40 °C to +85 °C
  - Automotive temperature range grade “E”: -40 °C to +125 °C
- **Excelon-LP**
  - 2Mb to 16Mb
  - 20-MHz SPI (Commercial), 50-MHz SPI (Industrial)
  - Ultra-low (0.1-µA) hibernate current
  - Ultra-low (0.75-µA) deep power-down current
  - Ultra-low (2.3-µA) standby current
  - Commercial temperature range: 0 °C to +70 °C
  - Industrial temperature range: -40 °C to +85 °C
- **Common features for Excelon-Ultra/Auto/LP**
  - Operating voltage ranges: 1.71 V to 1.89 V, 1.80 V to 3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

Collateral
Final Datasheets: 4Mb Excelon-Ultra; 2Mb Excelon-Auto; 8Mb Excelon-LP

Excelon F-RAM

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>Standby Current (Typ.)</th>
<th>Active Current (Typ.)</th>
<th>Packages</th>
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<tbody>
<tr>
<td>2Mb</td>
<td>2.3 µA</td>
<td>3 mA</td>
<td>SOIC (8), TDFN (8)</td>
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<td>2.3 µA</td>
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<td>SOIC (8), GQFN (8)</td>
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</table>

Availability
- **Sampling:** Now (4Mb Auto A, 4Mb & 8Mb Ultra/LP), Q419 (2Mb Ind), Q220 (16Mb)
- **Production:** Now (2Mb Auto E, 4Mb & 8Mb Ultra/LP), Q419 (4Mb Auto A), Q120 (2Mb Ind), Q420 (16Mb)

1 Quad SPI has 4 I/Os
# F-RAM Packages

<table>
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<th>Density</th>
<th>8-pin SOIC</th>
<th>8-pin DFN</th>
<th>8-pin GQFN</th>
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<th>14-pin SOIC</th>
<th>28-pin SOIC</th>
<th>28-pin TSOP I</th>
<th>32-pin TSOP I</th>
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# nvSRAM Packages

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<th>48-pin SSOP</th>
<th>48-pin TSOP I</th>
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Parallel Asynchronous SRAM

Low-Power (MoBL®), Fast, PowerSnooze™
### Parallel Asynchronous SRAM Portfolio

**High Density | Wide Voltage Range | Automotive A, E | On-Chip ECC**

<table>
<thead>
<tr>
<th>Density</th>
<th>32Mb–64Mb</th>
<th>2Mb–16Mb</th>
<th>64Kb–1Mb</th>
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<td><strong>Non-ECC (≥90 nm)</strong></td>
<td><strong>ECC (65 nm)</strong></td>
<td><strong>Non-ECC (290 nm)</strong></td>
<td><strong>ECC (65 nm)</strong></td>
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<tr>
<td>CY7C107x 32Mb; 3.3 V 12 ns; x8, x16 Ind</td>
<td>CY7C106xGN 16Mb; 1.8, 3.3 V 10 ns; x8, x16, x32 Ind</td>
<td>CY6218x 64Mb; 1.8, 3.0 V 55 ns; x16 Ind</td>
<td>CY6216x 64Mb, 3.0 V 55 ns; x16, x32 Ind</td>
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<tr>
<td>CY7C1012 12Mb; 3.3 V 10 ns; x24 Ind</td>
<td>CY7C106xG/GE 16Mb; 1.8–5.0 V 10 ns; x8, x16, x32 Ind</td>
<td>CY6217x 32Mb; 1.8–5.0 V 55 ns; x16 Ind</td>
<td>CY6217x 32Mb; 1.8–5.0 V 55 ns; x16, x32 Ind</td>
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<td>CY7C1004 6Mb; 3.3 V 10 ns; x24 Ind</td>
<td>CY7C106x 8Mb; 3.3, 5.0 V 10 ns; x8, x16, x32 Ind</td>
<td>CY6215x 8Mb; 1.8, 3.0, 2.5–5.0 V 45 ns; x8, x16 Ind</td>
<td>CY6215x 8Mb; 1.8, 3.0 V 45 ns; x8, x16 Ind</td>
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<td>CY7C1010/11 2Mb; 3.3 V 10 ns; x8, x16 Ind, Auto A, E</td>
<td>CY7C1014 4Mb; 3.3, 5.0 V 10 ns; x8, x16 Ind</td>
<td>CY6214x 4Mb; 1.8, 3.0, 2.5–5.0 V 45 ns; x8, x16 Ind</td>
<td>CY6214x 4Mb; 1.8–5.0 V 45 ns; x8, x16 Ind</td>
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<td>CY7C1020 512Kb; 2.6, 3.3, 5.0 V 10 ns; x16 Ind, Auto A</td>
<td>CY7C1019/21/100x 1Mb; 2.6, 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E</td>
<td>CY6213x 1Mb; 2.5–5.0 V 45 ns; x8, x16 Ind, Auto A, E</td>
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<td>CY7C19x/1399 256Kb; 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A</td>
<td>CY6212x 1Mb; 2.5–5.0 V 45 ns; x8, x16 Ind, Auto A, E</td>
<td>CY6212x 1Mb; 2.5–5.0 V 45 ns; x8, x16 Ind, Auto A, E</td>
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<tr>
<td>CY6225x 256Kb; 1.8, 3.0, 5.0 V 55 ns; 70 ns; x8 Ind, Auto A, E</td>
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<td>CY6225x 256Kb; 1.8, 3.0, 5.0 V 55 ns; 70 ns; x8 Ind, Auto A, E</td>
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1 AEC-Q100 -40°C to +85°C
2 AEC-Q100 -40°C to +125°C
3 More Battery Life
4 A Fast SRAM with a deep-sleep mode in addition to the conventional standby
5 Ultra-Low-Power
6 EEC (65 nm) ULP

**PowerSnooze™:**

- ECC (65 nm)
- Non-ECC (≥90 nm)
- Non-ECC (≥90 nm)
- ULP (65 nm)

**Manufacturing:**

- Industrial
- Automotive
- Concept
- Development
- Sampling
- Production
### Parallel Asynchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
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<tr>
<td>MoBL SRAM ULP 65 nm, ECC</td>
<td>8Mb, 16Mb, 32Mb, 64Mb</td>
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<tr>
<td>MoBL SRAM 65 nm, ECC</td>
<td>4Mb, 8Mb, 16Mb</td>
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<tr>
<td>MoBL SRAM ≥ 90 nm, Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
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<tr>
<td>PowerSnooze SRAM 65 nm, ECC</td>
<td>4Mb, 16Mb</td>
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<tr>
<td>Fast SRAM 65 nm, ECC</td>
<td>2Mb, 4Mb, 8Mb, 16Mb</td>
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<tr>
<td>Fast SRAM ≥ 90 nm, Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 4Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb</td>
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#### Timeline

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**Legend:**
- **Concept**
- **Samples**
- **Production**
- **EOL**
Low-Power SRAM Family with ECC

**Applications**
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive

**Features**
- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC\(^1\) logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS\(^2\)-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

**Collateral**
Datasheet: [Asynchronous SRAM with ECC](#)

---

\(^1\) Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

\(^2\) Restriction of Hazardous Substances: A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

---

**SRAM with ECC**

**Family Table**

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<tr>
<th>Density</th>
<th>MPN</th>
<th>Standby Current (Maximum at 85°C)</th>
<th>Standby Current (Typical at 25°C)</th>
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<td>5.5 µA</td>
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<td>CY6216x</td>
<td>16.0 µA</td>
<td>5.5 µA</td>
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</table>

**Availability**
Production: Now
Ultra Low-Power MoBL®\textsuperscript{1} SRAM Family with ECC\textsuperscript{2}

### Applications
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, and computation servers

### Features
- **Speed**
  - Access time: 45/55 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.0 µA max for 16Mb
- **Operating Voltage Range**
  - 2.2 V to 3.6 V, 1.65V to 2.25V (8Mb)
- **Features**
  - ECC\textsuperscript{2} logic to detect and correct single-bit errors
  - 16Mb, 32Mb, 64Mb; Industrial grade: -40 °C to +85 °C
  - 8Mb; Industrial and Automotive A grade: -40 °C to +85 °C, Automotive E grade: -40 °C to +125 °C
- **RoHS\textsuperscript{3}-compliant Packages**
  - All existing MoBL packages supported

### Collateral
- **Datasheet:** Contact Sales

### SRAM with ECC

![SRAM with ECC Diagram](image)

### Family Table

<table>
<thead>
<tr>
<th>Density</th>
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<th>Standby Current (Maximum at 85 C)</th>
<th>Standby Current (Typical at 25 C)</th>
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<td>CY6218x</td>
<td>38.0 µA</td>
<td>6.0 µA</td>
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</table>

### Availability
- **Sampling:** 8Mb Q419
- **Production:** 8Mb Q120, 16Mb Now, 32Mb: Now, 64Mb: Dec ‘19

\textsuperscript{1} MoBL: More Battery Life

\textsuperscript{2} Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

\textsuperscript{3} Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
Fast SRAM Family with PowerSnooze™

Applications
Programmable logic controllers, handheld devices, multifunction printers, computation servers and automotive

Features
- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS-compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

Collateral
**Datasheet:** Asynchronous SRAM with ECC

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (Maximum at 85ºC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>10 ns</td>
<td>15 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>10 ns</td>
<td>22 µA</td>
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</table>

Availability
**Production:** Now

Footnotes:
1. A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
2. Error-correcting code
3. Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous materials in electronic components
Fast SRAM Family with ECC

**Applications**

- Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

**Features**

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32

- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors

- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades

- **RoHS²-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

**Collateral**

- Datasheet: Asynchronous SRAM with ECC

---

1 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

2 Restriction of Hazardous Substances: A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

---

**SRAM with ECC**

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Operating Current (Maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7C104x</td>
<td>10 ns</td>
<td>45 mA</td>
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<tr>
<td>8Mb</td>
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<td>16Mb</td>
<td>CY7C106x</td>
<td>10 ns</td>
<td>110 mA</td>
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**Availability**

- **Production:** Now
## Asynchronous SRAM Packages

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</table>
HyperRAM

High-performance Pseudo-static RAM
# HyperRAM™ Portfolio

<table>
<thead>
<tr>
<th></th>
<th>HyperRAM 1.0 S27KL-1</th>
<th>HyperRAM 1.0 S27KS-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>63-nm DR, 3.0 V HyperBus I/F</td>
<td>63-nm DR, 1.8 V HyperBus I/F</td>
</tr>
<tr>
<td>Initial Access/DDR Clock * Temperature Range</td>
<td>36 ns/100 MHz</td>
<td>36 ns/166 MHz</td>
</tr>
<tr>
<td>64Mb–128Mb</td>
<td>128Mb</td>
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</tr>
<tr>
<td>* I, A, V, B</td>
<td>64Mb</td>
<td>64Mb</td>
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<tr>
<td>36 ns/100 MHz</td>
<td>36 ns/166 MHz</td>
<td>36 ns/66 MHz</td>
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<tr>
<td>* I, A, V, B</td>
<td>36 ns/100 MHz</td>
<td>36 ns/66 MHz</td>
</tr>
</tbody>
</table>

* I = Industrial: -40 °C to +85 °C
A = Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C
V = Industrial-plus: -40 °C to +105 °C
B = Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C

1 Stacked die

## HyperRAM Portfolio

- **HyperRAM 1.0 S27KL-1**: 63-nm DR, 3.0 V HyperBus I/F
- **HyperRAM 1.0 S27KS-1**: 63-nm DR, 1.8 V HyperBus I/F

### Density
- Initial Access/DDR Clock
- * Temperature Range

### Initial Access/DDR Clock
- 36 ns/100 MHz
- 36 ns/166 MHz
- 36 ns/66 MHz

### Temperature Ranges
- I = Industrial: -40 °C to +85 °C
- A = Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C
- V = Industrial-plus: -40 °C to +105 °C
- B = Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C

Additional information on the HyperRAM™ Portfolio includes:

- **HyperRAM™**: Stacked die production
- **Concept Development**: Sampling
- **Production**: Concept

**Note:** Cypress Roadmap: RAM Solutions – DMIT
# HyperRAM™ Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td>S27KS-1 (1.8 V)</td>
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<td>S27KL-1 (3.0 V)</td>
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<td>63-nm PS-RAM</td>
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1 Stacked die

Products supported by Longevity Program unless noted

- Concept
- Production
- Samples
- EOL - LTB
- EOL - LTS
Synchronous SRAM

Std Sync, NoBL®, QDR-II, DDR-II, QDR-IV
### Synchronous SRAM Portfolio

#### High Random Transaction Rate (RTR) | Low Latency | High Bandwidth

<table>
<thead>
<tr>
<th>Density</th>
<th>Standard Sync and NoBL</th>
<th>Standard Sync and NoBL with ECC</th>
<th>QDR®-II/DDR-II</th>
<th>QDR-II+/DDR-II+</th>
<th>QDR-II+/X/DDR-II+</th>
<th>QDR-IV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RTR: 250 MT/s (max.)</td>
<td>RTR: 250 MT/s (max.)</td>
<td>RTR: 666 MT/s (max.)</td>
<td>RTR: 666 MT/s (max.)</td>
<td>RTR: 900 MT/s (max.)</td>
<td>RTR: 2.1 GT/s (max.)</td>
</tr>
<tr>
<td></td>
<td>BW: 18 Gbps (max.)</td>
<td>BW: 18 Gbps (max.)</td>
<td>BW: 47.8 Gbps (max.)</td>
<td>BW: 79.2 Gbps (max.)</td>
<td>BW: 91.1 Gbps (max.)</td>
<td>BW: 153.5 Gbps (max.)</td>
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<td></td>
<td>Latency: 1 Cycle</td>
<td>Latency: 1 Cycle</td>
<td>Latency: 1.5 Cycles</td>
<td>Latency: 2 or 2.5 Cycles</td>
<td>Latency: 2.5 Cycles</td>
<td>Latency: 5 or 8 Cycles</td>
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<td>Pipeline and Flow</td>
<td>Pipeline and Flow</td>
<td>CIO² and SIO³</td>
<td>CIO and SIO, ODT</td>
<td>CIO and SIO, ODT</td>
<td>Dual-Port Bidirectional</td>
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<table>
<thead>
<tr>
<th>Model</th>
<th>Density</th>
<th>Frequency</th>
<th>Voltage</th>
<th>I/O Configuration</th>
<th>Features</th>
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</thead>
<tbody>
<tr>
<td>CY7C161/2xKV18</td>
<td>144Mb; 250–333 MHz</td>
<td>1.8 V; x18, x36</td>
<td>Burst 2, 4</td>
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<tr>
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<td>72Mb; 250–333 MHz</td>
<td>1.8 V; x9, x18, x36</td>
<td>Burst 2, 4</td>
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<td>CY7C141/2xKV18</td>
<td>36Mb; 250–333 MHz</td>
<td>1.8 V; x8, x9, x18, x36</td>
<td>Burst 2, 4</td>
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<td>CY7C131/2x9KV18</td>
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<td>CY7C1911xKV18</td>
<td>18Mb; 250–333 MHz</td>
<td>1.8 V; x9</td>
<td>Burst 2, 4</td>
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1. Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
2. Error-correcting code
3. Common I/O
4. Separate I/O
5. On-die termination
6. Radiation hardened, military grade
7. AEC-Q100: -40 °C to +125 °C

---

103 Cypress Roadmap: RAM Solutions – DMIT
<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
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<td>Q1</td>
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<td>QDR-IV SRAM 65 nm, ECC 2.1 GT/s, 153.5 Gbps</td>
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<td>QDR-II+ SRAM 65 nm, ECC 666 MT/s, 79.2 Gbps</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
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<tr>
<td>QDR-II SRAM 65 nm 666 MT/s, 47.9 Gbps</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
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<td>Standard Sync and NoBL SRAM 65 nm / 90 nm 250 MT/s, 18 Gbps</td>
<td>2Mb, 4Mb, 9Mb, 18Mb, 36Mb, 72Mb</td>
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<td>Standard Sync and NoBL SRAM 90 nm 250 MT/s, 18 Gbps</td>
<td>36Mb [LTS Q2'18]</td>
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1 Radiation hardened, military grade
2 AEC-Q100 -40°C to +125°C
3 65-nm
4 65-nm
Standard Synchronous SRAM With On-Chip ECC

**Applications**
- Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

**Features**
- **Speed**
  - Available in two modes:\(^2\): Pipeline and Flow-Through
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options:\(^3\)
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

**Collateral**
- Datasheets: [36M Sync SRAM](#), [18M Sync SRAM](#)

---

1. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2. Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
3. Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command

---

**Synchronous SRAM**

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb(^4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with On-Chip ECC Pipeline</td>
<td>18Mb/36Mb</td>
<td>CY7C1370/2K, CY7C1440/2K</td>
<td>250 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Standard Sync with On-Chip ECC Flow-Through</td>
<td>18Mb/36Mb</td>
<td>CY7C1371/3K, CY7C1441/3K</td>
<td>133 MT/s</td>
<td>&lt;0.01</td>
</tr>
</tbody>
</table>

---

**Availability**

**Production:** Now
**NoBL® SRAM With On-Chip ECC¹**

### Applications

Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

### Features

- **Speed**
  - Available in two modes²: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18, x36

- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades

- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

### Collateral

**Datasheets:** [36M NoBL SRAM](#), [18M NoBL SRAM](#)

---

¹ Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
² Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
³ The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

---

### Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
</tr>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
</tr>
<tr>
<td></td>
<td>CY7C1380/2K</td>
</tr>
<tr>
<td></td>
<td>CY7C1460/2K</td>
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<td></td>
<td>CY7C1381/3K</td>
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<tr>
<td></td>
<td>CY7C1461/3K</td>
</tr>
<tr>
<td>RTR</td>
<td>250 MT/s</td>
</tr>
<tr>
<td></td>
<td>133 MT/s</td>
</tr>
<tr>
<td>FIT/Mb³</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>&lt;0.01</td>
</tr>
</tbody>
</table>

---

### Availability

**Production:** Now
QDR®-IV SRAM

Applications
Switches and routers, high-performance computing, military and aerospace systems, test and measurement

Features
- **Speed**
  - Available in two options: QDR-IV HP (RTR 1,334 MT/s) and QDR-IV XP (RTR 2,132 MT/s)
  - Two independent, bidirectional DDR\(^1\) data ports
  - Bus widths: x18, x360.13
- **Features**
  - ECC\(^2\) to reduce soft error rate to less than 0.01 FIT/Mb\(^3\)
  - Bus inversion to reduce simultaneous switching I/O noise
  - On-die termination (ODT) to reduce board complexity
  - De-skew training\(^4\) to improve signal-capture timing
  - I/O levels: 1.2–1.25 V (HSTL/SSTL), 1.1–1.2 V (POD\(^5\))
- **Package**
  - 361-pin FCBGA\(^6\)

Collateral
- Datasheets: CY7C4122KV13/CY7C4142KV13
  - CY7C4121KV13/CY7C4141KV13
  - CY7C4022KV13/CY7C4042KV13
  - CY7C4021KV13/CY7C4041KV13

1 Double Data Rate: Two data transfers per clock cycle
2 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors
3 Failures in Time per Megabit
4 An iterative algorithm for assessing and eliminating the skew between multiple data signals
5 Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up drive strength
6 Flip-Chip Ball Grid Array

Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>Maximum Frequency</th>
<th>RTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDR-IV HP</td>
<td>72Mb</td>
<td>CY7C40x1KV13</td>
<td>667 MHz</td>
<td>1,334 MT/s</td>
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<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x1KV13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-IV XP</td>
<td>72Mb</td>
<td>CY7C40x2KV13</td>
<td>1,066 MHz</td>
<td>2,132 MT/s</td>
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<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x2KV13</td>
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Availability
Production: Now
# Synchronous SRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>100-pin TQFP</th>
<th>119-ball BGA</th>
<th>165-ball BGA</th>
<th>209-ball BGA</th>
<th>361-ball BGA</th>
<th>Wafer</th>
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</thead>
<tbody>
<tr>
<td>Std Sync</td>
<td>18Mb</td>
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<td>✓</td>
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<td>NoBL</td>
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<td>9Mb</td>
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<td>✓</td>
<td>✓</td>
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<td>✓</td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<td>✓</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>✓</td>
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<td>✓</td>
<td></td>
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<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
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<td>✓</td>
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<tr>
<td>QDR</td>
<td>9Mb</td>
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<td></td>
<td></td>
<td>✓</td>
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<tr>
<td></td>
<td>72Mb</td>
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<td>✓</td>
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<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
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</table>
Specialty Memory

Dual-Port SRAM, FIFO
## Specialty Memory

### Intelligent Memory | High Density | High Throughput

<table>
<thead>
<tr>
<th>Density</th>
<th>2Mb–1Mb</th>
<th>2Mb–72Mb</th>
</tr>
</thead>
<tbody>
<tr>
<td>128Kb–1Mb</td>
<td>Dual-Port SRAM</td>
<td>FIFO</td>
</tr>
</tbody>
</table>

### Dual-Port SRAM
- **Asynchronous**
- **Synchronous**

<table>
<thead>
<tr>
<th>Model</th>
<th>Density</th>
<th>Temp Range</th>
<th>Speeds</th>
<th>Pin Count</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY7C022x/3x/5x</td>
<td>512Kb, 1Mb</td>
<td>3.3, 5.0 V</td>
<td>12 ns, 20 ns, 25 ns</td>
<td>x8, x16, x18, x36; Ind</td>
<td>Development</td>
</tr>
<tr>
<td>CY7C060/25x/206</td>
<td>128Kb, 256Kb</td>
<td>3.3, 5.0 V</td>
<td>15 ns, 20 ns, 25 ns, 55 ns</td>
<td>x8, x16, x18, Ind</td>
<td>Development</td>
</tr>
<tr>
<td>CY7C024/144</td>
<td>64Kb</td>
<td>3.3, 5.0 V</td>
<td>15 ns, 20 ns, 25 ns, 55 ns</td>
<td>x8, x16, x18, Ind</td>
<td>Development</td>
</tr>
<tr>
<td>CY7C13x</td>
<td>8Kb, 16Kb, 32Kb</td>
<td>5.0 V</td>
<td>15 ns, 25 ns, 55 ns</td>
<td>x8; Ind</td>
<td>Development</td>
</tr>
</tbody>
</table>

### FIFO
- **Asynchronous**
- **Synchronous**

<table>
<thead>
<tr>
<th>Model</th>
<th>Density</th>
<th>Temp Range</th>
<th>Speeds</th>
<th>Pin Count</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYD02/9/18/365xxV18</td>
<td>2Mb, 9Mb, 18Mb, 36Mb</td>
<td>1.8 V</td>
<td>167 MHz, 200 MHz</td>
<td>x18, x36, x72; Ind</td>
<td>Production</td>
</tr>
<tr>
<td>CY7C083x/5x</td>
<td>2Mb, 4Mb, 9Mb</td>
<td>3.3 V</td>
<td>100 MHz, 133 MHz, 167 MHz</td>
<td>x18, x36, x72; Ind</td>
<td>Production</td>
</tr>
<tr>
<td>CY7C9279/289/389/579</td>
<td>512Kb, 1Mb</td>
<td>3.3 V</td>
<td>7, 9, 12 ns, 83 MHz</td>
<td>x8, x16, x18, x36; Ind</td>
<td>Production</td>
</tr>
<tr>
<td>CY7C09259/369</td>
<td>256Kb</td>
<td>3.3 V</td>
<td>9 ns, 12 ns</td>
<td>x16, x18; Ind</td>
<td>Production</td>
</tr>
<tr>
<td>CY7C09159/349</td>
<td>64Kb</td>
<td>3.3 V</td>
<td>9 ns, 12 ns</td>
<td>x9, x18; Comm</td>
<td>Production</td>
</tr>
</tbody>
</table>

### Video Frame Buffer products
1. Video Frame Buffer products
2. Programmable Bus Width
3. Industrial grade -40°C to +85°C
4. Commercial grade 0°C to +85°C
Timing Solutions Portfolio
## Clock Synthesizer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod)</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27430</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td></td>
<td>12 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EMP; 0.7-ps RMS Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.8 V/2.5 V/3.3 V; Ind; 48-QFN</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>CY27410</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td></td>
<td>8 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EMP; 0.7-ps RMS Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.8 V/2.5 V/3.3 V; Auto A²</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>8-QFN</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CCY254x/CY251x</td>
<td>1-4 PLL; Maximum Frequency: 200 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td></td>
<td>3-9 Outputs; FC; EMI; Low Power</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>100-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V</td>
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<tr>
<td></td>
<td>8-SOIC; 8/16/20-TSSOP; 24-QFN</td>
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</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Maximum Frequency: 166 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td></td>
<td>3-8 Outputs; CMOS; Low Power</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>200-ps PPJ; VCXO; Ind; 3.3 V/5 V</td>
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<tr>
<td></td>
<td>8/16/20-SOIC; 16-TSSOP</td>
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<tr>
<td>CY2429x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
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<tr>
<td></td>
<td>2-5 Outputs; HCSL, CMOS; EMI</td>
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<td>75-ps CCJ; PCIe 1.1; Ind; Auto A</td>
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<tr>
<td></td>
<td>3.3 V; 16-TSSOP; 32-QFN</td>
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</tr>
<tr>
<td>CY2239x</td>
<td>3-4 PLL; Maximum Frequency: 400 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
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<tr>
<td></td>
<td>5-8 Outputs; LVPECL, CMOS; FC</td>
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<tr>
<td></td>
<td>400-ps PPJ; VCXO; 3.3 V</td>
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<tr>
<td></td>
<td>Ind; Auto A; E⁶</td>
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<tr>
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<td>16-TSSOP; 32-QFN</td>
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<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
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<tr>
<td></td>
<td>1-3 Outputs; CMOS; EMI</td>
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<tr>
<td></td>
<td>110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP</td>
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</tr>
<tr>
<td>CY22050/150</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td></td>
<td>6 Outputs; CMOS; FC</td>
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<tr>
<td></td>
<td>250-ps PPJ; Ind; 2.5 V/3.3 V; 16-TSSOP</td>
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</tbody>
</table>

1. Differential and single-ended outputs
2. Voltage-controlled crystal oscillation
3. Electro Magnetic Interference reduction using Lexmark profile
4. Integrated phase noise across 12-kHz to 20-MHz offset
5. Industrial grade: -40°C to +85°C
6. AEC-Q100: -40°C to +85°C
7. AEC-Q100: -40°C to +105°C
8. Power management options
9. Cycle-to-cycle jitter
10. Peak-to-peak period jitter
11. AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted.

12 Timing Solutions - DMIT
### Oscillator Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
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<tbody>
<tr>
<td><strong>High Performance</strong></td>
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</tr>
<tr>
<td>CY294x</td>
<td>1-PLL, Maximum Frequency: 2.1 GHz</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>1 Output; Diff &amp; SE; 40/100 GbE; VCXO; 0.11-ps RMS Jitter; Ind; 8-LCC (7 x 5, 5 x 3.2); 16-QFN</td>
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<tr>
<td>CY51x7</td>
<td>1-PLL, Maximum Frequency: 2.1 GHz</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>1 Output; Diff &amp; SE; 40/100 GbE; VCXO; 0.11-ps RMS Jitter; Ind; 1.8 V/2.5 V/3.3 V; WAFER/DE</td>
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</tr>
<tr>
<td>CY2Xx (FleXO™)</td>
<td>1 PLL, Maximum Frequency: 680 MHz</td>
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</tr>
<tr>
<td></td>
<td>1 Output; LVCMOS, LVDS, LVPECL Frequency Margining; 0.6-ps RMS Jitter; Ind; 8-LCC (7 x 5, 5 x 3.2); 8-TSSOP</td>
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<tr>
<td>CY25701</td>
<td>1-PLL, Maximum Frequency: 166 MHz</td>
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<tr>
<td></td>
<td>1 Output; CMOS; EMF; 85-ps CCJ; Ind; 3.3 V; 4-LCC (8 x 3.2)</td>
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<tr>
<td>CY2037/5037</td>
<td>1-PLL, Maximum Frequency: 133 MHz</td>
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<tr>
<td></td>
<td>1 Output; CMOS; 100-ps CCJ; Ind; 3.3 V/5.0 V; WAFER</td>
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<tr>
<td>CY5077</td>
<td>1-PLL, Maximum Frequency: 166 MHz</td>
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<td>1 Output; CMOS; 75-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V; WAFER</td>
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<tr>
<td>CY5057</td>
<td>1-PLL, Maximum Frequency: 170 MHz</td>
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<tr>
<td></td>
<td>1 Output; CMOS; EMI; &lt;200-ps CCJ; Ind; 3.3 V/5.0 V; WAFER</td>
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</tbody>
</table>

1. Differential and single-ended outputs
2. Voltage-controlled crystal oscillation
3. Integrated phase noise across 12-kHz to 20-MHz offset
4. Industrial grade: -40°C to +85°C
5. Electromagnetic interference reduction using Lexmark profile
6. Cycle-to-cycle jitter

---

**Legend:**
- **Concept** (EOL - LTS)
- **Samples** (EOL - LTB)
- **Production** (EOL - LT)
# Clock Buffer Roadmap

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<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
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<tbody>
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<td><strong>High Performance</strong></td>
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<tr>
<td>CY2DPx/CPx</td>
<td>Maximum Frequency: 1.5 GHz</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td></td>
<td>2-10 Outputs; LVPECL; 2.5 V/3.3 V</td>
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<tr>
<td></td>
<td>0.11-ps Additive Jitter1; Ind2</td>
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<tr>
<td></td>
<td>8/20-TSSOP; 8-SOIC; 32-TQFP</td>
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<tr>
<td>CY2DMx/DLx</td>
<td>Maximum Frequency: 1.5 GHz</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td></td>
<td>2-10 Outputs; LVDS, CML; 2.5 V/3.3 V</td>
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<tr>
<td></td>
<td>0.11-ps Additive Jitter; Ind</td>
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<td></td>
<td>8/20-TSSOP; 32-TQFP</td>
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<tr>
<td>CY230x/EP0x (Zero Delay)</td>
<td>Maximum Frequency: 220 MHz</td>
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<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<td>2-9 Outputs; LVCMOS; 2.5 V/3.3 V/5 V</td>
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<td>22-ps CCJ; Ind; Auto A+</td>
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<td></td>
<td>8/16-SOIC; 16-TSSOP; WAFER</td>
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<tr>
<td>CY230xNZ/2994x (Non-Zero Delay)</td>
<td>Maximum Frequency: 200 MHz</td>
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<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<td></td>
<td>4-18 Outputs; LVCMOS</td>
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<td>100-ps Op-Op Skew; Ind</td>
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<td>2.5 V/3.3 V; 8-TSSOP; 16-SOIC</td>
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<td>CY23FS04/08/FP12 (Zero Delay)</td>
<td>Maximum Frequency: 200 MHz</td>
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<td>Q1</td>
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<td>Q3</td>
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<td>4-12 Outputs; LVCMOS; Fail Safe</td>
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<td>200-ps CCJ; Ind</td>
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<td></td>
<td>2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP</td>
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<tr>
<td>CY23S0x (Zero Delay)</td>
<td>Maximum Frequency: 133 MHz</td>
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<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<td>5-9 Outputs; LVCMOS</td>
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<td>Spread Aware; 90-ps CCJ; Ind</td>
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<td>2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP</td>
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<tr>
<td>CY7B99x (RoboClock™)</td>
<td>Maximum Frequency: 200 MHz</td>
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<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
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<td>8-13 Outputs</td>
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<tr>
<td></td>
<td>Configurable Skew; 2.5 V/3.3 V/5.0 V</td>
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<td>50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA</td>
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</tbody>
</table>

1 Additive RMS phase jitter
2 Industrial grade: -40°C to +85°C
3 Cycle-to-cycle jitter
4 AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted.
Timing Solutions Portfolio
Programmable | High-Performance | EMI Reduction | Automotive

### Clock Synthesizers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27410</td>
<td>4-PLL; Max Freq: 700 MHz; 12 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter; Auto A/E; 48-QFN</td>
</tr>
<tr>
<td>CY27430</td>
<td>4-PLL; Max Freq: 700 MHz; 8 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter; Auto A/E; 48-QFN</td>
</tr>
</tbody>
</table>

### Oscillators

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2941x/2xx</td>
<td>1-PLL; Max Freq: 2.1 GHz; 1 Output; Diff &amp; SE; 40/100 GbE; VCXO: 0.11-ps RMS Jitter; Ind; 1.8/2.5/3.3 V; Auto A/E; 48-QFN</td>
</tr>
<tr>
<td>CY51x7</td>
<td>1-PLL; Max Freq: 2.1 GHz; 1 Output; Diff &amp; SE; 40/100 GbE; VCXO: 0.11-ps RMS Jitter; Ind; 1.8/2.5/3.3 V; WAFER/DE</td>
</tr>
</tbody>
</table>

### Clock Buffers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2DPx/CPx</td>
<td>Max Freq: 1.5 GHz; 2-10 Outputs; LVPECL; 2.5/3.3 V; 0.11-ps Additive Jitter; 8/20-TSSOP; 8-SOIC; 32-TQFP</td>
</tr>
<tr>
<td>CY2DMx/OLx</td>
<td>Max Freq: 1.5 GHz; 2-10 Outputs; LVPECL; 2.5/3.3 V; 0.11-ps Additive Jitter; 8/20-TSSOP; 32-TQFP</td>
</tr>
</tbody>
</table>

### Standard Performance

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY254x/CY251x</td>
<td>1-4-PLL; Max Freq: 200 MHz; 3-9 Outputs; PC: EMI; Low Power; 100-pcs CCJ; Ind; 1.8/2.5/3.3 V; 8-SOIC; 8/16/20-TSSOP; 24-QFN</td>
</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4-PLL; Max Freq: 166 MHz; 3-8 Outputs; CMOS: Low Power; 200-ps PPU; VCXO; Ind; 3.3 V; 8-SOIC; 16-TSSOP; 32-QFN</td>
</tr>
</tbody>
</table>

### High Performance

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
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</thead>
<tbody>
<tr>
<td>CY22429x</td>
<td>1-PLL; Max Freq: 200 MHz; 2-5 Outputs; HCSL; CMOS; EMI; 75-ps CCJ; PCL; Ind; Auto A; 3.3 V; 16-TSSOP; 32-QFN</td>
</tr>
<tr>
<td>CY2220x</td>
<td>3-4-PLL; Max Freq: 400 MHz; 5-8 Outputs; LVPECL, CMOS; PC; 400-ps PPU; VCXO; Ind; 3.3 V; 4-LCC (5 x 3.2)</td>
</tr>
<tr>
<td>CY25701</td>
<td>1-PLL; Max Freq: 166 MHz; 1 Output; CMOS; EMI; 85-ps CCJ; Ind; 3.3 V; 4-LCC (5 x 3.2)</td>
</tr>
<tr>
<td>CY2037/5037</td>
<td>1-PLL; Max Freq: 133 MHz; 1 Output; CMOS; 100-ps CCJ; Ind; 3.3/5.0 V; WAFER</td>
</tr>
<tr>
<td>CY2030/EPx</td>
<td>(Zero Delay) 2-2 Outputs; LVCMOS, LVDS, LVPECL; Freq Margining; 0.6-ps RMS Jitter; Ind; 1 Output; CMOS; 8/16-SOIC; 16-TSSOP; WAFER</td>
</tr>
<tr>
<td>CY2300/2300</td>
<td>(Non-Zero Delay) Max Freq: 220 MHz; 2-9 Outputs; LVCMOS; 2.5/3.3 V; 100-ps CCJ; Ind; Auto A; 8/16-SOIC; 16-TSSOP</td>
</tr>
</tbody>
</table>

### Timing Solutions

- Differential and single-ended outputs
- Voltage-controlled crystal oscillation
- Electromagnetic interference reduction using Lexmark profile
- Integrated phase noise across 12-kHz to 20-MHz offset
- Industrial grade: -40°C to +85°C
- AEC-Q100: -40°C to +85°C
- AEC-Q100: -40°C to +105°C
- Additive RMS phase jitter
- Power management options
- Cycle-to-cycle jitter
- Peak-to-peak period jitter
- AEC-Q100: -40°C to +125°C

### Status

- Concept
- Development
- Sampling
- Production
- EOL

### Availability

- Concept
- Development
- Sampling
- Production
- EOL
CY27410: High-Performance 4-PLL Clock Generator

**Applications**
Multifunction printers, digital TVs, Blu-ray recorders, home gateways, femtocells, routers and switches

**Features**
- **Twelve Outputs**
  - Eight configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0 and 10 GbE
  - Industrial temperature grade
- **Additional Features**
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency Select option to choose from eight pre-programmed configurations
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-Compliant Package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

**Datasheet**: 4-PLL High-Performance Clock Generator (CY274X)

**Four-PLL Spread-Spectrum Clock Generator**

**Availability**
Production: Now
CY2941x/2x: High-Performance 1-PLL Programmable Oscillator

**Applications**

Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

**Features**

- **Outputs**
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\) and CML\(^4\) outputs
- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Pin select and I\(^2\)C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40\(^\circ\)C to +105\(^\circ\)C)
- **RoHS-Compliant Packages**
  - Available in a 5 mm x 7 mm, 5 mm x 3.2 mm 8-pin LCC\(^9\) package

**Collateral**

Datasheet: [1-PLL High-Performance Programmable Oscillator (CY2941x/2x)](https://www.cypress.com)
CY29430: High-Performance 1-PLL Clock Synthesizer

**Applications**

Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

**Features**

- **Outputs**
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\), CML\(^4\) and LVCMOS outputs

- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 250 ppm
  - Frequency Select option to choose from four pre-programmed configurations
  - Pin select and I\(^2\)C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)

- **RoHS-Compliant Package**
  - Available in a 3 mm x 3 mm 16-pin QFN\(^6\) package

**Collateral**

Datasheet: [1-PLL High-Performance Clock Synthesizer (CY29430)](https://www.cypress.com/documents/1-PLL-High-Performance-Clock-Synthesizer-CY29430.pdf)

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\(^1\) Low-voltage positive emitter coupled logic
\(^2\) Low-voltage differential signaling
\(^3\) High-speed current steering logic
\(^4\) Current mode logic
\(^5\) The uncertainty of the clock rising and falling edge timing
\(^6\) I\(^2\)C input
\(^7\) Voltage input pin for VCFS
\(^8\) Frequency select inputs
\(^9\) Quad flat no-leads
Cypress Roadmap: Flash Memory
NOR Flash Memory Family
NOR Flash Memory Family Decoder

Technology:
- J = 110-nm Floating Gate (FG)
- K = 90-nm FG
- L = 65-nm FG
- M = 50-nm FG
- N = 110-nm MirrorBit® (MB)
- P = 90-nm MB
- R, S = 65-nm MB
- T = 45-nm MB

Density:
- 008 = 8Mb
- 016 = 16Mb
- 032 = 32Mb
- 064 = 64Mb
- 128 = 128Mb
- 256 = 256Mb
- 512 = 512Mb
- 01G = 1Gb
- 02G = 2Gb
- 04G = 4Gb

Voltage:
- D = 2.5 V
- L = 3.0 V
- S = 1.8 V

Family:
- A = Standard ADP (Address-Data Parallel)
- C = Burst Mode ADP (Address-Data Parallel)
- F = Serial
- G = Page Mode
- H = High-Performance Serial
- J = Simultaneous Read/Write ADP (Address-Data Parallel)
- K = HyperBus™
- N = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)
- P = Page Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- V = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)
- W = Burst Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- X = Burst Mode Simultaneous Read/Write AADM (Address-Address-Data Multiplexed)

Series:
- 25 = SPI
- 26 = HyperBus™
- 28 = Octal
- 35 = SPI with Security
- 36 = HyperBus™ with Security
- 38 = Octal with Security
- 29 = Parallel
- 70 = Stacked Die
- 79 = Dual Quad SPI

Prefix:
- S
## NOR Flash Memory Product Portfolio: New Products

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<tr>
<th>Family</th>
<th>Interface</th>
<th>Sector Size</th>
<th>Series</th>
<th>Voltage</th>
<th>Densities</th>
<th>Lead</th>
<th>Tech</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
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<th>2024</th>
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<td><strong>Semper™ Flash</strong></td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S25HS-T</td>
<td>1.8 V</td>
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<td>S26HL-T</td>
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<td>65-nm MB</td>
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<td>S25FL-L</td>
<td>3.0 V</td>
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<td>128–512Mb</td>
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<td>45-nm MB</td>
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*Legend:* Concept, Samples, Production, EOL
# x8 Serial NOR Flash Memory Roadmap

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<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
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<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<td>(Q2'20)³</td>
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<td>(Q1'20)¹</td>
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<td>256Mb</td>
<td>128Mb</td>
<td>512Mb</td>
<td>256Mb</td>
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<td>S26HL-T¹ (3.0 V)</td>
<td>1Gb¹</td>
<td>(TBD)</td>
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<td>128Mb</td>
<td>512Mb</td>
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<td>Semper Flash with HyperBus™ Interface 45-nm MB²</td>
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¹ JEDEC xSPI Compliant
² Hybrid Sector
³ Stacked Die
⁴ 1.8V Only
⁵ S79 Series (stacked die)

Products supported by Longevity Program unless noted

1. Concept
2. Samples
3. Production
4. EOL - LTB
5. EOL - LTS

48x20 Cypress Confidential Roadmap: Flash Memory (NDA)
### x8 Serial NOR Flash Memory Portfolio

<table>
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<tr>
<th>Product Family Number</th>
<th>Product Description</th>
<th>Technology</th>
<th>Temperature Range</th>
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<td>* I, A, V, B</td>
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<td>S26KL128S</td>
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<td>133 MHz/80 MHz</td>
<td>* I, A, V, B</td>
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### Dual Quad SPI

- **S79FL-S**: 65-nm MB, 3.0 V
- **S26KL-S**: 65-nm MB, 3.0 V
- **S26HL-S**: 45-nm MB, 3.0 V

### HyperFlash

- **S26KL**: 65-nm MB, 3.0 V
- **S26HL**: 45-nm MB, 3.0 V

### Semper™ Flash

- **S26HL**: 45-nm MB, 3.0 V
- **S26KL**: 65-nm MB, 3.0 V

### Semper Flash

- **S26HL**: 45-nm MB, 1.8 V
- **S26KL**: 65-nm MB, 1.8 V

### Status

- **Concept**: Ideas being explored.
- **Development**: Early development phase.
- **Sampling**: Samples available for testing.
- **Production**: Mass production.
- **EOL (Last-Time-Ship)**: End of life for all sales and repairs.

### Contact Information

- Contact Sales

---

1. Hybrid Sector
2. S79 series (stacked die)
3. HyperBus Interface (xSPI Profile 2.0)
4. Octal Interface (xSPI Profile 1.0)
5. Stacked die
6. Contact Sales

---

* I = Industrial: -40°C to +85°C
- A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
- V = Industrial-plus: -40°C to +105°C
- B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

---

124 Cypress Confidential Roadmap: Flash Memory (NDA)
# x4 Serial NOR Flash Memory Roadmap

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<td>Q2</td>
<td>Q3</td>
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<td>S25HL-T (3.0 V)</td>
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<td>(Q1’20)††</td>
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<td>QSPI</td>
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1 Hybrid Sector
2 QSPI 3.0V only in production
3 VIO 1.8 V to 3.0 V
4 Uniform Sector
5 S70 Series (stacked die)
6 S25FL127S & S25FL128S
7 Stacked die
8 FS-S only
9 Concept
10 Production
11 Samples
12 EOL - LTB
13 EOL - LTS

Products supported by Longevity Program unless noted.
## x4 Serial NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>SDR Clock/DDR Clock</th>
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<td>65-nm FG, 3.0 V</td>
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<td>S25HL-T^4</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
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<tr>
<td>S25HS-T^2</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
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<td>S25FS-S^3</td>
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<td>* I, A, V, B, M</td>
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<td>S25HL02GT^4</td>
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<td>* I, A, V, B, M</td>
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1 Uniform Sector  4 Stacked die
2 Hybrid Sector  5 S70 series (stacked die)
3 With QSPI  6 Contact Sales

* I = Industrial: -40°C to +85°C
  A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
  V = Industrial-plus: -40°C to +105°C
  B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
  M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

**EOL** (End-of-Life)
## Parallel NOR Flash Memory Roadmap

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<th>Density</th>
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<td>Q2</td>
<td>Q3</td>
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<td></td>
</tr>
<tr>
<td>S29AS-J (1.8 V)</td>
<td>110-nm FG</td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

1. Supports Page Mode
2. Supports simultaneous read/write operation
3. S70 series (stacked die)

### Notes
- Products supported by Longevity Program unless noted
  - Longevity Program:
    - Production: EOL - LTB
    - Samples: EOL - LTS

---

127 Cypress Confidential Roadmap: Flash Memory (NDA)
# Parallel NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial/Page Access</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S29AS-J</strong></td>
<td>110-nm FG, 1.8 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29AL-J</strong></td>
<td>110-nm FG, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29JL-J</strong></td>
<td>110-nm FG, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29PL-J</strong></td>
<td>110-nm FG, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29GL-N</strong></td>
<td>110-nm MB, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29GL-P</strong></td>
<td>90-nm MB, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29GL-S</strong></td>
<td>65-nm MB, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
<tr>
<td><strong>S29GL-T</strong></td>
<td>45-nm MB, 3.0 V</td>
<td>40°C to +85°C</td>
</tr>
</tbody>
</table>

### 256Mb

- **S29AS016J** 70 ns/— *I, A, N, M
- **S29AL016J** 55 ns/— *I, A, N, M
- **S29JL032J** 60 ns/20 ns *I, A
- **S29PL032J** 55 ns/20 ns *I, A
- **S29GL032N** 90 ns/25 ns *I, A

### 64–128Mb

- **S29AS016J** 70 ns/— *I, A
- **S29AL016J** 55 ns/— *I, A, N, M
- **S29JL064J** 60 ns/20 ns *I, A
- **S29PL064J** 55 ns/20 ns *I, A
- **S29GL064N** 90 ns/25 ns *I, A
- **S29GL256P** 90 ns/25 ns *I
- **S29GL256S** 90 ns/15 ns *I, A, V, B

### 32Mb

- **S29JL064J** 60 ns/20 ns *I, A
- **S29PL064J** 55 ns/20 ns *I, A
- **S29GL064N** 90 ns/25 ns *I, A
- **S29GL128P** 90 ns/15 ns *I, A, V, B
- **S29GL128S** 90 ns/15 ns *I, A, V, B

### S70 series

- **S70GL02GS** 110 ns/20 ns *I, A, V, B
- **S70GL02GT** 110 ns/20 ns *I, A, V, B, N
- **S29GL01GS** 100 ns/15 ns *I, A, V, B
- **S29GL01GT** 100 ns/15 ns *I, A, V, B, N
- **S29GL125S** 100 ns/15 ns *I, A, V, B
- **S29GL512T** 100 ns/15 ns *I, A, V, B, N

### Status

- Concept
- Development
- Sampling
- Production

**EOL** (Last-Time-Ship)

1. Supports simultaneous read/write operation
2. Supports Page Mode
3. S70 series (stacked die)

* = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
N = Extended: -40°C to +125°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
# Burst NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density (Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
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<tbody>
<tr>
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<td>90-nm MB</td>
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<tr>
<td></td>
<td>512Mb</td>
<td>256Mb</td>
<td>128Mb</td>
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<tr>
<td>S29NS-P(^2)</td>
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<td></td>
<td>512Mb</td>
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<tr>
<td>S29VS-R(^3)</td>
<td>65-nm MB</td>
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<tr>
<td></td>
<td>256Mb</td>
<td>128Mb</td>
<td>64Mb</td>
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<tr>
<td>S29XS-R(^4)</td>
<td>65-nm MB</td>
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<td></td>
<td>256Mb</td>
<td>128Mb</td>
<td>64Mb</td>
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</tr>
<tr>
<td>S29CD-J(^5)</td>
<td>110-nm MB</td>
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<td>32Mb</td>
<td>16Mb</td>
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<tr>
<td>S29CL-J(^5)</td>
<td>110-nm MB</td>
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<tr>
<td></td>
<td>32Mb</td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Address Data Parallel (ADP) Burst
2. Address high, Address low, Data Multiplex (AADM) Burst
3. Address Data Multiplex (ADM) Burst

*Products supported by Longevity Program unless noted*
### Burst NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial Access/SDR Clock</th>
<th>Temp Range</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29CL-J³</td>
<td>110-nm FG, 3.0 V</td>
<td>54 ns/66 MHz</td>
<td>* I, A, N, M, H, T</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
<tr>
<td>S29CD-J³</td>
<td>110-nm FG, 2.5 V</td>
<td>54 ns/66 MHz</td>
<td>* I, A, N, M, H, T</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
<tr>
<td>S29XS-R³</td>
<td>65-nm MB, 1.8 V</td>
<td>80 ns/108 MHz</td>
<td>* W, I</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
<tr>
<td>S29VS-R³</td>
<td>65-nm MB, 1.8 V</td>
<td>80 ns/108 MHz</td>
<td>* W, I</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
<tr>
<td>S29NS-P³</td>
<td>90-nm MB, 1.8 V</td>
<td>80 ns/104 MHz</td>
<td>* W</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
<tr>
<td>S29WS-P³</td>
<td>90-nm MB, 1.8 V</td>
<td>80 ns/104 MHz</td>
<td>* W</td>
<td>EOL (Last-Time-Ship)</td>
</tr>
</tbody>
</table>

- **Address Data Parallel (ADP) Burst**
- **Address high, Address low, Data Multiplex (AADM) Burst**
- **Address Data Multiplex (ADM) Burst**

* W = Wireless: -25°C to +85°C
* I = Industrial: -40°C to +85°C
* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
* N = Extended: -40°C to +125°C
* M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
* T = Automotive, AEC-Q100 Grade 0: -40°C to +150°C

**Legend**
- **Concept**
- **Development**
- **Sampling**
- **Production**

**Note:** All parts supported by Longevity Program unless noted.
# KGD/ KGW NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>HyperFlash 3.0 V</th>
<th>HyperFlash 1.8 V</th>
<th>Quad SPI 3.0 V</th>
<th>Quad SPI 1.8 V</th>
<th>Parallel 3.0 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product Family Number</td>
<td>Initial Access/DDR Clock</td>
<td>Initial/Page Access</td>
<td>SDR Clock/DDR Clock</td>
<td>Initial/Page Access</td>
</tr>
<tr>
<td>All parts supported by Longevity Program unless noted</td>
<td>* Temperature Range</td>
<td>* Temperature Range</td>
<td>* Temperature Range</td>
<td>* Temperature Range</td>
</tr>
</tbody>
</table>

- **S26KL512S**
  - 96 ns/100 MHz
  - * I, V, N

- **S26KL256S**
  - 96 ns/100 MHz
  - * I, V, N

- **S26KL128S**
  - 96 ns/100 MHz
  - * I, V, N

- **S26KL064L**
  - 108 ns/54 MHz
  - * I, V, N

- **S26KS512S**
  - 96 ns/166 MHz
  - * I, V, N

- **S26KS256S**
  - 96 ns/166 MHz
  - * I, V, N, M

- **S26KS128S**
  - 96 ns/166 MHz
  - * I, V, N, M

- **S26KS064S**
  - 108 ns/54 MHz
  - * I, V, N

- **S25FL512S**
  - 133 MHz/80 MHz
  - * I, V

- **S25FS256L**
  - 133 MHz/66 MHz
  - * I, V

- **S25FL128L**
  - 133 MHz/66 MHz
  - * I, V

- **S25FS128S**
  - 133 MHz/80 MHz
  - * I, V

- **S25FS064S**
  - 133 MHz/80 MHz
  - * I, V

- **S25FL064L**
  - 108 MHz/54 MHz
  - * I, V, N

- **S25FS051S**
  - 133 MHz/80 MHz
  - * I, V

- **S25FL016J**
  - 55 ns/—
  - * I, V, N

- **S29AL016J**
  - 55 ns/—
  - * I, V, N

- **S29GL01GS**
  - 100 ns/15 ns
  - * I, V

- **S29GL016S**
  - 100 ns/15 ns
  - * I, V

- **S29GL016S**
  - 90 ns/15 ns
  - * I, V

- **S29GLQ128S**
  - 90 ns/15 ns
  - * I, V

- **S29GLQ016J**
  - 100 ns/15 ns
  - * I, V

- **S29FLQ016J**
  - 55 ns/—
  - * I, V, N

### Notes:

- *I = Industrial: -40°C to +85°C
- V = Industrial-plus: -40°C to +105°C
- N = Extended: -40°C to +125°C
- M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

All temperature grades are T<sub>J</sub>.

**Contact Sales for KGD datasheets**

---

1 Contact Sales for KGD datasheets
Flash and RAM Memory MCP
# Flash and RAM Memory MCP Decoder

<table>
<thead>
<tr>
<th>S</th>
<th>71</th>
<th>N</th>
<th>512</th>
<th>S</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM Density:</td>
<td>A = 16Mb</td>
<td>B = 32Mb</td>
<td>C = 64Mb</td>
<td>D = 128Mb</td>
<td>E = 256Mb</td>
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<tr>
<td>Flash Density:</td>
<td>032 = 32Mb</td>
<td>128 = 128Mb</td>
<td>512 = 512Mb</td>
<td>064 = 64Mb</td>
<td>256 = 256Mb</td>
</tr>
<tr>
<td>Voltage:</td>
<td>L = 3.0 V</td>
<td>S = 1.8 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Family:</td>
<td>G = Page Mode</td>
<td>H = High-Performance Serial</td>
<td>K = HyperFlash</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>N = Burst Mode Simultaneous Read / Write Address-Data Multiplexed (ADM)</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V = Burst Mode Simultaneous Read / Write Address-Data Multiplexed (ADM)</td>
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<td></td>
<td>W = Burst Mode Simultaneous Read / Write Address-Data Parallel (ADP)</td>
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<td>X = Burst Mode Simultaneous Read / Write Address-Address-Data Multiplexed (AADM)</td>
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<tr>
<td>Series:</td>
<td>71, 98 = NOR Flash + pSRAM</td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>72 = NOR Flash + DRAM</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>76 = HyperBus Interface (xSPI Profile 2.0) NOR Flash + pSRAM</td>
<td></td>
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<tr>
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<td></td>
<td>78 = Octal Interface (xSPI Profile 1.0) NOR Flash + pSRAM</td>
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<tr>
<td>Prefix:</td>
<td>S</td>
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## Cypress Confidential Roadmap: Flash Memory (NDA)

### Serial Flash and RAM Memory MCP Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td><strong>S78HS-T (1.8 V)</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/64Mb</td>
<td>512Mb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
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<tr>
<td><strong>S76HS-T (1.8 V)</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
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<tr>
<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/64Mb</td>
<td>512Mb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>S71KS-S (1.8 V)</strong>&lt;sup&gt;3&lt;/sup&gt;</td>
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</tr>
<tr>
<td>65-nm HyperFlash/ HyperRAM</td>
<td>512Mb/64Mb</td>
<td>256Mb/64Mb</td>
<td>128Mb/64Mb</td>
<td>(TBD)</td>
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<tr>
<td><strong>S78HL-T (1.8 V)</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
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<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/64Mb</td>
<td>512Mb/64Mb</td>
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<tr>
<td><strong>S76HL-T (1.8 V)</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
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<tr>
<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/64Mb</td>
<td>512Mb/64Mb</td>
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<tr>
<td><strong>S71KL-S (3.0 V)</strong>&lt;sup&gt;3&lt;/sup&gt;</td>
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<tr>
<td>65-nm HyperFlash/ HyperRAM</td>
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<td>256Mb/64Mb</td>
<td>128Mb/64Mb</td>
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1. Octal Interface (xSPI Profile 1.0)
2. HyperBus Interface (xSPI Profile 2.0)
3. HyperBus Interface

*Products supported by Longevity Program unless noted*
<table>
<thead>
<tr>
<th>Product Family</th>
<th>Flash / RAM Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
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<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td>S98GL-N (3.0 V)</td>
<td>110-nm MB/pSRAM</td>
<td>64Mb/32Mb</td>
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<tr>
<td>S72XS-R (1.8 V)</td>
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<td>256Mb/256Mb</td>
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<td>S72VS-R (1.8 V)</td>
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<tr>
<td>S71VS-R (1.8 V)</td>
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<td>128Mb/64Mb</td>
<td>128Mb/32Mb</td>
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<td></td>
<td>64Mb/32Mb</td>
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<tr>
<td>S71NS-P (1.8 V)</td>
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<td>512Mb/128Mb</td>
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<tr>
<td>S71WS-P (1.8 V)</td>
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<td>256Mb/64Mb</td>
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Products supported by Longevity Program unless noted.

- **Samples**
- **Production**
- **EOL - LTB**
- **EOL - LTS**
## Serial Flash and RAM Memory MCP Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>RAM Density</th>
<th>Temperature Range</th>
<th>Status</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>S71KL-S 65-nm MB, 3.0 V</td>
<td>All parts supported by Longevity Program unless noted</td>
<td>-</td>
<td>Concept</td>
<td>EOL (Last-Time-SHIP)</td>
</tr>
<tr>
<td>S76HL-T 45-nm MB, 3.0 V</td>
<td>S76HL01GTC² 64Mb⁴ * I, A, V, B</td>
<td>-</td>
<td>Sampling</td>
<td></td>
</tr>
<tr>
<td>S78HL-T 45-nm MB, 3.0 V</td>
<td>S78HL01GTC² 64Mb⁴ * I, A, V, B</td>
<td>-</td>
<td>Development</td>
<td></td>
</tr>
<tr>
<td>S71KS-S 65-nm MB, 1.8 V</td>
<td>S71KS512SC¹ 64Mb⁴ * I, A, V, B</td>
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<td>S76HS-T 45-nm MB, 1.8 V</td>
<td>S76HS1GTC² 64Mb⁴ * I, A, V, B</td>
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<td>EOL (Last-Time-SHIP)</td>
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1. HyperFlash
2. HyperBus Interface (xSPI Profile 2.0)
3. Octal Interface (xSPI Profile 1.0)
4. HyperRAM™
## Parallel Flash and RAM Memory MCP Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>RAM Density</th>
<th>Temperature Range</th>
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<td>S71WS-P^1</td>
<td>64–128Mb</td>
<td>* W</td>
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<td>S71NS-P^2</td>
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<td>S71VS-R^3</td>
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<td>S72XS-R^5</td>
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<td>S98GL-N^6</td>
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<td>* W</td>
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### Product Examples

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<td>S71VS256RC</td>
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<td>S72XS256RE</td>
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### Notes

1. Address Data Parallel (ADP) Burst
2. Address Data Multiplex (ADM) Burst
3. Address High, Address Low, Data Multiplex (AADM) Burst
4. Parallel, Page Mode
5. DRAM Version 2
6. DRAM Version 1
* W = Wireless: -25°C to +85°C
I = Industrial: -40°C to +85°C

### Status

- **EOL (Last-Time-Ship)**
- **Concept**
- **Development**
- **Sampling**
- **Production**
Aerospace and Military Family
NOR Flash Memory Family Decoder

**Aerospace**

- **CYRS 16 B 512**
  - **Density:** 256 = 256Mb 512 = 512Mb
  - **Voltage:** B = 3.0 V
  - **Technology:** 16 = 65 nm Floating Gate Process Technology
  - **Family:** CYRS = Cypress RadStop

**Military**

- **S 25 F L 512 S**
  - **Technology:** S = 65-nm MB
  - **Density:** 064 = 64Mb 128 = 128Mb 256 = 256Mb 512 = 512Mb 01G = 1Gb 02G = 2Gb 04G = 4Gb
  - **Voltage:** L = 3.0 V
  - **Family:** F = Serial  G = Page Mode
  - **Series:** 25 = SPI  29 = Parallel  70 = Stacked Die  79 = Dual Quad SPI
  - **Prefix:** S
Aerospace¹, ², ³ and Military⁴ Memory Portfolio

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<th>Military Serial I/O, ECC</th>
<th>Military Parallel I/O, ECC</th>
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<td>3.0 V</td>
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¹ Radiation Hardened
² Latch-up Immune
³ Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
⁴ Single-Event Latch-Up Immune
⁵ AEC-Q100 Grade 1

* E = Military: -55°C to +125°C
  M = Automotive: -40°C to +125°C

Status: Concept, Development, Sampling, Production
Availability: EOL (Last-Time-Ship)
Package Offerings
### x8 Serial Memory Packages

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<th>Device</th>
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1. Octal Interface (xSPI Profile 1.0)
2. HyperBus Interface (xSPI Profile 2.0)
3. HyperBus Interface

CF = Contact Factory
UD = Under Development
## x4 Serial NOR Flash Memory Packages

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<th>Family</th>
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CF = Contact Factory  
UD = Under Development
## Parallel NOR Flash Memory Packages

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<th>48-Ball FBGA (0.8-mm pitch)</th>
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<th>64-Ball Fortified BGA (1.0-mm pitch)</th>
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## Burst NOR Flash Memory Packages

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## Flash and RAM Memory MCP Packages

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Military Memory Portfolio
## Military Memory Portfolio

### Military Memory | Single-Event Latch-Up Immune

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<tr>
<th>Fast Async SRAM</th>
<th>Sync SRAM</th>
<th>Nonvolatile SRAM</th>
<th>F-RAM™</th>
<th>NOR Flash</th>
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<tr>
<td>ECC¹</td>
<td>NoBL², ECC</td>
<td>QDR⁵/IV</td>
<td>Serial/Parallel I/O</td>
<td>Serial/Parallel I/O, ECC</td>
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<td>CY7C41xKV13</td>
<td>144Mb; 667–1066 MHz, 1.3 V, x18/x36, Burst 2, M⁶</td>
<td>CY7C144/6xK</td>
<td>36Mb; 133–250 MHz, 2.5 V/3.3 V, x18/x36, M</td>
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<td>CY7C106x</td>
<td>16Mb, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M</td>
<td>CY7C144/4xK</td>
<td>36Mb, 133–250 MHz, 2.5 V/3.3 V, x18/x36, M</td>
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<td>8Mb, 1.8–5.0 V, 10 ns, x8/x16/x32, Auto E, M</td>
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1 Error-correcting code  
2 No Bus Latency  
3 Quad Data Rate  
4 Military Temperature: −55℃ to +125℃  
5 AEC-Q100 -40℃ to +125℃  
6 Real-time clock  
7 Qualified Manufacturers List Level Q, per MIL-PRF-38535  
8 Military Temperature: −55℃ to +125℃  
9 Qualified Manufacturers List Level Q, per MIL-PRF-38535

### Status

- **EOL (Last-Time-Ship)**
- **Production**
- **Sampling**
- **Development**
- **Concept**

---

*148 MILITARY MEMORY – HRP*
256Kb/1Mb Military nvSRAM

Applications
Military communication and real-time controls, avionics real-time controls and high-reliability data logging

Features
- Fast Nonvolatile Memory
  - Access time 35 ns
  - Available in parallel interface for 256Kb and 1Mb densities
  - Unlimited read/write endurance
  - One million store cycles on power fail
- Specifications
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- Packages: Ceramic 32-pin DIP

Collateral
Datasheet: Contact Sales (Available Now)

Availability
Production: Now

1 External capacitor connection
2 Hardware STORE busy
72Mb QDR®1-II+ SRAM

Applications
Payload processing and reconfigurable computing platforms

Features
- High Performance Memory
  - Maximum frequency of operation/throughput: 250 MHz/36 Gbps
  - Two independent unidirectional data ports for read and write enable concurrent transactions
  - Maximum throughput with double data rate (DDR) data ports
  - Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
  - Bit-interleaving to eliminate multi-bit errors
  - I/O signaling standards: 1.5–1.8 V (HSTL)
- Specifications
  - Burst sizes: 2 or 4
  - Bus-width configurations: x18 or x36
  - Military temperature grade: -55°C to +125°C
- Controllers available for Altera/Xilinx/Microsemi FPGAs
- Package: 165-pin CCGA2

Collateral
Datasheets: CYPT1542AV18/CYPT1544AV18
          CYPT1543AV18/CYPT1545AV18

Availability
Production: Now

1 Quad Data Rate: Four data transfers per clock cycle
2 Ceramic column grid array package
QDR®-IV SRAM

Applications
Switches and routers, high-performance computing, test equipment, military and aerospace systems

Features
- Highest Performance Memory
  - Available in two options: High Performance (RTR 1334 MT/s) and Extreme Performance (RTR 2132 MT/s)
  - Two independent, bidirectional double data rate (DDR) data ports
  - Error-correcting code (ECC) to detect and correct single-bit errors (<0.01 FIT/Mb)
  - On-die termination (ODT) to reduce board complexity
  - De-skew training to improve signal-capture timing
- Specifications
  - I/O Levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD)
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- RoHS-Compliant Package
- Package: 361-ball flip-chip ball grid array (FCBGA)

Collateral
Datasheets: CY7C4121KV13/CY7C4141KV13

Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>Maximum Frequency</th>
<th>RTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDR-IV HP</td>
<td>72Mb</td>
<td>CY7C40x1KV13</td>
<td>667 MHz</td>
<td>1,334 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x1KV13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-IV XP</td>
<td>72Mb</td>
<td>CY7C40x2KV13</td>
<td>1,066 MHz</td>
<td>2,132 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x2KV13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

QDR-IV

Address/Control Clock

Bus Inversion

Address Port

Address Parity

Parity Error

Data Clocks

Data Valid

Data Port A

(HSTL/SSTL or POD)

Address Interface

ECC

SRAM Array

Data Port B

(HSTL/SSTL or POD)

Data Clocks

Data Valid

Data Port B

(HSTL/SSTL or POD)

Data Port A

(HSTL/SSTL or POD)

ODT

Control Logic

Test Engine

Impedance Matching

Control

JTAG Interface

Availability
Production: Now

Footnotes:
1 Two data transfers per clock cycle
2 The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
3 An iterative algorithm for assessing and eliminating the skew (differences in arrival times) between data signals
4 Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up
Synchronous SRAM with On-Chip ECC

Applications
Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features
- **New Features**
  - Available in two modes\(^1\): Pipeline and Flow-Through
  - SCD and DCD deselect options\(^2\)
  - Error-correcting code (ECC) to detect and correct single-bit errors
- **Specifications**
  - Voltage options: 2.5 V and 3.3 V
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55\(^\circ\)C to +125\(^\circ\)C
- **Packages**: 165-ball BGA (w/ and w/o leaded balls) and 100-pin TQFP

Collateral
**Datasheets:** CY7C135XKV33/CY7C136XKV33
CY7C137XKV33/CY7C138XKV33
CY7C144XKV33/CY7C146XKV33

Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb(^3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with ECC Pipeline</td>
<td>9Mb/18Mb/36Mb</td>
<td>CY7C1360/2K/CY7C1370/2K/CY7C1440/2K</td>
<td>250 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Standard Sync with ECC Flow-Through</td>
<td>9Mb/18Mb/36Mb</td>
<td>CY7C1361/3K/CY7C1371/3K/CY7C1441/3K</td>
<td>133 MT/s</td>
<td>&lt;0.01</td>
</tr>
</tbody>
</table>

Availability
Production: Now

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\(^1\) Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)

\(^2\) Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command

\(^3\) The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
Fast SRAM Family with PowerSnooze

**Applications**
Programmable logic controller, handheld devices, multifunction printers, computation servers and automotive

**Features**
- Error Detection and Correction
  - Error-correcting code (ECC) logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- Specifications
  - Access time: 10 ns
  - Deep-sleep current: 15 µA for 4Mb
  - Bus-width configurations: x8, x16, and x32
  - Industrial and automotive temperature grades
  - Military temperature grade: -55°C to +125°C
- Packages: 48-ball BGA (w/ and w/o leaded balls)

**Collateral**
Datasheets: CY7S1049G/CY7C1049G
CY7S1051H/CY7C1051H
CY7S1061G/CY7C1061G

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>10 ns</td>
<td>15 µA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY7S105x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
</tbody>
</table>

**Fast SRAM with PowerSnooze**

**Availability**
Production: Now

1 A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
16Mb Parallel nvSRAM

**Applications**
Industrial automation, programmable logic controllers, gaming machines, industrial data logging, telecom equipment, networking and storage

**Features**
- Fast Nonvolatile Memory
  - Access time (25 ns)
  - Optional real-time clock (RTC) functionality
  - Available in parallel and open NAND Flash Interface (ONFI) Version 1.0 interfaces
  - Unlimited read/write endurance
  - One million store cycles on power fail
- Specifications
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- Packages: 44-pin TSOP, 54-pin TSOP, 165-ball BGA (w/ and w/o leaded balls)

**Collateral**
Datasheet: CY14X116L/CY14X116N/CY14X116S

**Availability**
Sampling: Now
Production: Contact Sales

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1 Crystal connection input
2 Crystal connection output
3 Interrupt output/calibration/square wave
4 External capacitor connection
5 Hardware STORE busy
2Mb / 1Mb Military SPI F-RAM

Applications
Multifunction printers, industrial controls and automation, medical wearables, test and measurement equipment, smart meters, aerospace and defense applications, missiles and launchers

Features
- Ultra-Low Power Memory
  - 40-MHz SPI interface
  - 100-trillion read/write cycle endurance
- Specifications
  - Operating voltage range: 2.0–3.6 V
  - Low (20-µA) sleep current at +125°C
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- Packages: 8-pin TDFN and 8-pin SOIC

Collateral
Datasheet: CY15B102Q

Availability
Sampling: Now (1Mb)
Production: Now (2Mb) / Q4’19 (1Mb)
64Mb/128Mb/256Mb/512Mb/1Gb/2Gb Parallel NOR Flash

**Applications**
- Military systems boot memory
- Avionics boot memory

**Features**
- **High-Reliability Boot Flash Memory**
  - 100 program\1\sector erase\2\ endurance cycles\3\ at +125°C
  - >10 years data retention at +125°C

- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Initial access time: 120 ns
  - Page access time: 15 ns
  - Program time (512B): 0.4 ms (typical)
  - Sector erase time (128KB): 410 ms (typical)
  - Military temperature grade: -55°C to +125°C

- **Packages:** 64-ball fortified\4\ BGA (9 x 9 mm and 13 x 11 mm, w/ and w/o leaded balls)

**Collateral**

**Datasheet:** [S29GLXXXS](#) (128M/256M/512M/1G)

**Availability**
- **Samples:** Now (1Gb, 2Gb, 64Mb)
- **Production:** Now (128Mb/256Mb/512Mb) / Q4’19 (1Gb) / Q4’19 (2Gb) / Q4’19 (64Mb)

1. The operation required to change a NOR Flash memory cell state from “1” to “0”
2. The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
3. The number of times a NOR Flash memory sector can be programmed or erased before it wears out
4. Fortified BGA supports a 1-mm ball pitch
5. Write protect input
6. Ready/busy output

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128Mb/256Mb/512Mb/1Gb SPI NOR Flash

**Applications**
- Military systems boot memory
- Avionics boot memory

**Features**
- **High-Reliability Boot Flash Memory**
  - 100 program\(^1\)/sector erase\(^2\) endurance cycles\(^3\) at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Single data rate (SDR)\(^4\) clock rate: 104-MHz quad input/output (QIO)\(^5\)
  - Double data rate (DDR)\(^6\) clock rate: 80-MHz QIO
  - Program time (512B): 0.340 ms (typical)
  - Sector erase time (256KB): 520 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages**: 24-ball BGA (6 x 8 mm, w/ and w/o leaded balls)

**Collateral**
- Datasheets: [S25FL512S](#) (512Mb)
  - [S25FL128/256S](#) (128Mb/256Mb)

**Availability**
- Sampling:Now (1Gb)
- Production:Now (128/256/512Mb) / Q4'19 (1Gb)

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1 The operation required to change a NOR Flash memory cell state from “1” to “0”
2 The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously
3 The number of times a NOR Flash memory sector can be programmed/erased before it wears out
4 A mode of data transfer in which data is transferred once per clock cycle
5 An interface that transfers addresses or data on four I/O’s simultaneously
6 A mode of data transfer in which data is transferred twice per clock cycle
7 Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
8 \(^*\)RESET\(^*\) is an optional signal available on 16-pin SOIC and BGA packages.
Aerospace Memory Portfolio
# Aerospace Memory Portfolio

Radiation Hardened | Latch-up Immune | QML-V¹ Certified

<table>
<thead>
<tr>
<th>Fast Async SRAM</th>
<th>Sync SRAM</th>
<th>Nonvolatile NOR</th>
<th>FRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-ECC²</td>
<td>ECC²</td>
<td>QDR®-II+/IV</td>
<td>Serial I/O</td>
</tr>
<tr>
<td>CYRS104x</td>
<td>4Mb; 3.3 V</td>
<td>12 ns; x8</td>
<td></td>
</tr>
<tr>
<td>CYRS106x</td>
<td>16Mb; 1.8-5.0 V</td>
<td>10 ns; x8, x16, x32</td>
<td></td>
</tr>
<tr>
<td>CYRS108x</td>
<td>64Mb; 1.8-5.0 V</td>
<td>12 ns; x8, x16, x32</td>
<td></td>
</tr>
<tr>
<td>CYRS264x</td>
<td>144Mb; 1.8 V; 250 MHz</td>
<td>x18, x36; Burst 2,4</td>
<td></td>
</tr>
<tr>
<td>CYRS274x</td>
<td>288Mb; 1.8 V; 250 MHz</td>
<td>x18, x36; Burst 2,4</td>
<td></td>
</tr>
<tr>
<td>CYRS4141x</td>
<td>144Mb; 1.2 V; 667 MHz</td>
<td>x18, x36; Burst 2</td>
<td></td>
</tr>
<tr>
<td>CYRS104x</td>
<td>4Mb; 3.3 V</td>
<td>12 ns; x8</td>
<td></td>
</tr>
<tr>
<td>CYRS106x</td>
<td>16Mb; 1.8-5.0 V</td>
<td>10 ns; x8, x16, x32</td>
<td></td>
</tr>
<tr>
<td>CYRS108x</td>
<td>64Mb; 1.8-5.0 V</td>
<td>12 ns; x8, x16, x32</td>
<td></td>
</tr>
<tr>
<td>CYRS264x</td>
<td>144Mb; 1.8 V; 250 MHz</td>
<td>x18, x36; Burst 2,4</td>
<td></td>
</tr>
<tr>
<td>CYRS104x</td>
<td>4Mb; 3.3 V</td>
<td>12 ns; x8</td>
<td></td>
</tr>
</tbody>
</table>

1 Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
2 Error-correcting code

---

159 AEROSPACE MEMORY – HRP
72Mb QDR®-II+ SRAM with RadStop™

Applications
Payload processing and reconfigurable computing platforms

Features
- Maximum frequency of operation/throughput: 250 MHz/36 Gbps
- Burst sizes: 2, 4
- Bus-width configurations: x18, x36
- Military temperature grade: -55°C to +125°C
- Two independent unidirectional data ports for read/write enable concurrent transactions
- Maximum throughput with double data rate (DDR) data ports
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Bit-interleaving to eliminate multi-bit errors
- I/O signaling standards: 1.5 – 1.8 V (HSTL)
- Controller available for Xilinx and Microsemi FPGAs
- Total ionizing dose: 300 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg
- Heavy-ION single-event upset (SEU): 1.34E-07 (geosynchronous) error/bit-day
- QML-V²-qualified (DLAM³ part number: 5962F11201/02VXA)

Availability
Non-Space-Qualified Prototypes (CYPT154x): Now
QML-V Space-Qualified Devices (CYRS154x): Now

Collateral
Cypress Datasheet: 72-Mbit SRAMs w/ RadStop™
DLAM Datasheet: 72-Mbit SRAMs w/ RadStop

1 Cypress’s proprietary design and process technology that increases radiation-resistance
2 Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
3 Defense Logistics Agency Land and Maritime, Columbus, OH
144Mb QDR®-II+ SRAM with RadStop™1

Applications
Payload processing and reconfigurable computing platforms

Features
- Maximum frequency of operation/throughput: 250 MHz/36 Gbps
- Burst sizes: 2, 4
- Bus-width configurations: x18, x36
- Military temperature grade: −55°C to +125°C
- Two independent unidirectional data ports for read/write enable concurrent transactions
- Maximum throughput with double data rate (DDR) data ports
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Featuring On-Die-Termination
- I/O signaling standards: 1.5 –1.8 V (HSTL)
- Controller available for Xilinx and Microsemi FPGAs
- Total ionizing dose: 200 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg
- Heavy-ION single-event upset (SEU): 3.34E-07 (geosynchronous) error/bit-day
- QML-V²-qualified (DLAM³ part number: 5962R18214VXF/18215VXF)

Availability
Non-Space-Qualified Prototypes (CYPT264x/164x): Now
QML-V Space-Qualified Devices (CYRS264x/164x): Now

Collateral
Cypress Datasheet: Release pending
DLAM Datasheet: Release pending

1 Cypress’s proprietary design and process technology that increases radiation-resistance
2 Qualified Manufacturers List Level V, per military specification MIL-PRF-38535
3 Defense Logistics Agency Land and Maritime, Columbus, OH
### 4Mb Fast SRAM with RadStop™

#### Applications
Payload processing, sensors and switches

#### Features
- Access time: 10 ns (85°C), 12 ns (125°C)
- Bus-width configuration: x8
- Operating voltage: 3.3 V
- Military temperature grade: −55°C to +125°C
- Bit-interleaving to eliminate multi-bit errors
- Package: 36-pin ceramic flat pack (CFP)
- Total ionizing dose: 300 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm²/mg
- Heavy-ION single-event upset (SEU): 5.0E-08 (geosynchronous) error/bit-day
- QML-V qualified (DLAM part number: 5962F1123501VXC)

#### Collateral
- Cypress Datasheet: [4-Mbit SRAM w/ RadStop™](#)
- DLAM³ Datasheet: [4-Mbit SRAM w/ RadStop](#)

#### Availability
- Non-Space-Qualified Prototypes (CYPT1049): Now
- QML-V Space-Qualified Devices (CYRS1049): Now

---

**Diagram:**

CYRS1049DV33: Radiation Hard 4M Fast Asynchronous SRAM

- **Fast SRAM**
- **Address Decoder**
- **SRAM Array**
- **Sense Amps**
- **IO MUX**
- **Address Port** x18
- **Data Port** x8
- **Control Logic**
- CE
- OE
- WE

---

**Notes:**

- [4-Mbit SRAM w/ RadStop™](#)
- [4-Mbit SRAM w/ RadStop](#)
Energy Harvesting PMIC Portfolio
# Energy Harvesting PMIC Portfolio

<table>
<thead>
<tr>
<th>Wearable Activity Monitor</th>
<th>Residential WSNs^2 for HVAC^3, Level of Light Emitted, Temperature, Humidity, Motion</th>
<th>Building WSNs for HVAC, Level of Light Emitted, Temperature, Humidity, Motion, BLE^4 Beacon^5</th>
<th>Industrial WSNs for Infrastructure, Agriculture, Transportation, Factory Automation, Animal Monitoring</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Light Series Solar Cell</strong></td>
<td><strong>S6AE101A</strong> Linear, Power Gating^6, Multiplexer^7, 10-pin QFN</td>
<td><strong>S6AE102A</strong> Linear, Power Gating, Multiplexer, LDO^8, Comparator, 20-pin QFN</td>
<td><strong>S6AE103A</strong> Linear, Power Gating, Multiplexer, LDO, Timer, Comparator, 24-pin QFN</td>
</tr>
<tr>
<td><strong>Single Solar Cell</strong></td>
<td><strong>S6AE101A</strong> Linear, Power Gating, Multiplexer, 10-pin QFN</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Heat Thermoelectric Generator (TEG)</strong></td>
<td></td>
<td></td>
<td><strong>CY39C831</strong> Boost DC/DC, MPPT^9, Li-ion Protection, 40-pin QFN</td>
</tr>
<tr>
<td><strong>Series Solar Cell by Panasonic (AM-1801)</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>Single Solar Cell by Ningbo Hebe Solar (HSC125155)</strong></td>
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<tr>
<td><strong>TEG by Micropelt (TGP-651)</strong></td>
<td></td>
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</tr>
</tbody>
</table>

## Materials

- **Power Management IC**: S6AE101A, S6AE102A, S6AE103A
- **Wireless sensor nodes**: CY39C831
- **Heating, ventilation, air conditioning (HVAC)**
- **Bluetooth Low Energy (BLE)**

## Market Segment

- **Indoor/Outdoor**
- **Indoor**
- **Outdoor**

## Status Availability

<table>
<thead>
<tr>
<th>Concept</th>
<th>Development</th>
<th>Sampling</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>QQYY</td>
<td>QQYY</td>
<td>QQYY</td>
<td>QQYY</td>
</tr>
</tbody>
</table>

## Notes

1. Power Management IC
2. Wireless sensor nodes
3. Heating, ventilation, air conditioning
4. Bluetooth Low Energy
5. A wireless device that transmits data (e.g., signal strength and ID) over a periodic radio signal from a known location
6. Output power control circuit that controls power provided to the system load
7. Power source switch circuit for primary battery or energy harvesting device
8. Low dropout regulator
9. Maximum power point tracking
S6AE101A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications
Series solar cell energy harvesting\(^1\) and wireless sensor nodes\(^2\)

Features
- Ultra-Low Power
  - Enables 1 cm\(^2\) minimum solar cell size for startup operation\(^3\)
- Input Voltage Range
  - 2.0–5.5 V (series solar cell and primary battery)
- 1.1–5.2-V Output Voltage Range
- 250-nA Quiescent Current\(^4\)
- 1.2-µW Startup Power
- Power Gating\(^5\) Switch Circuit
- Storage Control Circuit
- Multiplexer\(^6\) Circuit (battery vs. solar cell)
- Overvoltage Protection (OVP)
- Packages
  - 3.0 mm x 3.0 mm 10-pin SON

Collateral
Datasheet: S6AE101A Datasheet
Development Kits: Solar-Powered IoT Device Kit
S6AE10xA Evaluation Board

Availability
Production: Now

S6AE101A: Solar-Optimized Energy Harvesting PMIC

1 The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
2 A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
3 Estimate based on solar cell power = 2 µW/cm\(^2\) at 100 lx
4 Current consumed at no load condition
5 Output power control circuit that controls power provided to the system load
6 Power source switch circuit for primary battery and Energy Harvesting Device
7 Voltage reference circuit for internal block
S6AE102A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications
- Series solar cell energy harvesting\(^1\) and wireless sensor nodes\(^2\)

Features
- **Ultra-Low Power**
  - Enables 1 cm\(^2\) minimum solar cell size for startup operation\(^3\)
- **Input Voltage Range**
  - Series solar cell: 2.0–5.5 V (series solar cell and primary battery)
  - 1.1–5.2 V Output Voltage Range
- **280-nA Quiescent Current**\(^4\)
- **1.2-µW Startup Power**
- **400-nA Low Quiescent Current Low Dropout Regulator (LDO)**
- **Dual-Channel Power Gating\(^5\) Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management**
- **Signal Output Circuit of Power Gating Switch Control**
- **Multiplexer\(^6\) Circuit (battery vs. solar cell)**
- **Hybrid Storage Control Circuit\(^7\) and Overvoltage Protection (OVP)**
- **Packages**
  - 4.0 mm x 4.0 mm 20-pin QFN

Collateral
- **Datasheet:** [S6AE102A Datasheet](#)
- **Development Kits:** [S6AE10xA Evaluation Board, CYALKIT-E04](#)

Availability
- **Production:** Now

---

\(^1\) The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
\(^2\) A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
\(^3\) Estimate based on solar cell power = 2 µW/cm\(^2\) at 100 lx
\(^4\) Current consumed at no load condition
\(^5\) Output power control circuit that controls power provided to the system load
\(^6\) Power source switch circuit for primary battery or series solar cell
\(^7\) Uses a small and large capacitor to automatically store excess power for backup
\(^8\) Voltage reference circuit for internal block
S6AE103A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications
Series solar cell energy harvesting\(^1\) and wireless sensor nodes\(^2\)

Features
- **Ultra-Low Power**
  - Enables 1 cm\(^2\) minimum solar cell size for startup operation\(^3\)
- **Input Voltage Range**
  - 2.0-5.5 V (series solar cell and primary battery)
- **Output Voltage Range**
  - 1.1-5.2 V
- **280 nA Quiescent Current\(^4\)**
- **1.2 µW Startup Power**
- **400 nA Low Quiescent Current Low Dropout Regulator (LDO)**
- **30 nA Low Consumption Current CR Timer\(^5\)**
- **20 nA General-Purpose Low Consumption Current Comparator**
- **Dual-Channel Power Gating\(^6\)** Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management
- **Signal Output Circuit of Power Gating Switch Control**
- **Multiplexer\(^7\)** Circuit (battery vs. solar cell)
- **Hybrid Storage Control Circuit\(^8\)** and Overvoltage Protection (OVP)
- **Packages**
  - 4.0 mm x 4.0 mm 20-pin QFN

Collateral
Datasheet: [S6AE103A Datasheet](#)
Development Kits: [S6AE10xA Evaluation Board, CYALKIT-E04](#)

Availability
Production: Now

---

\(^1\) The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity

\(^2\) A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device

\(^3\) Estimate based on solar cell power = 2 µW/cm\(^2\) at 100 lx

\(^4\) Current consumed at no load condition

\(^5\) Output power control circuit that controls power provided to the system load

\(^6\) Power source switch circuit for primary battery or series solar cell

\(^7\) Uses a small and large capacitor to automatically store excess power for backup

\(^8\) Voltage reference circuit for internal block
**CY39C831**

**General Purpose Energy Harvesting Power Management IC (PMIC)**

**Applications**
- Single solar cell energy harvesting, thermoelectric generator energy harvesting and wireless sensor nodes

**Features**
- Ultra-Low-Voltage Startup Boost DC/DC Converter
- 0.3–4.75-V Input Voltage Range
- 0.35-V Startup Voltage
- Output Voltage (constant voltage mode only)
  - 3.0 V, 3.3 V, 3.6 V, 4.1 V, 4.5 V and 5.0 V
- 32-µA Quiescent Current
- Output Current
  - 8 mA ($V_{DD} = 0.6$ V, $V_{OUT} = 3.3$ V) and 80 mA ($V_{DD} = 3.0$ V, $V_{OUT} = 3.3$ V)
- 200-mA Input Peak Current Limit
- Built-In Maximum Power Point Tracking (MPPT) Function
- Built-In Li-ion Charge Function
- Input and Output Power Good Monitoring
- Package
  - 6.0 mm x 6.0 mm 40-pin QFN

**Collateral**

- **Datasheet:** [CY39C831 Datasheet](#)
- **Development Kits:** [CY39C831 Evaluation Board](#)

**Availability**

- **Production:** Now

---

1. The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
2. Power Generation Device using heat
3. A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
4. Current consumed at no load condition
5. Maximum Power Point Tracking maximizes the Energy Harvest by adjusting current drawn from a solar panel
6. Undervoltage lockout
7. Band Gap Reference
Cypress Roadmap: Automotive Products
# Cypress Automotive Roadmaps Slide Index

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HMI Solutions Automotive Roadmaps
Automotive TrueTouch® Roadmap
## Automotive Portfolio: TrueTouch®

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<td>Gestures, AMS&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Hover, Haptic/Acoustic Feedback, LPWUB&lt;sup&gt;6&lt;/sup&gt;, Force Touch&lt;sup&gt;6&lt;/sup&gt;, TCPWM, I&lt;sup&gt;2&lt;/sup&gt;S, CAN, Crypto</td>
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<tr>
<td>Thick Glove&lt;sup&gt;3&lt;/sup&gt; or Thick Overlay</td>
<td>In-Cell, Gestures, AMS Thick Glove&lt;sup&gt;4&lt;/sup&gt;or Thick/Curved Overlay</td>
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**Touchscreen, 10 Finger, AutoArmor<sup>7</sup>™, DualSense<sup>8</sup>™, H<sub>2</sub>O<sup>9</sup>, Glove Touch<sup>10</sup>, Grades: A<sup>11</sup> and S<sup>12</sup>**

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
<th>Qty</th>
<th>Qty</th>
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<td>88 I/O, 100-Hz RR</td>
<td>Q419</td>
<td>Q419</td>
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<td>CYAT8268X</td>
<td>54 RX&lt;sup&gt;13&lt;/sup&gt;, 100-Hz RR</td>
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<tr>
<td>CYAT8168X</td>
<td>77/71 I/O, 120-Hz RR</td>
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<td>61 I/O, 120-Hz RR</td>
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<td>48 I/O, 100-Hz RR</td>
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<td>77/61 I/O, 120-Hz RR</td>
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</table>

<sup>1</sup> Automatic Mode Switching  
<sup>2</sup> 1-mm to 5-mm glove thickness (ski gloves)  
<sup>3</sup> A type of sensor stack-up in which the RX sensor is inside the LCD module under the color-filter glass  
<sup>4</sup> Less than 1-mm glove thickness (normal leather gloves)  
<sup>5</sup> Low-power wake-up button  
<sup>6</sup> The ability of touchscreen to distinguish between different levels of force being applied on the touchscreen  
<sup>7</sup> Enables compliance with chip-level emission, immunity and system-level specifications  
<sup>8</sup> Self-Capacitance + Mutual-Capacitance  
<sup>9</sup> Waterproofing and wet-finger tracking  
<sup>10</sup> A feature that allows the detection of gloved fingers on a touch sensor  
<sup>11</sup> AEC-Q100: -40°C to +85°C  
<sup>12</sup> AEC-Q100: -40°C to +105°C  
<sup>13</sup> Refresh rate  
<sup>14</sup> Number of available I/Os depends on package selection  
<sup>15</sup> Receive Pins
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<th>PSoC® Designer™</th>
<th>TrueTouch® Host Emulator²</th>
<th>TrueTouch Driver for Android³</th>
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<td>CYAT8X7XX</td>
<td>Production</td>
<td>Contact Sales</td>
<td></td>
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</tr>
</tbody>
</table>

Contact Cypress Sales for the latest TrueTouch software, drivers and tools

1 PSoC Designer, TTHE and MTK releases are backward compatible. The latest version is recommended for new designs.
2 TrueTouch Host Emulator (TTHE) is a front-end tool used to configure, tune, debug and demonstrate TrueTouch devices
3 TrueTouch Driver for Android (TTDA) is the driver for Android that translates touch information into Linux/Android events
4 TrueTouch Manufacturing Test Kit (MTK) enables customers and ITO partners to test touch panels that use Cypress TrueTouch controllers through the manufacturing flow
CYAT8268X
Automotive TrueTouch® Gen6 Family

Applications
Large touchscreen human machine interface (HMI) systems

Features

- Advanced User Interface
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay

- Proprietary Analog Front End\(^2\) with AutoArmor™\(^3\)
  - 54 Receive channels to support ≥100-Hz refresh rates
  - DualSense™: Self\(^4\) and mutual\(^5\)-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications

- Sensor Design
  - Supports Hybrid In-Cell\(^6\) sensors

- System Solutions
  - Manufacturing test kits for production testing

- Package
  - 100-pin TQFP

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Sampling: Now
Production: Now

1 The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
2 Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3 Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4 The capacitance of a row or column line in a touchscreen sensor
5 The capacitance between a row and a column in a touchscreen sensor
6 TX/VCOM share the same layer, receive ITO layer on/above the color filter
7 Interrupt
8 Display Driver Interface
CYAT8168X
Automotive TrueTouch® Gen6 Family

Applications
Large touchscreen human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay

- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - True 5-V TX-Boost\(^4\) with Multi-Phase TX\(^4\)
  - 54 Receive Channels to support ≥100-Hz refresh rates
  - DualSense\(^5\): Self\(^5\) and mutual\(^6\)-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications

- **System Solutions**
  - Manufacturing test kits for production testing

- **Package**
  - 128-pin TQFP, 100-pin TQFP

Collateral
Datasheet and Design Guide: [Contact Sales](mailto:automotive@cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

Availability

Sampling: Now  Production: Now

---

1 The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
2 Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3 Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4 A scanning method used to drive multiple TX lines simultaneously
5 The capacitance of a row or column line in a touchscreen sensor
6 The capacitance between a row and a column in a touchscreen sensor
7 Interrupt
CYAT8165X
Automotive TrueTouch® Gen6 Family

Applications
Small and medium touchscreen human machine interface (HMI) systems

Features
- **Advanced User Interface**
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - True 5-V TX-Boost\(^4\) with Multi-Phase TX\(^4\)
  - 17 Receive Channels to support ≥100-Hz refresh rates
  - DualSense\(^5\): Self- and mutual-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 100-pin TQFP and 64-pin TQFP

Collateral
Datasheet and Design Guide: [Contact Sales](mailto:automotive@cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

Availability
Sampling: Now  Production: Now

---

1. The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
2. Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3. Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4. A scanning method used to drive multiple TX lines simultaneously
5. The capacitance of a row or column line in a touchscreen sensor
6. The capacitance between a row and a column in a touchscreen sensor
7. Interrupt
CYAT7165X
Automotive TrueTouch® Gen6 Family

Applications

Touchpad human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Support with square, rectangular, round, and free-form shape
  - Waterproofing: Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
  - Typical refresh rate of 120 Hz

- **Proprietary Analog Front End** with AutoArmor™
  - True 5-V TX-Boost™ with Multi-Phase TX
  - 17 Receive Channels to support typical refresh rate of 120 Hz
  - DualSense™: Self- and mutual-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications

- **System Solutions**
  - Manufacturing test kits for production testing

- **Package**
  - 56-QFN wettable flank, 64-pin TQFP

Collateral

Datasheet and Design Guide: [Contact Sales](mailto:ContactSales) or [automotive@cypress.com](mailto:automotive@cypress.com)

Availability

Sampling: Q1 2020  
Production: Q1 2020

---

1 The ability of a touchpad sensor to work properly in the presence of water droplets, condensation or sweat
2 Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3 Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4 A scanning method used to drive multiple TX lines simultaneously
5 The capacitance of a row or column line in a touchscreen sensor
6 The capacitance between a row and a column in a touchscreen sensor
7 Interrupt
### Applications
- Slider human machine interface (HMI) systems

### Features
- **Advanced User Interface**
  - Waterproofing: Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
  - Typical refresh rate of 200 Hz
  - Low-power wake-up button: Typical power consumption of 50 µA
- **Proprietary Analog Front End** with AutoArmor
  - True 5-V TX-Boost™ with Multi-Phase TX
  - 17 Receive Channels to support ≥200-Hz refresh rates
  - DualSense™: Self- and mutual-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 56-pin QFN wettable flank, 64-pin TQFP

### Collateral
- Datasheet and Design Guide: [Contact Sales](mailto:automotive@cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

### Availability
- **Sampling:** Now
- **Production:** Now

---

1 The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
2 Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3 Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4 A scanning method used to drive multiple TX lines simultaneously
5 The capacitance of a row or column line in a touchscreen sensor
6 The capacitance between a row and a column in a touchscreen sensor
7 Interrupt
CYAT817X
Automotive TrueTouch® Gen7 Family

**Applications**
Integrated touchscreen human machine interface (HMI) systems with multimodal feedback

**Features**
- **Advanced User Interface**
  - 50-mm hover\(^1\) performance and force touch\(^2\) support
  - Supports low-power CapSense\(^3\) wake-up button
  - 4x timer/counter/pulse-width modulator (TCPWM) blocks for haptic feedback controls
  - 1x I²S block for acoustic feedback
  - Parallel reporting of touch data via SCB\(^4\) or CAN blocks
  - Includes a Crypto block for optional data encryption
- **Proprietary Analog Front End\(^5\) with AutoArmor\(^6\)**
  - True 5-V TX-Boost\(^7\) with multi-phase TX
  - 64 receive channels to support ≥100-Hz refresh rates
  - Multi-phase self-capacitance methodology aids in meeting EMI/EMC requirements without performance degradation
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), ESD (IEC 62132), and system-level (CISPR 25) specifications
- **Packages**
  - 128-pin TQFP, 100-pin TQFP

**Collateral**
Datasheet and Design Guide: [Contact Sales](mailto:contact.sales@cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

**Availability**
Sampling: Now
Production: Now

---

1. A feature allowing the detection of fingers hovering over the touchscreen sensor
2. The ability of a touchscreen sensor to distinguish between different levels of force being applied on the touchscreen
3. Cypress’ touch-sensing user interface solution. The industry’s No. 1 solution in sales by 4x over No. 2 due to superior performance
4. Serial communication block, configurable as SPI, I²C or UART
5. Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
6. Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
## Automotive TrueTouch Packages

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<tr>
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³ Wettable flanks package to allow automated optical inspection (AOI)
Automotive PSoc® Roadmap
Automotive PSoC and MCU Portfolio

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<td>Ultra-Low-Power 8-/16-Bit Replacement</td>
<td>Mid-Range Performance</td>
<td>High Performance</td>
<td>Next Generation</td>
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</tbody>
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Programmable System-on-Chip (PSoC) is a brand of Cypress MCUs for the broad-base embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing.

Flexible MCU (FM) is a portfolio of high-performance Arm<sup>®</sup>-M-based MCUs for industrial and consumer applications.

1 A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters.

2 A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic.

**PSoC 3**
- 8051 CPU
- 67 MHz, 64KB Flash
- Up to 19 PAB, 30 PDB, 72 I/Os

**PSoC 4**
- Cortex<sup>®</sup>-M0/M0+
- 48 MHz, 256KB Flash
- Up to 13 PAB, 20 PDB, 96 I/Os

**PSoC Analog Coprocessor CY8C4xxx**
- 48 MHz, 32KB Flash
- Up to 12 PAB, 11 PDB, 38 I/Os

**PSoC 6 HMI**
- Cortex<sup>®</sup>-M7
- NDA Required, Contact Sales

**FM3 MCUs**
- Cortex<sup>®</sup>-M3
- 144 MHz, 1.5MB Flash, 154 I/Os

**FM4 MCUs**
- Cortex<sup>®</sup>-M4
- 200 MHz, 2MB Flash, 190 I/Os

**8FX**
- 8-bit RISC MCU
- 16 MHz, 32–50KB Flash

**FM0+ MCUs**
- Cortex<sup>®</sup>-M0+
- 40 MHz, 512KB Flash, 102 I/Os

**PSoC 1**
- M8C CPU
- 24 MHz, 32KB Flash
- 16 PAB, 16 PDB, 64 I/Os

**PSoC 5LP**
- Cortex<sup>®</sup>-M3
- 80 MHz, 256KB Flash
- 20 PAB, 30 PDB, 72 I/Os

**PSoC 4**
- Cortex<sup>®</sup>-M0/M0+
- 48 MHz, 256KB Flash
- Up to 13 PAB, 20 PDB, 96 I/Os

**PSoC CP**
- Cortex<sup>®</sup>-M0
- 40 MHz, 512KB Flash, 102 I/Os

**PSoC 7**
- Cortex<sup>®</sup>-M7
- NDA Required, Contact Sales
## Automotive Portfolio: PSoC® 1

**M8C CPU | 24 MHz**

### PSoC MCU
- **CY8C21x23**
  - 4K/0.25K, 16 GPIOs
  - CapSense, 1x10-bit ADC
  - Grades: A and E

- **CY8C23x33**
  - 8K/0.25K, 26 GPIOs
  - CapSense, 1x8-bit ADC

- **CY8C24x93**
  - 32K/2K, 36 GPIOs
  - 1x10-bit ADC

### Programmable Digital

### Intelligent Analog
- **CY8C21x34**
  - 8K/0.5K, 28 GPIOs
  - CapSense, 1x10-bit ADC
  - Grades: A and E

- **CY8C23x45**
  - 16K/1K, 38 GPIOs
  - CapSense, 1x10-bit SAR ADC
  - Grades: A and E

- **CY8C24x23**
  - 4K/0.25K, 24 GPIOs
  - CapSense, 1x14-bit ΔΣ ADC

### Performance Analog
- **CY8C24894**
  - 16K/1K, 56 GPIOs
  - CapSense, 2x14-bit SAR ADC
  - Grade: A

- **CY8C28xxx**
  - 16K/1K, 44 GPIOs
  - CapSense, 4x14-bit ΔΣ ADC

### Flash KB/SRAM KB
1. **Flash KB**
2. **SRAM KB**

### General-purpose input/output pins

### Analog-to-digital converter: Includes incremental, successive approximation register (SAR) or Delta-Sigma (ΔΣ) ADCs

### Performance
- **CY8C29x66**
  - 32K/2K, 44 GPIOs
  - 1x14-bit ΔΣ ADC
  - Grades: A and E

- **CY8C27x43**
  - 32K/2K, 44 GPIOs
  - CapSense, 1x14-bit ΔΣ ADC

- **CY8C24894**
  - 16K/1K, 56 GPIOs
  - CapSense, 2x14-bit SAR ADC
  - Grade: A

- **CY8C2xx45**
  - 16K/1K, 44 GPIOs
  - CapSense, 1x10-bit SAR ADC
  - Grades: A and E

### Concept Development Sampling Production

### Industrial Automotive Availability

### Grade
- **AEC-Q100**: -40°C to +85°C
- **AEC-Q100**: -40°C to +125°C

### Availability

### Production

### Sampling

### Development

### Concept
<table>
<thead>
<tr>
<th>Automotive Portfolio: PSoC® 4</th>
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<tbody>
<tr>
<td>**Flexibility</td>
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### PSoC Portfolio

<table>
<thead>
<tr>
<th>PSoC MCU</th>
<th>Intelligent Analog</th>
<th>Precision Analog</th>
<th>Prog Digital</th>
<th>Sense Anything</th>
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<tbody>
<tr>
<td><strong>PSoC 4000</strong></td>
<td><strong>PSoC 4100</strong></td>
<td><strong>PSoC 4 HV PA</strong></td>
<td><strong>PSoC 4200</strong></td>
<td><strong>PSoC 4700</strong></td>
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#### Flash

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#### Automotive Portfolio: PSoC® 4

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### PSoC 4100

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### Precision Analog PSoC 4 HV PA

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### Prog Digital PSoC 4200

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### Sense Anything PSoC 4700

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<tr>
<td>Grades: A and S</td>
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</table>

### Additional Features

- **Flash KB/SRAM KB**
- **Universal digital block**
- **Comparator**
- **Controller area network**
- **Current-output DAC**
- **AEC-Q100: -40°C to +105°C**
- **AEC-Q100: -40°C to +85°C**

---

185 Cypress Roadmaps
## Automotive Portfolio: PSoC® Software

<table>
<thead>
<tr>
<th>Software</th>
<th>PSoC Creator™</th>
<th>PSoC Designer™</th>
<th>PSoC Programmer</th>
<th>EZ-Click™</th>
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<tr>
<td>PSoC 4</td>
<td>Production</td>
<td>Production</td>
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</tbody>
</table>

Download the latest PSoC software version [here](#).

---

1 All software and tool releases are backward compatible. The latest versions are recommended for new designs.
2 PSoC Creator is an Integrated Design Environment (IDE) that allows concurrent hardware and firmware design of PSoC 3 and PSoC 4 systems.
3 PSoC Designer is an IDE that enables firmware design using a library of precharacterized peripherals for PSoC 1 systems.
4 PSoC Programmer can be used with PSoC Designer and PSoC Creator to program and debug any design onto a PSoC device.
5 EZ-Click is a Windows® GUI-based tool that enables development of CapSense MBR solutions. It allows you to set up sensor configuration, apply global system properties, monitor real-time sensor output, and run production-line system diagnostics.
PSoC® 4000S-Series
PSoC MCU

Applications
User interface for infotainment systems, user interface for heating, ventilation, air conditioning

Features
- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 32KB Flash
  - 4KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope analog-to-digital converter (ADC)\(^1\)
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Two serial communication blocks (SCB) that are configurable as I2C, SPI, UART or LIN Slave
- **Packages**
  - 24-pin QFN and 28-pin SSOP
- **I/O Subsystem**
  - Up to 24 GPIOs, including 16 Smart I/Os\(^2\)

Collateral
Datasheet: **PSoC 4000S**

Availability
**Sampling:** Now  **Production:** Now

---

\(^1\) A simple ADC used to measure slow-moving signals
\(^2\) Embedded programmable digital logic in the I/O subsystem
PSoC® 4100S-Series

Intelligent Analog

Applications
User interface for heating, ventilation, air conditioning, MCU and discrete analog replacement

Features
- 32-Bit MCU Subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB Flash
  - 8KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- Programmable Analog Blocks
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-kspS single-slope ADC
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- Programmable Digital Blocks
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave
- Packages
  - 28-pin SSOP and 40-pin QFN
- I/O Subsystem
  - Up to 34 GPIOs, including 16 Smart I/Os

Collateral
Datasheet: PSoC 4100S

Availability
Sampling: Now  Production: Now

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem
**PSoC® 4100S Plus-Series**

**Intelligent Analog**

### Applications
User interface for HMI applications, Body Control and HVAC applications

### Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller and real-time clock (RTC)
  - 128KB Flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32KHz watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksp single-slope ADC¹
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave

- **One Controller Area Network (CAN) Controller**

- **Packages**
  - Up to 54 GPIOs, including 24 Smart I/Os²

### Collateral

**Datasheet:** Contact Sales

---

¹ A simple ADC used to measure slow-moving signals
² Embedded programmable digital logic in the I/O subsystem
**PSOC® 4100M-Series**

**Intelligent Analog**

### Applications
User interface for HMI applications, body control and HVAC applications

### Features
- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Mspa/s successive approximation register (SAR) ADC
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 48-pin LQFP and 64-pin TQFP
- **I/O Subsystem**
  - Up to 51 GPIOs

### Collateral
Datasheet: [Contact Sales](#)

---

**Availability**

**Sampling:** Now  
**Production:** Now
**PSoC® 4200M-Series**

**Programmable Digital**

**Applications**

User interface for HMI applications, body Control and HVAC applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM

- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Mspss successive approximation register (SAR) analog-to-digital converter (ADC)
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)

- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART

- **Two Controller Area Network (CAN) Controllers**

- **Packages**
  - 48-pin LQFP, 56-pin QFN and 64-pin TQFP

**Collateral**

Datasheet: [Contact Sales](#)

**Availability**

Sampling: Now  
Production: Now
## Automotive PSoC Packages

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<tr>
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<th>Package</th>
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<th>SSOP</th>
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1 Wettable flanks package to allow automated optical inspection (AOI)
Flash Memory Automotive Roadmaps
### NOR Flash Memory Automotive Family Decoder

**Technology:**
- J = 110-nm Floating Gate (FG)
- K = 90-nm FG
- L = 65-nm FG
- M = 50-nm FG
- P = 90-nm MirrorBit® (MB)
- Q = 90-nm MB
- S = 65-nm MB
- T = 45-nm MB

**Density:**
- 008 = 8Mb
- 016 = 16Mb
- 032 = 32Mb
- 064 = 64Mb
- 128 = 128Mb
- 256 = 256Mb
- 512 = 512Mb
- 1G = 1Gb
- 2G = 2Gb
- 4G = 4Gb

**Voltage:**
- D = 2.5 V
- L = 3.0 V
- S = 1.8 V

**Family:**
- A = Standard Address-Data Parallel (ADP)
- C = Burst Mode ADP
- F = Serial
- G = Page Mode
- H = High-Performance Serial
- J = Simultaneous Read/Write ADP
- K = HyperBus™
- P = Page Mode Simultaneous Read/Write ADP

**Series:**
- 25 = SPI
- 26 = HyperBus™
- 28 = Octal
- 35 = SPI with Security
- 36 = HyperBus™ with Security
- 38 = Octal with Security
- 29 = Parallel
- 70 = Stacked Die
- 79 = Dual Quad SPI

**Prefix:**
- S
## NOR Flash Memory Automotive Product Portfolio: New Products

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Sector Size</th>
<th>Series</th>
<th>Voltage</th>
<th>Densities</th>
<th>Lead</th>
<th>Tech</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
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<td>Quad SPI</td>
<td>Hybrid</td>
<td>S25HS-T S25HL-T</td>
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<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
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- **Concept**
- **Samples**
- **Production**
- **EOL**
## x8 Serial NOR Flash Memory Automotive Roadmap

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<tr>
<th>Product Family</th>
<th>Density</th>
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<th>2020</th>
<th>2021</th>
<th>2022</th>
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<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
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<tr>
<td>S28HL-T² (3.0 V)</td>
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<td>(TBD)</td>
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1. AEC-Q100  
2. JEDEC xSPI Compliant  
3. Hybrid Sector  
4. Stacked Die  
5. S79 Series (stacked die)

Products supported by Longevity Program unless noted.

- Concept  
- Samples  
- EOL - LTB  
- EOL - LTS
### x8 Serial NOR Flash Memory Automotive Portfolio

<table>
<thead>
<tr>
<th>256 Mb</th>
<th>64–128 Mb</th>
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</thead>
<tbody>
<tr>
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<td>HyperFlash</td>
</tr>
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<td>S26KL-S</td>
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<td>65-nm MB, 3.0 V</td>
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<td>S26HL01GT</td>
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<tr>
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<td>133 MHz / 166 MHz</td>
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<td>* A, B, M</td>
<td>* A, B, M</td>
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</tbody>
</table>

### Product Family Number

**SDR Clock / DDR Clock**

* Temperature Range

**At parts supported by Longevity Program unless noted**

### Status

**Concept** | **Development** | **Sampling** | **Production** |

**Availability**

**EOL (Last-Time-Ship)**

### Notes

1. Hybrid Sector
2. S79 series (stacked die)
3. With HyperBus™ Interface
4. JEDEC xSPI Compliant
5. With Octal Interface
6. Stacked die
7. Contact Sales

* A = Automotive, AEC-Q100 Grade 3: -40°C to +105°C
  B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
  M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
## x4 Serial NOR Flash Memory Automotive Roadmap

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<th>Product Family</th>
<th>Density</th>
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<th>2020</th>
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<th>2022</th>
<th>2023</th>
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<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
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<td>90-nm FG³</td>
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1. AEC-Q100
2. Hybrid Sector
3. VDD 1.8 V to 3.0 V
4. Uniform Sector
5. Stacked Die
6. 3.0 V QSPI only in production
7. S70 Series (stacked die)
8. S25FL127S and S25FL128S
9. FS-S only
10. S25FL128P and S25FL129P

Products supported by Longevity Program unless noted:
- Concept: Samples
- Production: EOL - LTB
- Facilities: EOL - LTS

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198 Cypress Roadmaps
# x4 Serial NOR Flash Memory Automotive Portfolio

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<th>S25FL1-K¹</th>
<th>S25FL-P¹</th>
<th>S25FL-S¹</th>
<th>S25FL-L¹</th>
<th>S25HL-T¹</th>
<th>S25FS-S¹</th>
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<th>S25FS256S</th>
<th>S25HL256L</th>
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<td>* A, B, M</td>
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## Notes
- **¹** Hybrid Sector
- **²** Uniform Sector
- **³** With QSPI
- **⁴** Stacked die
- **⁵** S70 series (stacked die)
- **⁶** S25FL129P Quad SPI
- **⁷** S25FL129P Dual SPI
- **⁸** Contact Sales

## AEC-Q100
- **A** = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
- **B** = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- **M** = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
## Parallel and Burst Parallel NOR Flash Memory

### Automotive Roadmap

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<th>2020</th>
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1. AEC-Q100
2. Supports Page Mode
3. Supports Simultaneous Read/Write Operation
4. S70 series (stacked die)

**Products supported by Longevity Program unless noted**

- **Concept**
- **Samples**
- **Production**
- **EOL - LTB**
- **EOL - LTS**

---

200 Cypress Roadmaps
# Parallel and Burst Parallel NOR Flash Memory

## Automotive Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial / Page Access</th>
<th>* Temp Range</th>
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1. **Address Data Parallel (ADP) Burst**
2. **Supports Simultaneous Read/Write Operation**
3. **Supports Page Mode**
4. **S70 series (stacked die)**

- **A** = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
- **B** = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- **M** = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
- **T** = Automotive, AEC-Q100 Grade 0: -40°C to +145°C

## Marketing Information

**Engineering AEC-Q100/Production**

- **Status**
  - Concept
  - Development
  - Sampling
  - EOL (Last-Time-Ship)
  - EOL (Last-Time-Ship)

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<td>Production</td>
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Flash and RAM Memory Automotive MCP
Flash and RAM Memory Automotive MCP Decoder

- **RAM Density:**
  - A = 16Mb
  - B = 32Mb
  - C = 64Mb
  - D = 128Mb
  - E = 256Mb

- **Flash Technology:**
  - S = 65-nm MirrorBit (MB)
  - T = 45-nm MB

- **Flash Density:**
  - 128 = 128Mb
  - 256 = 256Mb
  - 512 = 512Mb
  - 01G = 1Gb

- **Voltage:**
  - L = 3.0 V
  - S = 1.8 V

- **Family:**
  - H = High-Performance Serial
  - K = HyperFlash

- **Series:**
  - 71 = NOR Flash + pSRAM

- **Prefix:**
  - S
### Flash and RAM Memory Automotive MCP Roadmap

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\(^1\)AEC-Q100

Products supported by Longevity Program unless noted

- Concept
- Production
- EOL - LTB
- EOL - LTS

- Samples

---

204 Cypress Roadmaps
# Flash and RAM Memory Automotive MCP Portfolio

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All parts supported by Longevity Program unless noted.

* HyperFlash
  * A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
  * B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

© Cypress Semiconductor Corporation

Cypress Roadmaps

205 Cypress Roadmaps
Package Offerings
## x8 NOR Flash Memory Packages

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<th>Device</th>
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CF = Contact Factory
UD = Under Development
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CF = Contact Factory  
UD = Under Development
## Parallel and Burst Parallel NOR Flash Memory Packages

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CF = Contact Factory
RAM Automotive Roadmap
Nonvolatile RAM Roadmap

F-RAM™, nvSRAM
# Cypress Roadmaps

## LPC™ F-RAM

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<th>Speed</th>
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<td>1.8 V, 108-MHz QSPI</td>
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<td>40-MHz SPI</td>
<td>1.8 V, 108-MHz QSPI</td>
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## Processor Companion

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<td>2.0-3.6 V</td>
<td>60 ns; x16; Ind</td>
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## Parallel F-RAM

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<td>2Mb</td>
<td>2.0-3.6 V</td>
<td>60 ns; x16; Ind</td>
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## Features

- Low-pint-count
- Industrial grade -40 °C to +85 °C
- Ultra-low-energy
- Quad serial peripheral interface
- AEC-Q100 -40 °C to +125 °C
- AEC-Q100 -40 °C to +85 °C
- Real-time clock
- Concept
- Development
- Sampling
- Production

---

1. Low-pin-count
2. Industrial grade -40 °C to +85 °C
3. Ultra-low-energy
4. Quad serial peripheral interface
5. AEC-Q100 -40 °C to +85 °C
6. AEC-Q100 -40 °C to +125 °C
7. Real-time clock
## nvSRAM Portfolio

### High Density | High Speed

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<th>LPC(^1) nvSRAM</th>
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<td>CY14B256PA 256Kb: 3.0 V 40-MHz SPI; Ind RTC</td>
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<tr>
<td>CY14B116KL 15Mb: 3.0 V 25, 45 ns; x8; Ind RTC</td>
<td>CY14B256I 256Kb: 3.0 V 3.4-MHz FC; Ind RTC</td>
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<td>CY14V116F/G 16Mb: 3.0, 1.8 V IO 30 ns; ONFI(^1) 1.0 x8, x16; Ind</td>
<td>CY14B064PA 64Kb: 3.0 V 3.4-MHz SPI; Ind RTC</td>
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<td>CY14B064I 64Kb: 3.0 V 3.4-MHz FC; Ind RTC</td>
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<td>CY14B101PS 1Mb: 3.0, 1.8 V IO 108-MHz QSPI; Ind Ext. Ind; RTC</td>
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1. Low-pin-count
2. Industrial grade -40 °C to +85 °C
3. Real-time clock
4. Open NAND flash interface
5. Error-correcting code
6. AEC-Q100 -40 °C to +125 °C
7. Quad serial peripheral interface
8. Extended Industrial grade -43 °C to +105 °C
9. Military grade -55 °C to +125 °C

---

**Legend:**

- Industrial
- Automotive
- Concept
- Development
- Sampling
- Production
## Nonvolatile RAM Roadmap

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<th>Product Family</th>
<th>Density</th>
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<th>2020</th>
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2Mb-to-16Mb Excelon™ F-RAM Family

**Applications**
Medical devices, wearables, industrial control and automation, and automotive

**Features**
- **Excelon-Ultra**
  - 2Mb to 16Mb
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - Industrial temperature range: -40 °C to +85 °C
- **Excelon-Auto**
  - 2Mb to 8Mb Auto “E”, 4Mb to 16Mb Auto “A”
  - 50-MHz Serial Peripheral Interface (SPI)
  - Automotive temperature range grade “A”: -40 °C to +85 °C
  - Automotive temperature range grade “E”: -40 °C to +125 °C
- **Excelon-LP**
  - 2Mb to 16Mb
  - 20-MHz SPI (Commercial), 50-MHz SPI (Industrial)
  - Ultra-low (0.1-µA) hibernate current
  - Ultra-low (0.75-µA) deep power-down current
  - Ultra-low (2.3-µA) standby current
  - Commercial temperature range: 0 °C to +70 °C
  - Industrial temperature range: -40 °C to +85 °C
- **Common features for Excelon-Ultra/Auto/LP**
  - Operating voltage ranges: 1.71 V to 1.89 V, 1.80 V to 3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

**Collateral**
- Final Datasheets: 4Mb Excelon-Ultra, 2Mb Excelon-Auto, 8Mb Excelon-LP

**Excelon F-RAM**

**Features**
- Control
  - Control Logic
- Instruction Register
- Address Register
- Data I/O Register
- Status Register
- I/Os
- Quad SPI has 4 I/Os

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>Standby Current (Typ.)</th>
<th>Active Current (Typ.)</th>
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<td>3 mA</td>
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**Availability**

**Sampling:**
- Now (4Mb Auto A, 4Mb & 8Mb Ultra/LP), Q419 (2Mb Ind), Q220 (16Mb)

**Production:**
- Now (2Mb Auto E, 4Mb & 8Mb Ultra/LP), Q419 (4Mb Auto A), Q120 (2Mb Ind), Q420 (16Mb)
## F-RAM Packages

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## nvSRAM Packages

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Parallel Asynchronous SRAM Roadmap

Low-Power (MoBL®), Fast, PowerSnooze™
## Parallel Asynchronous SRAM Portfolio

### Fast SRAM

<table>
<thead>
<tr>
<th>Density</th>
<th>2MB–16Mb</th>
<th>32MB–64Mb</th>
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<tbody>
<tr>
<td>CY7C107x</td>
<td>32Mb: 3.3 V</td>
<td>12 ns; x8, x16</td>
</tr>
<tr>
<td>CY7C108x</td>
<td>32Mb: 3.3 V</td>
<td>10 ns; x8, x16, x32</td>
</tr>
<tr>
<td>CY7C109x</td>
<td>16Mb: 3.3, 5.0 V</td>
<td>10 ns; x8, x16, x32</td>
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<tr>
<td>CY7C110x</td>
<td>8Mb: 3.3, 5.0 V</td>
<td>10 ns; x8, x16</td>
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<td>CY7C111x</td>
<td>4Mb: 3.3, 5.0 V</td>
<td>10 ns; x4, x8, x16</td>
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<tr>
<td>CY7C120x</td>
<td>512Kb: 2.6, 3.3, 5.0 V</td>
<td>10 ns; x16</td>
</tr>
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</table>

### Low-Power SRAM (MoBL<sup>®</sup>3)

| Non-ECC (≥90nm) | ECC (65nm) | CY6216x | 16Mb: 1.8, 3.0 V | 45 ns; x16 |
| Non-ECC (65nm) | ECC (65nm) | CY6217x | 32Mb: 1.8-5.0 V | 55 ns; x16 |

### PowerSnooze™4

<table>
<thead>
<tr>
<th>Production</th>
<th>Development</th>
<th>Sampling</th>
<th>Concept</th>
</tr>
</thead>
</table>

### 1 AEC-Q100 -40°C to +85°C
### 2 AEC-Q100 -40°C to +125°C
### 3 More Battery Life
### 4 A Fast SRAM with a deep-sleep mode in addition to the conventional standby
### 5 Ultra-Low-Power
# Parallel Asynchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(ES) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
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<tbody>
<tr>
<td>MoBL SRAM ULP 65 nm, ECC Parallel Asynchronous</td>
<td>16Mb</td>
<td>(Q3’20)</td>
<td>(Q1’20)</td>
<td>Q1</td>
<td>Q2</td>
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<td>Q4</td>
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<td>MoBL SRAM 65 nm, ECC Parallel Asynchronous</td>
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<tr>
<td>MoBL SRAM ≥ 90 nm, Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
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<tr>
<td>PowerSnooze SRAM 65 nm, ECC Parallel Asynchronous</td>
<td>4Mb, 16Mb</td>
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<tr>
<td>Fast SRAM 65 nm, ECC Parallel Asynchronous</td>
<td>2Mb, 4Mb, 8Mb, 16Mb</td>
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</tr>
<tr>
<td>Fast SRAM ≥ 90 nm Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb</td>
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</tbody>
</table>
Low-Power SRAM Family with ECC

**Applications**
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive

**Features**
- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC\(^1\) logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS\(^2\)-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

**Collateral**
Datasheet: [Asynchronous SRAM with ECC](#)

---

\(^1\) Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

\(^2\) Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
Fast SRAM Family with ECC

Applications
Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

Features
- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS²-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

Collateral
Datasheet: [Asynchronous SRAM with ECC](#)

---

1 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2 Restriction of Hazardous Substances: A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

### Collateral
**Datasheet:** [Asynchronous SRAM with ECC](#)

### Availability
**Production:** Now

### Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Operating Current (Maximum at 85°C)</th>
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# Parallel Asynchronous SRAM Packages

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</table>
HyperRAM Roadmap

High-performance Pseudo-static RAM
HyperRAM™ Portfolio

HyperRAM 1.0
S27KL-1
63-nm DR, 3.0 V
HyperBus I/F

HyperRAM 1.0
S27KS-1
63-nm DR, 1.8 V
HyperBus I/F

Density
Initial Access/DDR Clock
* Temperature Range

64–128Mb

128Mb
36 ns/100 MHz
* I, A, V, B

128Mb
36 ns/166 MHz
* I, A, V, B

64Mb
36 ns/100 MHz
* I, A, V, B

64Mb
36 ns/166 MHz
* I, A, V, B

* I = Industrial: -40 °C to +85 °C
A = Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C
V = Industrial-plus: -40 °C to +105 °C
B = Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C

1 Stacked die
# HyperRAM™ Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
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<td>Q2</td>
<td>Q3</td>
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<td>128Mb¹</td>
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<td>S27KL-1 (3.0 V)</td>
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</table>

¹ Stacked die

Products supported by Longevity Program unless noted:

- **EOL - LTB**: End of Life - Limited Technical Bulletin
- **EOL - LTS**: End of Life - Long Term Support
- **Concept**: Concept
- **Production**: Production
- **Samples**: Samples
Synchronous SRAM Roadmap

Std Sync, NoBL®, QDR-II, DDR-II, QDR-IV
### Synchronous SRAM Portfolio

#### High Random Transaction Rate (RTR)\(^1\) | Low Latency | High Bandwidth

<table>
<thead>
<tr>
<th>Density</th>
<th>Standard Sync and NoBL(^6)</th>
<th>Standard Sync and NoBL with ECC(^2)</th>
<th>QDR(^{-}/)II-DDR-II</th>
<th>QDR-II+/DDR-II+</th>
<th>QDR-II+/X/DDR-II+X</th>
<th>QDR-IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes</td>
<td>RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes</td>
<td>RTR: 666 MT/s (max.) BW: 47.6 Gbps (max.) Latency: 1.5 Cycles CIO(^2) and SIO(^2)</td>
<td>RTR: 666 MT/s (max.) BW: 79.2 Gbps (max.) Latency: 2 or 2.5 Cycles CIO and SIO, ODT(^3)</td>
<td>RTR: 900 MT/s (max.) BW: 91.1 Gbps (max.) Latency: 2.5 Cycles SIO, ODT</td>
<td>RTR: 2.1 GT/s (max.) BW: 153.5 Gbps (max.) Latency: 5 or 8 Cycles Dual-Port Bidirectional ODT</td>
<td></td>
</tr>
<tr>
<td>CY7C147/8xK 72Mb; 133–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C144/6xK 36Mb; 133–250 MHz 2.5, 3.3 V; x36, x72</td>
<td>CY7C161/2xKV18 144Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C156/7xKXV18 72Mb; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4</td>
<td>CY7C41xKV13 144Mb; 667–1,066 MHz 1.3 V; x18, x36 Burst 2</td>
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<tr>
<td>CY7C137/8xD/K 18Mb; 100–250 MHz 3.3 V; x18, x32, x36</td>
<td>CY7C137/8xKVE 18Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C151/2xKV18 72Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C154/5/6xKV18 72Mb; 250–550 MHz 1.8 V; x18, x36 RH(^5); Burst 2, 4</td>
<td>CY7C40xKV13 72Mb; 667–1,066 MHz 1.3 V; x18, x36 Burst 2</td>
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<tr>
<td>CY7C135/6xC 9Mb; 100–250 MHz 3.3 V; x18, x32, x36 Auto (^7)</td>
<td>CY7C135/6xKVE 9Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C141/2xKV18 36Mb; 250–333 MHz 1.8 V; x8, x9, x18, x36 Burst 2, 4</td>
<td>CY7C126/7x 36Mb; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4</td>
<td>CY7C156/7xKV18 72Mb; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4</td>
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<td>CY7C134/2xG 2–4Mb; 100–250 MHz 3.3 V; x18, x32, x36</td>
<td>CY7C137/8xKVE 18Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C131/2/9xKV18 18Mb; 250–333 MHz 1.8 V; x8, x18, x36 Burst 2, 4</td>
<td>CY7C124/5/6xKV18 18Mb; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4</td>
<td>CY7C124/5/6/7xKV18 18Mb; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4</td>
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<tr>
<td>CY7C1911xKXV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td>CY7C1911xKXV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td>CY7C1911xKXV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td>CY7C1911xKXV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td>CY7C1911xKXV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1. Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s).
2. Error-correcting code.
3. Common I/O.
4. Separate I/O.
5. On-die termination.
6. Radiation hardened, military grade.
7. AEC-Q100: -40 °C to +125 °C.
## Synchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td><strong>QDR-IV SRAM</strong></td>
<td>65 nm, ECC</td>
<td>72Mb, 144Mb</td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td>2.1 GT/s, 153.5 Gbps</td>
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<tr>
<td><strong>QDR-II-X SRAM</strong></td>
<td>65 nm, ECC</td>
<td>36Mb, 72Mb</td>
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<td></td>
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</tr>
<tr>
<td></td>
<td>900 MT/s, 91.1 Gbps</td>
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</tr>
<tr>
<td><strong>QDR-II+ SRAM</strong></td>
<td>65 nm, ECC</td>
<td>18Mb, 36Mb, 72Mb&lt;sup&gt;1&lt;/sup&gt;, 144Mb</td>
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<tr>
<td></td>
<td>666 MT/s, 79.2 Gbps</td>
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</tr>
<tr>
<td><strong>QDR-II SRAM</strong></td>
<td>65 nm</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
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<tr>
<td></td>
<td>666 MT/s, 47.9 Gbps</td>
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<tr>
<td><strong>Standard Sync and NoBL® SRAM</strong></td>
<td>65 nm, ECC</td>
<td>18Mb, 36Mb</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>250 MT/s, 18 Gbps</td>
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</tr>
<tr>
<td><strong>Standard Sync and NoBL SRAM</strong></td>
<td>65 nm / 90 nm</td>
<td>2Mb, 4Mb, 9Mb&lt;sup&gt;2&lt;/sup&gt;, 18Mb&lt;sup&gt;3&lt;/sup&gt;, 36Mb&lt;sup&gt;3&lt;/sup&gt;, 72Mb</td>
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<tr>
<td></td>
<td>250 MT/s, 18 Gbps</td>
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</tr>
<tr>
<td><strong>Standard Sync and NoBL SRAM</strong></td>
<td>90 nm</td>
<td>36Mb</td>
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</tr>
</tbody>
</table>

<sup>1</sup> Radiation hardened, military grade
<sup>2</sup> AEC-Q100 -40°C to +125°C
<sup>3</sup> 65-nm

![Cypress Roadmap Diagram]
## Synchronous SRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>100-pin TQFP</th>
<th>119-ball BGA</th>
<th>165-ball BGA</th>
<th>209-ball BGA</th>
<th>361-ball BGA</th>
<th>Wafer</th>
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<tr>
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<tr>
<td></td>
<td>36Mb</td>
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<tr>
<td>NoBL</td>
<td>2Mb</td>
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<tr>
<td></td>
<td>9Mb</td>
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<td>18Mb</td>
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<td>✓</td>
<td>✓</td>
<td></td>
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<td>✓</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
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<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
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<td>✓</td>
<td>✓</td>
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<td>✓</td>
</tr>
<tr>
<td>QDR</td>
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<td></td>
<td>✓</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
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<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td></td>
<td></td>
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<td>✓</td>
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<td>✓</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
<td></td>
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<td>✓</td>
</tr>
</tbody>
</table>
PMIC Automotive Roadmap
## Automotive PMIC Family Portfolio

<table>
<thead>
<tr>
<th>Single-channel PMIC</th>
<th>Multi-Channel PMIC Instrument Cluster &amp; Body, ADAS (works with Cypress Traveo/Traveo II)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S6BP203A</strong></td>
<td><strong>S6BP502A</strong></td>
</tr>
<tr>
<td>( V_{BAT} \rightarrow 3.3V \ 2.4A, ) 2-MHz Buck-Boost, PG, 16-Pin TSSOP</td>
<td>( V_{BAT} \rightarrow 5.0V / 3.3V / 1.1V (2.0A), 400-kHz Buck, 2-MHz Buck, PG, SSCG, HOT, 32-Pin wettable QFN</td>
</tr>
<tr>
<td><strong>S6BP202A</strong></td>
<td></td>
</tr>
<tr>
<td>( V_{BAT} \rightarrow 5.0V \ 2.4A, ) 2-MHz Buck-Boost, PG, 16-Pin TSSOP</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP201A</strong></td>
<td></td>
</tr>
<tr>
<td>( V_{BAT} \rightarrow 5.0V \ 1.0A, ) 2-MHz Buck-Boost, PG, 16-Pin TSSOP</td>
<td></td>
</tr>
</tbody>
</table>

### Typical Input Voltage

- **12 V**
- **5.0 V/3.3 V**

### Status

- **Concept**
- **Development**
- **Sampling**
- **Production**

### Availability

- **SOYV**
- **SOYP**

---

1. Lead-acid battery whose typical voltage is 12V.
2. Topology to supply stable output regardless of input variation.
3. Power-Good signal output.
4. Step-down voltage regulator.
5. Step-up voltage regulator.
6. Spread-spectrum clock generator which deliberately varies the internal clock signal frequency to lower the electromagnetic radiation.
7. Hard pin output that indicates the die is getting hot.
8. QFN packages whose pin is processed so that the solder fillet would form between the pin and pad.
S6BP20xA
One-Channel Buck-Boost Automotive PMIC

**Applications**
- Instrument clusters, body electronics and ADAS

**Features**
- **1-Channel PMIC**: Synchronous buck-boost converter
- **Wide Input Voltage Range**: 2.5–42 V
- **Low Quiescent Current**: 20 µA
- **Programmable Switching Frequency**: 0.2–2.1 MHz
  - Synchronization with external clock from 200 kHz to 400 kHz
  - Autonomous PFM/PWM\(^1\) switching
- **BOM Integration**: Built-in switching transistors
- **System Safety Function\(^2\)** Support:
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with power good\(^3\) pin
- **Operating Temperature Range**: -40°C to +125°C
- **Package**: 16-pin thermally enhanced TSSOP (5-mm x 6.4-mm)
- **Qualification**: AEC-Q100 Grade-1

**Collateral**
- **Datasheet**: S6BP201A, S6BP202A and S6BP203A
- **Evaluation Kit**: S6BP201A, S6BP202A and S6BP203A

**Family Table**

<table>
<thead>
<tr>
<th>Output Voltage(^4)</th>
<th>Max. Output Current</th>
<th>MPN</th>
<th>UVP/OVP Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0–5.2 V</td>
<td>2.4 A</td>
<td>S6BP202A</td>
<td>±4.5%, ±8.0%</td>
</tr>
<tr>
<td>5.0–5.2 V</td>
<td>1.0 A</td>
<td>S6BP201A</td>
<td>±4.5%</td>
</tr>
<tr>
<td>3.3 V</td>
<td>2.4 A</td>
<td>S6BP203A</td>
<td>±8.0%</td>
</tr>
</tbody>
</table>

\(^1\) Pulse-frequency modulation / pulse-width modulation
\(^2\) A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
\(^3\) An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
\(^4\) S6BP201A and S6BP202A have factory-selectable options of output voltage, power-on-reset time, UVP/OVP threshold, and SYNC Function
S6BP50xA
Three-Channel Automotive PMIC

Applications
Low-end to mid-range hybrid automotive cluster systems

Features
- **3-Channels**: Buck controller with load switch, boost converter, buck converter
- **Wide Range Input**: 2.5-42 V
- **Low Quiescent Current**: 15 µA
- **High Switching Frequency**:
  - Boost converter and buck converter: 2.1 MHz
  - Built-in spread-spectrum clock generator (SSCG)
  - Synchronization with external clock from 1.8-2.4 MHz
- **System Safety Function**\(^1\) Support:
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Thermal warning
  - Window-monitoring voltage supervisors with independent power good\(^2\) pins
- **Operating Temperature Range**: -40°C to +105°C
- **Package**: 32-pin thermally enhanced side-wettable\(^3\) QFN (5-mm x 5-mm)
- **Qualification**: AEC-Q100 Grade-2

Collateral
- Preliminary Datasheet: S6BP501A/S6BP502A
- Evaluation Kit: S6SBP501A00VA1001/S6SBP502A00VA1001

1 A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
2 An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
3 QFN packages whose pin is processed so that the solder fillet would form between the pin and pad
4 Output voltages are finely adjustable with external resistive dividers

Family Table

<table>
<thead>
<tr>
<th>Buck Converter Output Specification(^4)</th>
<th>MPN</th>
<th>Buck Controller Output Specification</th>
<th>Boost Converter Output Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.15 V, 1.4 A</td>
<td>S6BP501A</td>
<td>3.3 V, 1.6 A</td>
<td>5.0 V, 1.3 A</td>
</tr>
<tr>
<td>1.2 V, 2.0 A</td>
<td>S6BP502A</td>
<td>3.3 V, 1.9 A</td>
<td>5.0 V, 1.3 A</td>
</tr>
</tbody>
</table>

Availability
- Sampling: Now
- Production: Now
S6BP401A
Six-Channel Automotive PMIC

Applications
Advanced driver assistance systems (ADAS), security camera systems

Features
- **6-Channel PMIC**: 4-channel buck converters, 2-channel LDOs
- **Input Voltage Range**: 4.5–5.5 V
  - Input voltage for LDO: 1.62–5.5 V
- **High Switching Frequency**: 2.1 MHz
  - Synchronization with external clock from 1.8–2.4 MHz
- **BOM Integration**:
  - Switching transistors, voltage setting resistors, and compensation circuitry
- **System Safety Function**¹ Support:
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with independent power good² pins
  - Built-in windowed watchdog timer (WDT)
  - Independent enable pins
- **Operating Temperature Range**: -40°C to +125°C
- **Package and Qualification**: 40-pin QFN (6-mm x 6-mm), AEC-Q100 Grade-1

Collateral
- **Datasheet**: S6BP401A
- **Evaluation Kit**: S6SBP401AJ0SA1001, S6SBP401AM2SA1001

Availability
- **Sampling**: Now
- **Production**: Now

¹ A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
² An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
³ S6BP401A has factory-selectable options of output voltage for each channel
## Compatibility with Traveo™ MCU

<table>
<thead>
<tr>
<th>Cypress Automotive PMIC</th>
<th>S6BP201A</th>
<th>S6BP202A</th>
<th>S6BP203A</th>
<th>S6BP501A</th>
<th>S6BP502A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Traveo MCU for Instrument Cluster</strong></td>
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<td>S6J3120</td>
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<td><strong>Traveo MCU for Body Control</strong></td>
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Timing Solutions Automotive Roadmap
# Clock Synthesizer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27430</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>12 Outputs; Diff &amp; SE; PCIe 3.0;</td>
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</tr>
<tr>
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<td>VCXO; EMP; 0.7-ps RMS Jitter</td>
<td>(EOL)</td>
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</tr>
<tr>
<td></td>
<td>1.8 V/2.5 V/3.3 V; Ind; 48-QFN</td>
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</tr>
<tr>
<td>CY27410</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
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<tr>
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<td>8 Outputs; Diff &amp; SE; PCIe 3.0;</td>
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<td>VCXO; EMP; 0.7-ps RMS Jitter</td>
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<tr>
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<td>1.8 V/2.5 V/3.3 V; Auto A 5; S 5; 48-QFN</td>
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<tr>
<td>CY254x/CY251x</td>
<td>1-4 PLL; Maximum Frequency: 200 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<td>3-9 Outputs; PC; EMI; Low Power</td>
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<tr>
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<td>100-ps CCJ 5; Ind; 1.8 V/2.5 V/3.0 V/3.3 V</td>
<td>(EOL)</td>
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<td>8-SOIC; 8/16/20-TSSOP; 24-QFN</td>
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<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Maximum Frequency: 166 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td></td>
<td>3-8 Outputs; CMOS; Low Power</td>
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</tr>
<tr>
<td></td>
<td>200-ps PPJ 5; VCXO; Ind; 3.3 V/5 V</td>
<td>(EOL)</td>
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<tr>
<td></td>
<td>8/16/20-TSSOP; 16-TSSOP</td>
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</tr>
<tr>
<td>CY2429x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td></td>
<td>2-5 Outputs; HCSL, CMOS; EMI</td>
<td></td>
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<tr>
<td></td>
<td>75-ps CCJ 1.1; Ind; Auto A</td>
<td>(EOL)</td>
<td></td>
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<tr>
<td></td>
<td>3.3 V; 16-TSSOP; 32-QFN</td>
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</tr>
<tr>
<td>CY2239x</td>
<td>3-4 PLL; Maximum Frequency: 400 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>5-8 Outputs; LVPECL; CMOS; PC</td>
<td></td>
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<tr>
<td></td>
<td>400-ps PPJ 5; VCXO; 3.3 V</td>
<td>(EOL)</td>
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<tr>
<td></td>
<td>Ind; Auto A 5; 16-TSSOP; 32-QFN</td>
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<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>1-3 Outputs; CMOS; EMI</td>
<td></td>
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<tr>
<td></td>
<td>110-ps CCJ 5; VCXO; Ind;</td>
<td>(EOL)</td>
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<tr>
<td></td>
<td>3.3 V; 8-SOIC; 8-TSSOP</td>
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<tr>
<td>CY22050/150</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td>(Prod)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td></td>
<td>6 Outputs; CMOS; PC</td>
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<tr>
<td></td>
<td>250-ps PPJ 5; Ind</td>
<td>(EOL)</td>
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<td></td>
<td>2.5 V/3.3 V; 16-TSSOP</td>
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</tbody>
</table>

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1 Differential and single-ended outputs
2 Voltage Controlled Crystal Oscillation
3 Electromagnetic interference reduction using Lexmark profile
4 Integrated phase noise across 12-kHz to 20-MHz offset
5 Industrial grade: -40°C to +85°C
6 AEC-Q100: -40°C to +85°C
7 AEC-Q100: -40°C to +105°C
8 Power Management options
9 Cycle-to-cycle Jitter
10 Peak-to-peak period Jitter
11 AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted
# Clock Buffer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2DPx/CPx</td>
<td>Maximum Frequency: 1.5 GHz 2–10 Outputs; LVPECL; 2.5 V/3.3 V 0.11-ps Additive Jitter(^1); Ind(^2) 820-TSSOP; 8-SOIC; 32-TQFP</td>
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<tr>
<td>CY2DMx/DLx</td>
<td>Maximum Frequency: 1.5 GHz 2–10 Outputs; LVDS, CML; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 820-TSSOP; 32-TQFP</td>
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<tr>
<td>CY230x/EP0x (Zero Delay)</td>
<td>Maximum Frequency: 220 MHz 2–9 Outputs; LVCMOS; 2.5 V/3.3 V/5 V 22-ps CCJ; Ind; Auto A(^4) 8/16-SOIC; 16-TSSOP; WAFER</td>
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<tr>
<td>CY230xNZ/2994x (Non-Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4–18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5 V/3.3 V; 8-TSSOP, 16-SOIC</td>
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<tr>
<td>CY23FS04/08/FP12 (Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4–12 Outputs; LVCMOS; Fail Safe 200-ps CC; Ind 2.5 V/3.3 V 16/28-SSOP</td>
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</tr>
<tr>
<td>CY23S0x (Zero Delay)</td>
<td>Maximum Frequency: 133 MHz 5–9 Outputs; LVCMOS Spread Aware; 90-ps CC; Ind 2.5 V/3.3 V 8/16-SOIC; 16-TSSOP</td>
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</tr>
<tr>
<td>CY7B99x (RoboClock™)</td>
<td>Maximum Frequency: 200 MHz; 8–13 Outputs Configurable Skew; 2.5 V/3.3 V/5.0 V 50-ps CC; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA</td>
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</tr>
</tbody>
</table>

1. Additive RMS Phase Jitter  
2. Industrial grade: -40°C to +85°C  
3. Cycle-to-cycle Jitter  
4. AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted

- **Concept**  
- **Samples**  
- **Production**  
- **EOL - LTB**  
- **EOL - LTS**

241 Cypress Roadmaps
# Timing Solutions Portfolio

**Programmable | High-Performance | EMI Reduction | Automotive**

## Clock Synthesizers

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27410</td>
<td>4-PLL; Max Freq: 700 MHz, 12 Outputs; Spread Aware, 90° peak period jitter</td>
</tr>
<tr>
<td>CY29430</td>
<td>1-PLL; Max Freq: 2.1 GHz, 1 Output; DFF &amp; SE, 40/100 GbE, VCOX; 0.11-ps RMS Jitter, Ind, 48-QFN</td>
</tr>
<tr>
<td>CY254x/CY251x</td>
<td>1-4 PLL; Max Freq: 200 MHz, 3-9 Outputs; FC, EMI; Low Power, 100-ps CCJ, Ind, 1.8/2.5/3.3/3.3 V, 8-SOIC, 16/20-TSSOP, 24-QFN</td>
</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Max Freq: 166 MHz, 3-8 Outputs; CMOS; Low Power, 200-ps PJT, VCOX; Ind, 3.3 V, 8/16/20-SOIC, 16-TSSOP</td>
</tr>
<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Max Freq: 200 MHz, 1-3 Outputs; CMOS, EMI, 110-ps CCJ; VCOX; Ind, 3.3 V, 8-SOIC, 8-TSSOP</td>
</tr>
<tr>
<td>CY22050/150</td>
<td>1-PLL; Max Freq: 200 MHz, 6 Outputs; CMOS, FC, 250-ps PJT, Ind, 2.5/3.3 V, 16-TSSOP</td>
</tr>
</tbody>
</table>

## Oscillators

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2941x/2x</td>
<td>1-PLL; Max Freq: 2.1 GHz, 1 Output; DFF &amp; SE, 40/100 GbE, VCOX; 0.11-ps RMS Jitter, Ind, 8-LCC (7 x 5, 5 x 3.2)</td>
</tr>
<tr>
<td>CY25701</td>
<td>1-PLL; Max Freq: 166 MHz, 1 Output; CMOS; EMI, 85-ps CCJ, Ind, 3.3 V, 4-LCC (5 x 3.2)</td>
</tr>
<tr>
<td>CY5077</td>
<td>1-PLL Max Freq: 166 MHz, 5 Outputs; CMOS, FC, 400-ps PJT, VCOX; 3.3 V, Ind, Auto A E15, 16-TSSOP, 32-QFN</td>
</tr>
<tr>
<td>CY5057</td>
<td>1-PLL Max Freq: 170 MHz, 1 Output; CMOS, EMI, 200-ps CCJ, Ind, 3.3/5.0 V, WAFFER</td>
</tr>
</tbody>
</table>

## Clock Buffers

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2DPx/CPx</td>
<td>Max Freq: 1.5 GHz, 2-10 Outputs; LVPECL, 2.5/3.3 V, 0.11-ps Additive Jitter, 8/20-TSSOP, 8-SOIC, 32-TQFP</td>
</tr>
<tr>
<td>CY2MDx/CLx</td>
<td>Max Freq: 1.5 GHz, 2-10 Outputs; LVDS, CM, 2.5/3.3 V, 0.11-ps Additive Jitter, 8/20-TSSOP, 32-TQFP</td>
</tr>
</tbody>
</table>

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**Standard Performance**

**High Performance**

**EMI Reduction**

**Automotive**

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**Status**

- **Concept**
- **Development**
- **Sampling**
- **Production**
- **EOL**

**Availability**

- **Q219**
- **Q319**
- **Q419**

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242 Cypress Roadmaps
**CY27430: High-Performance 4-PLL Clock Generator**

### Applications
Car infotainment and navigation systems

### Features
- **Eight Outputs**
  - Four configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0, and 10 GbE
  - AEC Q-100 qualified (-40°C to +105°C)
- **Additional Features**
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency select
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-Compliant Package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

### Collateral
- **Preliminary Datasheet**: Contact Sales

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1. Crystal input
2. Crystal output
3. Reference clock inputs
4. Serial port
5. Voltage input pin for VCFS
6. Frequency select inputs
Traveo™ MCU Family Automotive Roadmaps
Wireless Product Automotive Roadmaps
USB Product Automotive Roadmaps

Please Contact Your Cypress Local Sales Office For Details