Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

www.infineon.com
# Cypress Roadmaps Slide Index

<table>
<thead>
<tr>
<th>Page</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Module Solutions</td>
</tr>
<tr>
<td>24</td>
<td>MCU Portfolio</td>
</tr>
<tr>
<td>62</td>
<td>USB Controllers</td>
</tr>
<tr>
<td>85</td>
<td>RAM Solutions</td>
</tr>
<tr>
<td>113</td>
<td>Timing Solutions</td>
</tr>
<tr>
<td>121</td>
<td>Flash Memory</td>
</tr>
<tr>
<td>149</td>
<td>Military Memory</td>
</tr>
<tr>
<td>160</td>
<td>Aerospace Memory</td>
</tr>
<tr>
<td>166</td>
<td>Energy Harvesting PMIC</td>
</tr>
<tr>
<td>172</td>
<td>Automotive Products</td>
</tr>
</tbody>
</table>
Cypress Roadmap: Module Solutions
<table>
<thead>
<tr>
<th>Features</th>
<th>CYBLE-416045-02 EZ-BLE Creator BT 5.0 PSoC 6 BLE 1MB Flash, 2Mbps BLE, 36 GPIOs 14 x 18.5 x 2.00 mm SMT</th>
<th>CYBT-4320xx-02 EZ-BT WICED BT 5.0 Dual Mode CYW20719/21 1MB Flash, 2Mbps BLE 11 x 11 x 1.70 mm SMT</th>
<th>CYBT-3330xx-02 EZ-BT WICED BT 5.0 Dual Mode CYW20706 512KB SFlash, LMA3, XR Ext. Antenna via RF Pad or u.FL 12 x 12 x 1.95 mm SMT</th>
<th>CYBT-4830xx-02 EZ-BT WICED BT 5.0 Dual Mode CYW20719/21 1MB Flash, 2Mbps BLE, PA/LNA, XR Ext. Antenna via RF Pad or u.FL 12 x 12 x 1.95 mm SMT</th>
<th>CYBT-343151-02 EZ-BT WICED BT 5.0 Dual Mode CYW20706 512KB SFlash, 11 GPIOs, XR 12 x 15.5 x 1.95 mm SMT</th>
<th>CYBLE-224111x-0x EZ-BLE Creator BT 4.1/4.2 PSoC4-BLE 256 KB Flash, PA/LNA, XR Opamp, CMP, 4 UDBs, 25 GPIOs 9.5 x 15.4 x 1.80 mm SMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYBT-4130xx-02 EZ-BT WICED BT 5.0 Dual Mode CYW20719/21 1MB Flash, 2Mbps BLE 12 x 16.3 x 1.70 mm SMT</td>
<td>CYBT-223056-02 EZ-BT WICED BT 5.0 Dual Mode CYW20819 256KB Flash, 22 GPIOs, 2Mbps BLE, 11 x 11 x 1.70 mm SMT</td>
<td>CYBT-2630xx-02 EZ-BT WICED BT 5.0 Dual Mode CYW20819 256KB Flash, PA/LNA, XR Ext. Antenna via RF Pad or u.FL 12.5 x 19 x 1.95 mm SMT</td>
<td>CYBT-273063-02 EZ-BT WICED BT 5.0 Dual Mode CYW20819 256KB Flash, PA/LNA, XR 20 GPIOs 12.5 x 19 x 1.95 mm SMT</td>
<td>CYBLE-243053-02 EZ-BT WICED BT 5.0 Dual Mode CYW20820 256KB Flash, 22 GPIOs, 2Mbps BLE, XR, 11 GPIOs 15 x 23 x 2.05/1.55 mm SMT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYBT-213043-02 EZ-BT WICED BT 5.0 Dual Mode CYW20819 256KB Flash, 2Mbps BLE 12 x 16.61 x 1.70 mm SMT</td>
<td>CYBT-253099-02 EZ-BT WICED BT 5.0 Dual Mode CYW20820 256KB Flash, 22 GPIOs, 2Mbps BLE, XR, 11 x 11 x 1.70 mm SMT</td>
<td>CYBLE-2020xx-01 EZ-BLE Creator BT 4.2 PSoC 4 BLE, 256 KB Flash, PA/LNA, XR, Ext. Antenna via RF Pad or u.FL, 19 GPIOs</td>
<td>CYBLE-343052-02 EZ-BT WICED BT 5.0 Dual Mode CYW20820 512KB SFlash, 24 GPIOs, XR, Analog MIC Interface 13.31 x 22.4 x 1.95 mm SMT</td>
<td>CYBLE-212006-01 EZ-BLE Creator BT 4.2 PSoC 4 BLE 256 KB Flash, PA/LNA, XR PCB Antenna, 19 GPIOs 15 x 23 x 2.00 mm SMT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CYBT-343026-01 EZ-BT WICED BT 5.0 Dual Mode CYW20706 512KB SFlash, 11 GPIOs, XR 12 x 15.5 x 1.95 mm SMT</td>
<td>CYBT-353027-02 EZ-BT WICED BT 5.0 Dual Mode CYW20707 512KB SFlash4, XR 9 x 9 x 1.75 mm SMT</td>
<td>CYBLE-x120xx-0x EZ-BLE Creator BT 4.1/4.2 PSoC 4 BLE 128/256KB Flash, 23 GPIOs 14 x 19 x 2.00 mm SMT</td>
<td>CYBLE-x140xx-0x EZ-BLE Creator BT 4.1/4.2 PSoC 4 BLE, 128/256KB Flash, Opamp, CMP, 4 UDBs, 25 GPIOs 11 x 11 x 1.70 mm SMT</td>
<td>CYBLE-416045-02 EZ-BLE Creator BT 4.0 PSoC 4 BLE 128/256KB Flash, 16/18 GPIOs 14 x 19 x 2.25 mm SMT</td>
<td>CYBLE-x220xx-0x EZ-BLE WICED BT 4.1/4.2 PSoC 4 BLE 128/256KB Flash, 16 GPIOs 10 x 10 x 1.80 mm SMT</td>
<td></td>
</tr>
</tbody>
</table>

1. Extended range power
2. Extended temperature
3. Serial flash
4. Power amplifier/Low-noise amplifier
5. Limited modular approval
6. Comparator
7. Universal digital block
8. No shield
9. No certifications
10. Timer/counter/pulse-width modulator
11. Serial communication block

- **Cost**
- **Size**
- **External Antenna**
- **XR**
- **XT**

**BLE, 128/256KB Flash, BT 5.0 Dual Mode XT**

---

**Cypress Bluetooth Module Portfolio**

---

**Cypress Roadmap: Modules – SHNG**
EZ-BLE™ Creator Modules CYBLE-x220xx-0x
Space-Optimized Bluetooth Low-Energy (BLE) Modules

Applications
Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- Qualification and Certification
  - Bluetooth SIG QDID¹, FCC, CE, KC², MIC³, and ISED⁴
- Small Footprint
  - 10 mm x 10 mm x 1.8 mm, 21/22-pad SMT with 16 GPIOs
- Bluetooth Smart Connectivity with BLE 4.1 and 4.2
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
- 1.3-µA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes
- Highly Integrated Solution
  - Two crystals, chip antenna, passives, shield
  - 128KB and 256KB flash sizes
  - Preprogrammed with EZ-Serial firmware
- CYBLE-x220xx-EVAL Evaluation Board Interface
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense®, buttons, GPIOs, over-the-air (OTA)

Availability
Sampling (4.1/128KB, 4.1/256KB, 4.2): Now
Production (4.1/128KB, 4.1/256KB, 4.2): Now

Collateral
Datasheets
CYBLE-022001-00 Datasheet
CYBLE-222005-00 Datasheet
CYBLE-222014-01 (BT 4.2) Datasheet
BLE Silicon Datasheet
App Notes/Evaluation Kit User Guides
Getting Started With EZ-BLE™ Module (AN96841)
PSoC Creator
PSoC Programmer
CySmart™ Windows Host Emulation Tool
CySmart iOS and Android Apps

¹ Bluetooth Special Interest Group Qualification Design ID
² Korea certification
³ Ministry of Internal Affairs and Communications (Japan)
⁴ Innovation, Science and Economic Development Canada
⁵ Serial wire debug communication protocol
⁶ VREF only available on 256KB module
⁷ A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
**EZ-BLE Creator Modules CYBLE-x140xx-0x**

BLE Modules Designed to Maximize System Integration with Integrated Analog Functionality

### Applications
Sports and fitness monitors, medical devices, wearable, electronics, home automation solutions, and game controllers

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, KC\(^2\), MIC\(^3\), and ISED\(^4\)
- **Small Footprint**
  - 11 mm x 11 mm x 1.8 mm, 32-SMT, 25 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
- **Highly Integrated Solution**
  - Two crystals, trace antenna, passives, shield
  - 128KB and 256KB flash sizes, with over-the-air (OTA) firmware upgrades
  - Preprogrammed with EZ-Serial firmware
- **Programmable Analog Blocks**
  - Four opamps and one 12-bit, 1-Msps SAR\(^5\) ADC
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable TCPWM\(^6\) blocks: 16-bit timer, counter, or PWM
  - Two configurable serial communication blocks for I^2^C/SPI/UART
- **1.3-µA Deep Sleep, 150-nA Hibernate, 60-nA Stop Power Modes**
- **CYBLE-x140xx-EVAL Kit for Fast Evaluation and Development**

### Availability
- **Sampling (4.1/128KB, 4.1/256KB, 4.2):** Now
- **Production (4.1/128KB, 4.1/256KB, 4.2):** Now

### Collateral
- **Datasheets**
  - CYBLE-014008-00 Datasheet
  - CYBLE-214009-00 Datasheet
  - CYBLE-214015-01 (BT 4.2) Datasheet
  - BLE Silicon Datasheet
- **App Notes/Evaluation Kit User Guides**
  - Getting Started With EZ-BLE™ Module (AN96841)
  - PSoC Creator
  - PSoC Programmer
  - CySmart® Windows Host Emulation Tool
  - CySmart iOS and Android Apps

---

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Korea Certification
\(^3\) Ministry of Internal Affairs and Communications (Japan)
\(^4\) Innovation, Science and Economic Development Canada
\(^5\) Successive approximation register
\(^6\) Timer/counter/pulse-width modulator

\(^7\) Serial wire debug communication protocol
\(^8\) A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE Creator Modules CYBLE-x120xx-xx
Cost-Optimized Bluetooth Low-Energy (BLE) Modules

Applications
Connectivity, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\) (CYBLE-012011-00/CYBLE-212019-00), FCC, CE, KC\(^2\), MIC\(^3\), and ISED\(^4\)
- Small Footprint
  - 14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 23 GPIO
- Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2
  - 2.4-GHz BLE radio and baseband
  - -91-dBm Rx sensitivity, +3-dBm Tx output power
- Power Modes
  - 1.3-µA Deep Sleep, 150-nA Hibernate, and 60-nA Stop
- Highly Integrated Solution
  - Two crystals, trace antenna, passives, shield\(^5\)
  - Preprogrammed with EZ-Serial firmware
- CYBLE-x120xx-EVAL Adapter Board Interface
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

Availability
Sampling (4.1/128KB, 4.1/256KB, 4.2): Now
Production (4.1/128KB, 4.1/256KB, 4.2): Now

Collateral

Datasheets
- CYBLE-012011-00 Datasheet
- CYBLE-212019-00 Datasheet
- CYBLE-212020-01 (BT 4.2) Datasheet
- BLE Silicon Datasheet

App Notes/Evaluation Kit User Guides
- Getting Started With EZ-BLE™ Module (AN96841)
- PSoC Creator
- PSoC Programmer
- CySmart? Windows Host Emulation Tool
- CySmart iOS and Android Apps

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Korea Certification
\(^3\) Ministry of Internal Affairs and Communications (Japan)
\(^4\) Innovation, Science and Economic Development Canada
\(^5\) CYBLE-012012-10 does not include metal shield
\(^6\) Serial wire debug communication protocol
\(^7\) A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
# EZ-BLE Creator XR Modules CYBLE-2x20xx-x1

**Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna**

## Applications

| BLE connectivity, lighting, industrial, and medical |

## Features

- **Qualification and Certification**
  - Bluetooth SIG QDID\(^2\), FCC, CE, MIC\(^3\), KC\(^4\), and ISED\(^5\)
- **Small Footprint**
  - 15.0 mm x 23.0 mm x 2.0 mm, 30-pad SMT with 19 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.2**
  - 2.4-GHz BLE radio and baseband
- **Industrial Temperature Range**
  - Operating temperature range from -40 °C to +85 °C
- **Long Range**
  - +7.5-dBm Tx output power, 400 meters line-of-sight range
  - -93-dBm Rx sensitivity
- **Highly Integrated Solution**
  - Two crystals, trace antenna (optional), power amplifier, passives
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-2x20xx-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

## Availability

| Sampling: Now | Production: Now |

---

1. Extended range
2. Bluetooth Special Interest Group Qualification Design ID
3. Ministry of Internal Affairs and Communications (Japan)
4. Innovation, Science and Economic Development Canada
5. Serial wire debug communication protocol
6. Serial wire debug communication protocol
7. A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
Cypress Roadmap: Modules – SHNG

**EZ-BLE Creator XT/XR1 Modules CYBLE-22411x-0x**

**Long-Range Bluetooth Low-Energy (BLE) Modules Supporting Extended Temperatures**

### Applications
- Connectivity, lighting, industrial, and medical

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^\text{2}\), FCC, CE, MIC\(^3\), KC\(^4\), and ISED\(^5\)
- **Small Footprint**
  - 9.5 mm x 15.4 mm x 1.8 mm, 32-pad SMT with 25 GPIOs
- **Bluetooth Smart Connectivity with Bluetooth 4.1 and 4.2**
  - 2.4-GHz BLE radio and baseband
- **Extended Industrial Temperature Range**
  - Operating temperature range from -40 °C to +105 °C
- **Long Range**
  - +9.5-dBm Tx output power, 400 meters line-of-sight range
  - -95-dBm Rx sensitivity
- **Highly Integrated Solution**
  - Two crystals, trace antenna, power amplifier, passives, shield
  - Preprogrammed with EZ-Serial firmware
- **CYBLE-22411x-EVAL Adapter Board Interface**
  - Easy interface to CY8CKIT-042-BLE Pioneer Kit
  - Enables testing of CapSense, buttons, GPIOs, over-the-air (OTA)

### Availability
- **Sampling (4.1/128KB, 4.2/256KB):** Now
- **Production (4.1/128KB, 4.2/256KB):** Now

### EZ-BLE Creator Module Family: CYBLE-22411x-0x

- **EZ-BLE Creator XT / XR Module**
  - 32.768-kHz Crystal
  - 24-MHz Crystal
  - Chip antenna
  - Power amplifier

### Collateral
- **Datasheet**
  - CYBLE-224110-00 Datasheet
  - BLE Silicon Datasheet
  - CYBLE-224116-01 (BT 4.2) Datasheet
- **App Notes/Evaluation Kit User Guides**
  - Getting Started With EZ-BLE™ Module (AN96841)
  - PSoC Creator
  - PSoC Programmer
  - CySmart\(^7\) Windows Host Emulation Tool
  - CySmart iOS and Android Apps

---

\(^{1}\) Extended temperature/extended range
\(^{2}\) Bluetooth Special Interest Group Qualification Design ID
\(^{3}\) Ministry of Internal Affairs and Communications (Japan)
\(^{4}\) Korea Certification
\(^{5}\) Ministry of Science and Economic Development Canada
\(^{6}\) Serial wire debug communication protocol
\(^{7}\) A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
EZ-BLE Creator Modules CYBLE-416045-02
Ultra-Low-Power Bluetooth Low-Energy (BLE) Module

Applications
- BLE connectivity, lighting, industrial, and medical

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 14.0 mm x 18.5 mm x 2.0 mm, 43-pad SMT with 36 GPIOs
- Bluetooth Smart Connectivity with Bluetooth 5.0
  - 2.4-GHz BLE radio and baseband
  - +4.0-dBm Tx output power, -95-dBm Rx sensitivity
- Industrial Temperature Range
  - Operating temperature range from -40 °C to +85 °C
- Power Modes
  - 5.7-mA TX (0 dBm) and 6.7-mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
  - Deep Sleep mode current with 64K SRAM retention is 7 μA with 3.3-V external supply and internal buck
  - On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 μA quiescent current
- Highly Integrated Solution
  - One crystal, trace antenna, passives

Availability
- Sampling: Now
- Production: Now

Collateral
- Datasheets
  CYBLE-416045-02 Datasheet
  BLE Silicon, PSoC 6 MCU: PSoC 63 with BLE Datasheet
- App Notes/Evaluation Kit User Guides
  Getting Started With EZ-BLE™ Module (AN96841)
- Cypress Tools
  PSoC Creator
  PSoC Programmer
  CySmart\(^6\) Windows Host Emulation Tool
  CySmart iOS and Android Apps

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada
4 Serial wire debug communication protocol
5 A GUI-based software tool that installs on your PC to test and debug BLE functionality; also available in iOS and Android mobile applications
**EZ-BLE WICED Modules CYBLE-0130xx-00**

**Cost-Optimized Bluetooth Low-Energy (BLE) WICED Modules**

### Features

<table>
<thead>
<tr>
<th>Qualification and Certification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bluetooth SIG QDID(^1), FCC, CE, MIC(^2), and ISED(^3)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Small Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>14.5 mm x 19.2 mm x 2.0 mm, 31-pad SMT with 16/18 GPIO</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bluetooth Smart Connectivity with Bluetooth 4.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.4-GHz BLE radio and baseband</td>
</tr>
<tr>
<td>-93-dBm Rx sensitivity, +4-dBm Tx output power</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Highly Integrated Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>One crystal, 128KB flash (CYBLE-013025-00), PCB antenna, shield</td>
</tr>
<tr>
<td>Simultaneous multiple Master and Slave (1M, 3S)</td>
</tr>
<tr>
<td>Security engine</td>
</tr>
<tr>
<td>Secure over-the-air (OTA) firmware upgrade (CYBLE-013025-00)</td>
</tr>
<tr>
<td>Preprogrammed with EZ-Serial firmware</td>
</tr>
</tbody>
</table>

| CYBLE-013025-EVAL Arduino Evaluation Board |

### Availability

**Sampling:** Now  
**Production:** Now

### Collateral

**Datasheets**  
CYBLE-0130xx-00 Datasheet

**Evaluation Kit User Guide**  
CYBLE-013025-EVAL Evaluation Board  
WICED SMART SDK \(2.x\) (Software)  
WICED SMART SDK \(2.x\) (Quick Start Guide)

---

1. Bluetooth Special Interest Group Qualification Design ID
2. Ministry of Internal Affairs and Communications (Japan)
3. Innovation, Science and Economic Development Canada
**EZ-BT WICED Module CYBT-343026-01**

**Cost-Optimized Bluetooth Smart Ready WICED Modules**

### Applications
- Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I\(^2\)S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

### Availability
- **Sampling:** Now
- **Production:** Now

---

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-3330xx-02
Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting External Antenna

Applications
Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
- Bluetooth Smart Ready with Bluetooth 5.0
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- Bluetooth SIG Mesh Supported
- Highly Integrated Solution
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/IPS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability
Sampling: Now
Production: Now

Datasheets
CYBT-333032-01 Datasheet
CYBT-333047-01 Datasheet

Evaluation Kit User Guide
CYBT-343047-EVAL Evaluation Board
WICED Studio

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada
**EZ-BT WICED Module CYBT-343151-02**

Cost-Optimized Bluetooth Smart Ready WICED Modules Supporting Extended Temperatures

---

### Applications

Connectivity, lighting, industrial, and medical

---

### Features

- **Qualification and Certification**
  - Bluetooth SIG QDID¹, FCC, CE, MIC², and ISED³
- **Small Footprint**
  - 12.0 mm x 15.5 mm x 1.95 mm, 24-pad SMT with 11 GPIOs
  - Drop-in compatible with CYBT-343026-01
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx Sensitivity, +9-dBm Tx output power
- **Extended Industrial Temperature Range**
  - Operating temperature range from -30°C to +105°C
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/I²S audio interface with wideband speech support
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

---

### Availability

Sampling: Now
Production: Now

---

¹ Bluetooth Special Interest Group Qualification Design ID
² Ministry of Internal Affairs and Communications (Japan)
³ Innovation, Science and Economic Development Canada

---

**Datasheets**
- CYBT-343151-02 Datasheet
- CYBT-343026-EVAL Evaluation Board
- WICED Studio
EZ-BT WICED Module CYBT-353027-02
Size-Optimized Bluetooth 5.0 WICED Module

Applications
- Bluetooth speaker, POS, medical, industrial, PC accessories, toys, and smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 9 mm x 9 mm x 1.75 mm, 19-pad SMT with 8 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -93.5-dBm Rx sensitivity, +12-dBm Tx output power
  - BLE: -96.5-dBm Rx sensitivity, +9-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - PCM/PS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability
- **Sampling:** Now
- **Production:** Now

Collateral
- **Datasheets**
  - CYBT-353027-02 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-353027-EVAL Board
  - WICED Studio

---
\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
## EZ-BT WICED Module CYBT-4230xx-02

**Ultra-Low-Power Size-Optimized Bluetooth 5.0 WICED Module**

### Applications

- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

### Features

- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)

- **Small Footprint**
  - 11 mm x 11 mm x 1.70 mm, 28-pad SMT with 17 GPIOs

- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power

- **Bluetooth SIG Mesh Supported**

- **Highly Integrated Solution**
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/I\(^2\)S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

### Availability

- **Sampling:** Now
- **Production:** Now

1. Bluetooth Special Interest Group Qualification Design ID
2. Ministry of Internal Affairs and Communications (Japan)
3. Innovation, Science and Economic Development Canada

### EZ-BT WICED Module Family: CYBT-4230xx-02

- **Power/Ground:** 4

- **XRES:**

- **XTALO_32K:**

- **24-MHz Crystal:**

- **Filter / Antenna:**

### Collateral

- **Datasheets**
  - CYBT-4230xx-02 Datasheet

- **Evaluation Kit User Guide**
  - CYBT-423028-EVAL Board
  - WICED Studio
**EZ-BT WICED Module CYBT-4130xx-02**  
**Ultra-Low-Power Cost-Optimized Bluetooth 5.0 WICED Module**

### Applications
- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID¹, FCC, CE, MIC², and ISED³
- **Small Footprint**
  - 12 mm x 16.3 mm x 1.70 mm, 30-pad SMT with 17 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 1MB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/I²S audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

### Availability
- **Sampling:** Now
- **Production:** Now

### Collateral
- **Datasheets**
  - CYBT-4130xx-02 Datasheet
- **Evaluation Kit User Guide**
  - CYBT-413034-EVAL Board
  - WICED Studio

---

¹ Bluetooth Special Interest Group Qualification Design ID  
² Ministry of Internal Affairs and Communications (Japan)  
³ Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-213043-02
Ultra-Low-Power Cost-Optimized Bluetooth 5.0 WICED Module

Applications
- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and
  PC/smartphone accessories

Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 12 mm x 16.61 mm x 1.70 mm, 35-pad SMT with 22 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR/EDR: -92.0-dBm Rx sensitivity, 0-dBm Tx output power
  - BLE: -95.5-dBm Rx sensitivity, 4-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 256KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/FS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2020)

Availability
- **Sampling:** Now
- **Production:** Q3 2020

\(^1\) Bluetooth Special Interest Group Qualification Design ID
\(^2\) Ministry of Internal Affairs and Communications (Japan)
\(^3\) Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-4830xx-02
Ultra-Long Range Bluetooth 5.0 WICED Module

Applications
Bluetooth audio, mesh, sensor hubs, and industrial

Features
- Qualification and Certification
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- Small Footprint
  - 12.75 mm x 18.59 mm x 1.8 mm, 34-pad SMT with 15 GPIOs
- Bluetooth Smart Ready with Bluetooth 5.0
  - BLE Tx output power up to 20 dBm for U.S. (FCC)
- Bluetooth SIG Mesh Supported
- Highly Integrated Solution
  - One crystal, 1MB flash, chip antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/PS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware

Availability
Sampling: Now
Production: Now

Collateral
Datasheets
CYBT-4830xx-02 Datasheet
Evaluation Kit User Guide
CYBT-483039-EVAL Board
WICED Studio

1 Bluetooth Special Interest Group Qualification Design ID
2 Ministry of Internal Affairs and Communications (Japan)
3 Innovation, Science and Economic Development Canada
**EZ-BT WICED Module CYBT-343052-02**

**Long Range Low Power Bluetooth 5.0 WICED Modules**

### Applications
- Remote, keyboard, Bluetooth audio, POS, medical, industrial, PC accessories, toys, and smartphone accessories

### Features
- **Qualification and Certification**
  - Bluetooth SIG QDID\(^1\), FCC, CE, MIC\(^2\), and ISED\(^3\)
- **Small Footprint**
  - 13.31 mm x 22.4 mm x 1.95 mm, 42-pad SMT with 24 GPIOs
- **Bluetooth Smart Ready with Bluetooth 5.0**
  - BR: -91.5-dBm Rx sensitivity, +1-dBm Tx output power
  - BLE: -94.5-dBm Rx Sensitivity, +12-dBm Tx output power
- **Bluetooth SIG Mesh Supported**
- **Highly Integrated Solution**
  - One crystal, 512KB flash, PCB antenna
  - 1x Microphone interface
  - Programmable key-scan matrix interface, up to 8 \(\times\) 20 key scanning matrix
  - 6x 16-bit PWMs
  - Simultaneous multiple Master and Slave
  - Secure over-the-air (OTA) firmware upgrade

### Availability
- **Sampling:** Now
- **Production:** Q3 2020

---

1. Bluetooth Special Interest Group Qualification Design ID
2. Ministry of Internal Affairs and Communications (Japan)
3. Innovation, Science and Economic Development Canada
EZ-BT WICED Module CYBT-243053-02
Ultra-Low-Power Cost-Optimized Long Range Bluetooth 5.0 WICED Module

Applications
- Bluetooth audio, mesh, sensor hubs, POS, medical, industrial, toys, and PC/smartphone accessories

Features
- Qualification and Certification
  - Bluetooth SIG QDID\textsuperscript{1}, FCC, CE, MIC\textsuperscript{2}, and ISED\textsuperscript{3}
- Small Footprint
  - 12 mm x 16.61 mm x 1.70 mm, 35-pad SMT with 22 GPIOs
- Bluetooth Smart Ready with Bluetooth 5.0
  - -94.5-dBm Rx sensitivity, 10.5-dBm Tx output power
- Bluetooth SIG Mesh Supported
- Highly Integrated Solution
  - One crystal, 256KB flash, PCB antenna
  - Two-wire Global Coexistence Interface (GCI)
  - Simultaneous multiple Master and Slave
  - PCM/PS audio interface with wideband speech support
  - Secure over-the-air (OTA) firmware upgrade
  - Preprogrammed with EZ-Serial firmware (Q4 2020)

Availability
- Sampling: Now
- Production: Q3 2020

Collateral
- Datasheets
  CYBT-243053-02 Datasheet
  CYBT-243053-EVAL Evaluation Board
- Evaluation Kit User Guide
  WICED Studio

\textsuperscript{1} Bluetooth Special Interest Group Qualification Design ID
\textsuperscript{2} Ministry of Internal Affairs and Communications (Japan)
\textsuperscript{3} Innovation, Science and Economic Development Canada

Sampling: Now
Production: Q3 2020
## EZ-BLE/EZ-BT Module Product Selector Guide

### EZ-BLE Module Part Numbering Decoder

<table>
<thead>
<tr>
<th>CY</th>
<th>BT</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>N</th>
<th>X</th>
</tr>
</thead>
</table>

- **Bluetooth Version:**
  - 0 = Bluetooth 4.1
  - 1 = Bluetooth 4.2
  - 2 = Bluetooth 5.0

- **Integration Type:**
  - 0 = Full Integration with Shield
  - 1 = No Shield

- **Device Identification #:**
  - Unique sequential product number for each module

- **Temperature Range:**
  - 0 = Industrial
  - 1 = Extended Industrial

- **EZ-BT Module Type:**
  - 2/4 = PSoC 4 Module
  - 3 = WICED Module
  - 6 = PSoC 6 Module

- **Antenna Type:**
  - 0 = No Antenna, Standard Range
  - 1 = PCB Antenna, Standard Range
  - 2 = Chip Antenna, Standard Range
  - 3 = No Antenna, Long Range (internal PA)
  - 4 = PCB Antenna, Long Range (internal PA)
  - 5 = Chip Antenna, Long Range (internal PA)
  - 6 = No Antenna, Long Range (external PA/LNA)
  - 7 = PCB Antenna, Long Range (external PA/LNA)
  - 8 = Chip Antenna, Long Range (external PA/LNA)

- **Flash Size:**
  - 0 = 128KB
  - 2 = 256KB
  - 3 = 512KB
  - 4 = 1024KB

- **Marketing Code:**
  - BLE = BLE Only Product
  - BT = Dual-Mode BT/LE Product

- **Company ID:**
  - CY = Cypress
MCU Portfolio Roadmap
## MCU Portfolio

<table>
<thead>
<tr>
<th></th>
<th>8-Bit</th>
<th>32-Bit Arm® Cortex®-M0/M0+</th>
<th>32-Bit Arm Cortex-M3</th>
<th>32-Bit Arm Cortex-M4 / Arm Cortex-M0+</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Analog Integration</td>
<td>8-/16-Bit Replacement</td>
<td>Mid-Range Performance</td>
<td>Ultra-Low-Power, Secure, High Performance</td>
<td></td>
</tr>
</tbody>
</table>

**PSoC** is a brand of Cypress MCUs for the broad-based embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing.

**FM** is a portfolio of high-performance Arm Cortex-M-based MCUs for industrial and consumer applications.

### FM4 MCUs
- **FM4 MCUs**
  - Cortex-M4
  - 200 MHz, 2MB Flash, 190 I/Os

### PSoC 6
- **PSoC 6**
  - 150 MHz Cortex-M4/100 MHz M0+
  - 2MB Flash
  - 7 PAB, 56 PDB, 104 I/Os

### FM3 MCUs
- **FM3 MCUs**
  - Cortex-M3
  - 144 MHz, 1.5MB Flash, 154 I/Os

### PSoC 4
- **PSoC 4**
  - Cortex-M0/M0+
  - 48 MHz, 384KB Flash
  - Up to 13 PAB, 20 PDB, 98 I/Os

### PSoC 3
- **PSoC 3**
  - 8051 CPU
  - 67 MHz, 64KB Flash
  - Up to 19 PAB, 30 PDB, 72 I/Os

### 8FX
- **8FX**
  - 8-bit RISC MCU
  - 16 MHz, 32–50KB Flash

### FM0+ MCUs
- **FM0+ MCUs**
  - Cortex-M0+
  - 40 MHz, 512KB Flash, 102 I/Os

### PSoC 1
- **PSoC 1**
  - M8C CPU
  - 24 MHz, 32KB Flash
  - 16 PAB, 16 PDB, 64 I/Os

### 8FX
- **8FX**
  - 8-bit RISC MCU
  - 16 MHz, 32–50KB Flash

---

1. A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters.
2. A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic.
## PSoC 6 MCU Portfolio

**Ultra-Low-Power | Flexibility | Hardware-Based Security and Root of Trust**

<table>
<thead>
<tr>
<th>PSoC 61 Line</th>
<th>Ultra-Low-Power and High-Performance MCU Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C61xA</td>
<td>Arm Cortex-M4</td>
</tr>
<tr>
<td></td>
<td>2MB/1MB1</td>
</tr>
<tr>
<td></td>
<td>DAC2, QSPI, FS-USB, SDHC2, DC-DC</td>
</tr>
<tr>
<td>NEW</td>
<td>Q220</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PSoC 62 Line</th>
<th>Ultra-Low-Power, Dual-Core, and High-Performance MCU Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C62xA</td>
<td>Arm Cortex-M4 &amp; Arm Cortex-M0+</td>
</tr>
<tr>
<td></td>
<td>2MB/1MB1</td>
</tr>
<tr>
<td></td>
<td>DAC, QSPI, FS-USB, SDHC, DC-DC</td>
</tr>
<tr>
<td>NEW</td>
<td>Q220</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PSoC 63 Line</th>
<th>High-Integration Wired/Wireless Connectivity MCU Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C63x7</td>
<td>Arm Cortex-M4 &amp; Arm Cortex-M0+</td>
</tr>
<tr>
<td></td>
<td>1MB/288KB</td>
</tr>
<tr>
<td></td>
<td>DAC, QSPI, UDB, BLE, DC-DC</td>
</tr>
<tr>
<td>NEW</td>
<td>Q320</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PSoC 64 Line</th>
<th>Ultra-Low-Power, Dual-Core, “Just Works” Secure Host MCU Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYB064xA</td>
<td>Arm Cortex-M4 &amp; Arm Cortex-M0+</td>
</tr>
<tr>
<td></td>
<td>2MB/1MB1</td>
</tr>
<tr>
<td></td>
<td>Secure-Boot MCU</td>
</tr>
<tr>
<td></td>
<td>SecureFlashboot, CY Secure Bootloader</td>
</tr>
<tr>
<td>NEW</td>
<td>Q320</td>
</tr>
</tbody>
</table>

### Roadmap

<table>
<thead>
<tr>
<th>New Products</th>
<th>CY8C61xA</th>
<th>CY8C62xA</th>
<th>CY8C63x7</th>
<th>CYB064xA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q220</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q320</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Status and Availability

- **Production** (QQYY)
- **Sampling** (QQYY)
- **Development**
- **Concept**

### Key Features

1. **Flash KB/SRAM KB**
2. **Digital to analog convertor**
3. **Quad-SPI**
4. **Full-Speed USB**
5. **Secure Digital Host Controller**
6. **Universal digital block – programmable logic**
7. **Controller Area Network Flexible Data-Rate**

### Secure MCUs

- **CYB064xA**
- **CYB0647BJI-DS4**
- **CYB0647BZI-BLD53**
- **CYB0647ZI-BLD53**

### AWS Secure MCUs

- **CYB0647ZI-BLD53**

---

*MCU PORTFOLIO – WKA*
<table>
<thead>
<tr>
<th>PSoC 4 Portfolio</th>
<th>Flexibility</th>
<th>CapSense®</th>
<th>Ease-of-Use</th>
</tr>
</thead>
</table>

### PSoC MCUs
- **PSoC 4000**
- **PSoC 4100**
- **PSoC 4200**
- **PSoC 4300**
- **PSoC 4400**
- **PSoC 4500**
- **PSoC 4700**

### Programmable Digital
- **PSoC 4200**
- **PSoC 4300**
- **PSoC 4400**
- **PSoC 4500**
- **PSoC 4700**

### Analog Coprocessor
- **PSoC 4200**
- **PSoC 4300**
- **PSoC 4400**
- **PSoC 4500**
- **PSoC 4700**

### Application Specific
- **PSoC 4000**
- **PSoC 4100**
- **PSoC 4200**
- **PSoC 4300**
- **PSoC 4400**
- **PSoC 4500**
- **PSoC 4700**

### Performance and Integration
- **BL = BLE-Series**
- **S = S-Series**
- **M = M-Series**
- **L = L-Series**

---

1. **Flash KB/SRAM KB**
2. **Comparator**
3. **Analog-to-digital converter**
4. **Serial communication block**
5. **Current-output DAC**
6. **Embedded programmable digital logic in the I/O subsystem**
7. **Bluetooth Low Energy**
8. **Universal digital block**
9. **Controller area network**
10. **Universal analog block**
11. **Motor Control Accelerator**
12. **Multi-sense converter**

### Availability
- **Concept**
- **Development**
- **Sampling**
- **Production**

---

**MCU PORTFOLIO – WKA**

27
## PSoC® 5LP Portfolio

### MCU PORTFOLIO – WKA

#### Programmed Digital PSoC 5200
- Analog: 1x ADC\(^1\), 1x DAC\(^2\), 2x CMP\(^3\), 0.9% \(V_{REF}\)
- Interfaces: USB, FF\(^4\) IC

#### Intelligent Analog PSoC 5400
- Analog: 1x ADC, 2x DAC, 4x CMP, 2x Opamps, 2x SC/CT PAB\(^5\), 0.9% \(V_{REF}\)
- Interfaces: USB, FF IC

#### Performance Analog PSoC 5600
- Analog: 2x ADC, 4x DAC, 4x CMP, 4x Opamps, DFB\(^6\), 4x SC/CT PAB, 0.1% \(V_{REF}\)
- Interfaces: USB, FF IC, CAN\(^7\)

#### Precision Analog PSoC 5800
- Analog: 2x/3x ADC, 4x DAC, 4x CMP, 4x Opamps, DFB, 4x SC/CT PAB, 0.1% \(V_{REF}\)
- Interfaces: USB, FF IC

### CPU Speed and Flash

<table>
<thead>
<tr>
<th>CPU Speed and Flash</th>
<th>Analog</th>
<th>Fixed function</th>
<th>Switched capacitor/continuous time programmable analog block</th>
<th>Digital filter block</th>
<th>Comparator</th>
<th>Flash KB/SRAM KB/EEPROM KB</th>
<th>Delta-Sigma ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C5268</td>
<td>80 MHz, 256K/64K/2K</td>
<td>12b SAR ADC</td>
<td>24x UDB, 99-CSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5268</td>
<td>67 MHz, 128K/32K/2K</td>
<td>12b SAR ADC</td>
<td>24x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5266</td>
<td>67 MHz, 64K/16K/2K</td>
<td>12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5265</td>
<td>67 MHz, 32K/8K/2K</td>
<td>12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5468</td>
<td>80 MHz, 256K/64K/2K</td>
<td>12b SAR ADC</td>
<td>24x UDB, 99-CSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5467</td>
<td>67 MHz, 128K/32K/2K</td>
<td>12b SAR ADC</td>
<td>24x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5466</td>
<td>67 MHz, 64K/16K/2K</td>
<td>12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5465</td>
<td>67 MHz, 32K/8K/2K</td>
<td>12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5668</td>
<td>80 MHz, 256K/64K/2K</td>
<td>2x 12b SAR ADC</td>
<td>24x UDB, 99-CSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5667</td>
<td>67 MHz, 128K/32K/2K</td>
<td>12b ΔΣ ADC, 12b SAR/2x 12b SAR ADC</td>
<td>24x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5666</td>
<td>67 MHz, 64K/16K/2K</td>
<td>12b ΔΣ ADC, 12b SAR ADC</td>
<td>24x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5665</td>
<td>67 MHz, 32K/8K/2K</td>
<td>12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5668</td>
<td>80 MHz, 256K/64K/2K</td>
<td>20b ΔΣ ADC, 2x 12b SAR ADC</td>
<td>24x UDB, 99-CSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5667</td>
<td>67 MHz, 128K/32K/2K</td>
<td>20b ΔΣ ADC, 12b SAR ADC</td>
<td>24x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5666</td>
<td>67 MHz, 64K/16K/2K</td>
<td>20b ΔΣ ADC, 12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C5665</td>
<td>67 MHz, 32K/8K/2K</td>
<td>20b ΔΣ ADC, 12b SAR ADC</td>
<td>20x UDB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Analog-to-digital converter  
\(^2\) Digital-to-analog converter  
\(^3\) Comparator  
\(^4\) Fixed function  
\(^5\) Switched capacitor/continuous time programmable analog block  
\(^6\) Digital filter block  
\(^7\) Controller area network  
\(^8\) Flash KB/SRAM KB/EEPROM KB  
\(^9\) Universal digital block  
\(^10\) Chip-scale package  
\(^11\) Delta-Sigma ADC

---

**Status**

- **Concept**
- **Development**
- **Sampling**
- **Production**

**Availability**

- **QTY**
- **QTY**
### FM4® and FM0+® MCU Portfolio

**Arm® Cortex®-M4 and Arm Cortex-M0+**

#### Ultra-Low-Power

<table>
<thead>
<tr>
<th>Series</th>
<th>CPU Speed</th>
<th>CoreMark</th>
<th>Voltage</th>
<th>Flash</th>
<th>SDRAM</th>
<th>Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>S6E1A-Series</td>
<td>40 MHz, 2.7–5.5 V</td>
<td>88K/6K, 32/48 Pins</td>
<td>70 µA/MHz</td>
<td>88K/6K, 32/48 Pins</td>
<td>70 µA/MHz</td>
<td></td>
</tr>
<tr>
<td>S6E1C-Series</td>
<td>40 MHz, 1.7–3.6 V</td>
<td>128K/16K, 26/32/48/64 Pins</td>
<td>40 µA/MHz</td>
<td>128K/16K, 26/32/48/64 Pins</td>
<td>40 µA/MHz</td>
<td></td>
</tr>
</tbody>
</table>

#### High Performance

<table>
<thead>
<tr>
<th>Series</th>
<th>CPU Speed</th>
<th>CoreMark</th>
<th>Voltage</th>
<th>Flash</th>
<th>SDRAM</th>
<th>Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY9BFx6xM/R-Series</td>
<td>160 MHz, 540 CoreMark, 2.7–5.5 V</td>
<td>1M/128K, 32KB Work Flash</td>
<td>80/100/120 Pins</td>
<td>1M/128K, 32KB Work Flash</td>
<td>80/100/120 Pins</td>
<td></td>
</tr>
<tr>
<td>CY9BFx6xK/L-Series</td>
<td>180 MHz, 608 CoreMark, 2.7–5.5 V</td>
<td>512K/64K, 32KB Work Flash</td>
<td>80/100/120 Pins</td>
<td>512K/64K, 32KB Work Flash</td>
<td>80/100/120 Pins</td>
<td></td>
</tr>
</tbody>
</table>

1. Flash KB/ SRAM KB
2. Independent flash memory available to store data or additional firmware
3. Active power consumption
Midrange Performance

- CY9BFx2xS/T-Series
  - 60 MHz, 2.7–5.5 V
  - 1.5M/192K\(^1\), 64KB Work Flash\(^2\)
  - 144/176 Pins

- CY9BFx1xS/T-Series
  - 144 MHz, 2.7–5.5 V
  - 1M/128K, 144/176 Pins

- CY9BFx1xN/R-Series
  - 144 MHz, 2.7–5.5 V
  - 512K/64K, 32KB Work Flash, 100/120 Pins

- CY9AFx2xK/L-Series
  - 40 MHz, 2.7–5.5 V
  - 512K/32K, 80/100 Pins

- CY9AFx5xM/N/R-Series
  - 40 MHz, 1.7–3.6 V
  - 512K/64K, 32KB Work Flash
  - 80/100/120 Pins

- CY9AFx4xL/M/N-Series
  - 40 MHz, 1.7–3.6 V
  - 256K/32K, 32KB Work Flash
  - 64/80/100 Pins

- CY9AFx3xK/L-Series
  - 20 MHz, 1.8–5.5 V
  - 128K/8K, 48/64 Pins

- CY9AFx1xL/M/N-Series
  - 40 MHz, 2.7–5.5 V
  - 256K/32K, 64/80/100 Pins

- CY9AFx1xK-Series
  - 40 MHz, 2.7–5.5 V
  - 128K/16K, 32KB Work Flash
  - 48 Pins

- CY9AFx2xK/L-Series
  - 40 MHz, 2.7–5.5 V
  - 64K/4K, 48/64 Pins

- CY9AFx2xK/L-Series
  - 20 MHz, 1.8–5.5 V
  - 128K/8K, 48/64 Pins

- CY9AFx1xK-Series
  - 40 MHz, 2.7–5.5 V
  - 128K/16K, 32KB Work Flash
  - 48 Pins

- CY9BFx2xK/L-M-Series
  - 72 MHz, 2.7–5.5 V
  - 256K/32K, 32KB Work Flash
  - 48/64/80 Pins

- CY9BF121J-Series
  - 72 MHz, 2.7–5.5 V
  - 64K/8K, 32 Pins

\(^1\) Flash KB/SRAM KB
\(^2\) Independent flash memory available to store data or additional firmware
<table>
<thead>
<tr>
<th>Programmable Digital PSoC 3200</th>
<th>Intelligent Analog PSoC 3400</th>
<th>Performance Analog PSoC 3600</th>
<th>Precision Analog PSoC 3800</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog: $\Delta\Sigma$ ADC(^1), 1x DAC(^2), 2x CMP(^3), 0.9% $V_{\text{REF}}$</td>
<td>Analog: $\Delta\Sigma$ ADC, 2x DAC, 4x CMP, 2x Opamps, 2x SC/CT PAB(^4), 0.9% $V_{\text{REF}}$</td>
<td>Analog: $\Delta\Sigma$ ADC, 2x4x DAC, 0x/2x/4x CMP, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% $V_{\text{REF}}$</td>
<td>Analog: $\Delta\Sigma$ ADC, 2x4x DAC, 0x/2x/4x CMP, 0x/2x/4x Opamps, 0x/2x/4x SC/CT PAB, 0.1% $V_{\text{REF}}$</td>
</tr>
<tr>
<td>Interfaces: FF(^5) I^C</td>
<td>Interfaces: FF I^C</td>
<td>Interfaces: FF, FF I^C</td>
<td>Interfaces: USB, FF I^C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CY8C3244</th>
<th>CY8C3245</th>
<th>CY8C3246</th>
<th>CY8C3665</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 MHz, 64K/8K/2K</td>
<td>50 MHz, 64K/8K/2K</td>
<td>50 MHz, 64K/8K/2K</td>
<td>67 MHz, 64K/8K/2K</td>
</tr>
<tr>
<td>12b ADC</td>
<td>12b ADC</td>
<td>12b ADC</td>
<td>12b ADC</td>
</tr>
<tr>
<td>2x UDB, USB, 72-CSP</td>
<td>2x UDB, USB, 72-CSP</td>
<td>2x UDB, USB, 72-CSP</td>
<td>0x/1x DFB(^7), 12b ADC</td>
</tr>
<tr>
<td>0x/2x/4x UDB(^8), CAN(^9)</td>
<td>20x UDB, USB</td>
<td>24x UDB, USB, CAN</td>
<td>20x24x UDB, CAN, 72-CSP(^{10})</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CY8C3444</th>
<th>CY8C3445</th>
<th>CY8C3446</th>
<th>CY8C3666</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 MHz, 16K/2K/0.5K</td>
<td>50 MHz, 16K/2K/0.5K</td>
<td>50 MHz, 16K/2K/0.5K</td>
<td>50 MHz, 64K/8K/2K</td>
</tr>
<tr>
<td>12b ADC</td>
<td>12b ADC</td>
<td>12b ADC</td>
<td>12b ADC</td>
</tr>
<tr>
<td>16x UDB</td>
<td>16x UDB</td>
<td>16x UDB</td>
<td>0x/1x DFB, 20b ADC</td>
</tr>
<tr>
<td>16x UDB</td>
<td>20x UDB</td>
<td>20x UDB</td>
<td>16x/20x UDB</td>
</tr>
</tbody>
</table>

1. Delta-Sigma analog-to-digital converter
2. Digital-to-analog converter
3. Comparator
4. Digital filter block
5. Fixed function
6. Flash KB/SRAM KB/EPPROM KB
7. Universal digital block
8. Controller area network
9. Chip-scale package
10. Programmable Analog Block

**CPU Speed and Flash**

**Status Availability**

- Concept
- Development
- Sampling
- Production
## PSOC® 1 Portfolio

### M8C CPU | 24 MHz

<table>
<thead>
<tr>
<th>PSOC MCU</th>
<th>Programmable Digital</th>
<th>Intelligent Analog</th>
<th>Performance Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C24x93 32K/2K, 36 GPIOs</td>
<td>CY8C24x94 16K/1K, 56 GPIOs CapSense, 4x PDB, 2x CMP 2x14-bit SAR ADC, 6x SC/CT PAB</td>
<td>CY8C28xxx 16K/1K, 44 GPIOs CapSense, 12x PDB, 4x CMP 4x14-bit ΔΣ ADC, 16x SC/CT PAB</td>
<td>CY8C28xxx 16K/1K, 44 GPIOs CapSense, 8x PDB, 4x CMP 4x14-bit ΔΣ ADC, 16x SC/CT PAB</td>
</tr>
<tr>
<td>CY8C21x34 8K/0.5K, 26 GPIOs</td>
<td>CY8C21x34 8K/0.5K, 26 GPIOs CapSense, 4x PDB, 2x CMP 1x10-bit Single-Slope ADC, 4x SC/CT PAB</td>
<td>CY8C28xxx 16K/1K, 44 GPIOs CapSense, 12x PDB, 4x CMP 4x14-bit ΔΣ ADC, 16x SC/CT PAB</td>
<td>CY8C28xxx 16K/1K, 44 GPIOs CapSense, 8x PDB, 4x CMP 4x14-bit ΔΣ ADC, 16x SC/CT PAB</td>
</tr>
<tr>
<td>CY8C23x33 4K/0.25K, 16 GPIOs</td>
<td>CY8C23x33 4K/0.25K, 16 GPIOs CapSense, 4x PDB, 1x CMP 1x8-bit SAR ADC, 4x SC/CT PAB</td>
<td>CY8C24x23 4K/0.25K, 24 GPIOs CapSense, 4x PDB, 2x CMP 1x14-bit ΔΣ ADC, 6x SC/CT PAB</td>
<td>CY8C24x23 4K/0.25K, 24 GPIOs CapSense, 4x PDB, 2x CMP 1x14-bit ΔΣ ADC, 6x SC/CT PAB</td>
</tr>
<tr>
<td>CY8C21x23 4K/0.25K, 16 GPIOs</td>
<td>CY8C21x23 4K/0.25K, 16 GPIOs CapSense, 4x PDB, 2x CMP 1x10-bit Single-Slope ADC, 4x SC/CT PAB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Flash KB/SRAM KB
2. General purpose input/output pins
3. Comparator
4. Delta-Sigma ADC
5. Programmable digital block
6. Switched capacitor/continuous time programmable analog block
7. Successive approximation register ADC

<table>
<thead>
<tr>
<th>Status</th>
<th>Concept</th>
<th>Development</th>
<th>Sampling</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>Availability</td>
<td>QQYY</td>
<td>QQYY</td>
<td>QQYY</td>
<td>QQYY</td>
</tr>
</tbody>
</table>

32 MCU PORTFOLIO – WKA
### 8FX® MCU Portfolio

#### 8-Bit RISC CPU

<table>
<thead>
<tr>
<th>Series</th>
<th>32-Pin</th>
<th>48-/52-Pin</th>
<th>64-Pin</th>
<th>80-Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB95630H</td>
<td>16 MHz, 2.4–5.5 V 32/1/4</td>
<td>MB95690K</td>
<td>16 MHz, 2.8–5.5 V 56/2/4</td>
<td>MB95770M</td>
</tr>
<tr>
<td>MB95690K</td>
<td>16 MHz, 2.8–5.5 V 56/2/4</td>
<td>MB95810K</td>
<td>16 MHz, 2.8–5.5 V 56/2/4</td>
<td>MB95710M</td>
</tr>
</tbody>
</table>

1. Flash KB/SRAM KB/work flash KB; work flash is independent flash memory available to store data or additional firmware.

#### Status

- Concept
- Development
- Sampling
- Production

#### Availability

- QQYY
- QQYY
- QQYY
- QQYY
# CapSense® Portfolio

<table>
<thead>
<tr>
<th>CapSense Express™</th>
<th>CapSense Plus™</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Configurable Controllers</strong>&lt;sup&gt;1&lt;/sup&gt;</td>
<td><strong>Programmable Controllers</strong>&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>CY8CMBR3106S</td>
<td>CY8C20xx7</td>
</tr>
<tr>
<td>11 Buttons, 2 Sliders</td>
<td>31 Buttons, 6 Sliders</td>
</tr>
<tr>
<td>Proximity, Liquid Tolerance</td>
<td>16, 32KB Flash</td>
</tr>
<tr>
<td>SmartSense_EMCPlus™&lt;sup&gt;3&lt;/sup&gt;</td>
<td>Proximity, Liquid Tolerance</td>
</tr>
<tr>
<td>CY8CMBR3108</td>
<td>CY8C20xx6A/S</td>
</tr>
<tr>
<td>8 Buttons, 4 LEDs</td>
<td>33 Buttons, 6 Sliders</td>
</tr>
<tr>
<td>Proximity, Liquid Tolerance</td>
<td>16, 32KB Flash, 2KB SRAM</td>
</tr>
<tr>
<td>SmartSense_EMCPlus™</td>
<td>SmartSense Auto-tuning</td>
</tr>
<tr>
<td>CY8CMBR3102</td>
<td>CY8C21x34/B</td>
</tr>
<tr>
<td>2 Buttons, Proximity</td>
<td>24 Buttons, 4 Sliders</td>
</tr>
<tr>
<td>SmartSense_EMCPlus™</td>
<td>8KB Flash</td>
</tr>
<tr>
<td>CY8CMBR2044</td>
<td>CY8C20xx8H</td>
</tr>
<tr>
<td>4 Buttons, 4 LEDs</td>
<td>25 Buttons, 5 Sliders</td>
</tr>
<tr>
<td>SmartSense Auto-tuning</td>
<td>8, 16KB Flash</td>
</tr>
<tr>
<td>CY8CMBR2010</td>
<td>CY8C20xx6H</td>
</tr>
<tr>
<td>10 Buttons, 10 LEDs</td>
<td>25 Buttons, 5 Sliders</td>
</tr>
<tr>
<td>SmartSense Auto-tuning</td>
<td>8, 16KB Flash</td>
</tr>
<tr>
<td>CY8CMBR2016</td>
<td>CY8C20xx6H</td>
</tr>
<tr>
<td>16 Buttons</td>
<td>25 Buttons, 5 Sliders</td>
</tr>
<tr>
<td>SmartSense Auto-tuning</td>
<td>8, 16KB Flash</td>
</tr>
<tr>
<td>CY8CMBR3002</td>
<td>CY8C20xx34</td>
</tr>
<tr>
<td>2 Buttons, 2 LEDs</td>
<td>25 Buttons, 6 Sliders</td>
</tr>
<tr>
<td>SmartSense_EMCPlus™</td>
<td>8KB Flash</td>
</tr>
</tbody>
</table>

1 Standard products that are configured for target applications with a graphical user interface
2 Microcontroller-based products that can be freely programmed to implement additional functions
3 SmartSense Electromagnetic Compatible = SmartSense Auto-tuning + high noise immunity

---

1 Standard products that are configured for target applications with a graphical user interface
2 Microcontroller-based products that can be freely programmed to implement additional functions
3 SmartSense Electromagnetic Compatible = SmartSense Auto-tuning + high noise immunity
**PSOC® 61 Line**

### Applications
- IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

### Features
- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4
  - Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA
- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 2 x 12-bit SAR ADC (1 MspS)
- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)\(^1\)
  - 12 x serial communication blocks (SCBs)\(^2\), deep-sleep SCB
  - 2 x I²S and PDM-PCM\(^3\) converter, SMIF\(^4\), 2 x CAN\(^5\)
  - 2 x SDHC blocks
  - USB 2.0 (Host and Device)
- **Security Features**
  - Advanced cryptographic coprocessor (Crypto) and True random number generator
  - One-time programmable eFUSE\(^6\) for secure key storage
  - Secure over-the-air (OTA) firmware update with read-while-write Flash technology for firmware updates
- **I/O Subsystem**: Up to 104 GPIOs
- **Packages**: 124-BGA, 100-WLCSP, 128-TQFP, 100-TQFP, 80-TQFP, 80-WLCSP, 68-QFN, 64-TQFP, 49-WLCSP

### Collateral
- **Datasheet**: [PSOC 6 Product Page](#)

### Availability

<table>
<thead>
<tr>
<th>Model</th>
<th>Sampling</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C61x4</td>
<td>Q121</td>
<td>Q121</td>
</tr>
<tr>
<td>CY8C61x5</td>
<td>Now</td>
<td>Q220</td>
</tr>
<tr>
<td>CY8C61x7</td>
<td>Now</td>
<td>Now</td>
</tr>
<tr>
<td>CY8C61xA</td>
<td>Now</td>
<td>Q220</td>
</tr>
</tbody>
</table>

\(^1\) Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
\(^2\) Configurable as a UART, SPI, or I²C interface
\(^3\) Digital microphone interface
\(^4\) Serial memory interface for execute-in-place, encrypted Quad-SPI
\(^5\) Controller Area Network
\(^6\) One-time programmable bits for secure key storage
\(^7\) Single-Precision Floating-Point Unit
**MCU Subsystem**
- Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
- Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
- Up to 2MB Flash, 1MB SRAM with DMA

**Analog Blocks**
- 2 opamps, 2 low-power comparators (CMP), 2 x 12-bit SAR ADC (1 Msps)
- 12-bit DAC, CapSense® capacitive-sensing block

**Digital Blocks and Communication Interfaces**
- 12 universal digital blocks (UDBs): custom digital peripherals
- 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)^
- 12 serial communication blocks (SCBs), deep-sleep SCB
- 2 I²S and PDM-PCM converter, SMIF, 2 x CAN
- 2 SDHC blocks
- USB 2.0 (Host and Device)

**Security Features**
- Advanced cryptographic coprocessor (Crypto) and True random number generator
- One-time programmable eFUSE^6 for secure key storage
- Secure over-the-air (OTA) firmware update with read-while-write Flash technology for firmware updates

**I/O Subsystem**
- Up to 104 GPIOs

**Packages**
- 124-BGA, 100-WLCSP, 128-TQFP, 100-TQFP, 80-TQFP, 80-WLCSP, 68-QFN, 64-TQFP, 49-WLCSP

**Features**

**Applications**
- IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

**Collateral**
- **Datasheet**: [PSoC 6 Product Page](#)
**MCU Subsystem**
- Dual-core architecture: 150-MHz Arm® Cortex®-M4 and 100-MHz Arm Cortex-M0+
- Ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
- Up to 1MB Flash, 288KB SRAM with a DMA controller

**Analog Blocks**
- Two opamps, two low-power comparators (CMPs), 12-bit SAR ADC (1-Mmps)
- 12-bit DAC, CapSense® capacitive-sensing block

**Digital Blocks and Communication Interfaces**
- Eight serial communication blocks (SCBs)², deep sleep SCB
- I²S and PDM-PCM³ converter, SMIF⁴

**Bluetooth Smart Connectivity**
- Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput

**Security Features**
- Advanced cryptographic coprocessor (Crypto), true random number generator
- One-time programmable eFuse⁵ for secure key storage
- Secure over-the-air (OTA) firmware update with read-while-write flash technology for firmware updates

**I/O Subsystem**
- Up to 78 GPIOs

**Applications**
- Wearables, portable medical, industrial IoT, and smart home

**Features**

**Datasheet:** PSoC® 6 Product Page

---

³ Configurable as a UART, SPI or I²C interface
² Configurable as a 8-bit, 16-bit timer, or 32-bit counter or PWM
⁴ Serial memory interface for execute-in-place, encrypted Quad-SPI
⁵ One-time programmable bits for secure key storage
⁶ Single-precision floating-point unit
PSoC® 64 Secure Boot MCU Line with BLE

**Applications**
Wearables, portable medical, industrial IoT, and smart home

**Features**

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9-V) and low-power (1.1-0V) operation mode
  - Up to 1MB Flash, 288KB SRAM with DMA

- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Advanced hardware cryptographic acceleration and TRNG
  - CY Secure Bootloader for secure firmware updates

- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Mps)
  - 12-bit DAC, CapSense® capacitive-sensing block

- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)1
  - 8 x serial communication blocks (SCBs)2, deep-sleep SCB
  - I2S and PDM-PCM3 converter, SMIF4

- **Bluetooth Smart Connectivity**
  - Bluetooth Low Energy (BLE) 5.0 radio with 2-Mbps data throughput

- **I/O Subsystem**: Up to 78 GPIOs

**Collateral**

Preliminary Datasheet: [PSoC 6 Product Page](#)

**Availability**

Sampling: Now  Production: Q320

---

1 Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2 Configurable as a UART, SPI, or I²C interface
3 Digital microphone interface
4 Serial memory interface for execute-in-place, encrypted Quad-SPI
5 One-time programmable bits for secure key storage
6 Single-Precision Floating-Point Unit
PSoC® 64 Secure Boot MCU Line

Applications
IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

Features

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA

- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Advanced hardware cryptographic acceleration and TRNG
  - CY Secure Bootloader for secure firmware updates

- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Msps)

- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)<sup>1</sup>
  - 8 x serial communication blocks (SCBs)<sup>2</sup>, deep-sleep SCB
  - I²S and PDM-PCM<sup>3</sup> converter, SMIF<sup>4</sup>
  - USB 2.0 (Host and Device)

- **I/O Subsystem**: Up to 104 GPIOs

Collateral

- Preliminary Datasheet: [PSoC 6 Product Page](#)

Availability

- **Sampling**: Now
- **Production**: Q320

---

<sup>1</sup> Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM

<sup>2</sup> Configurable as a UART, SPI, or I²C interface

<sup>3</sup> Digital microphone interface

<sup>4</sup> Serial memory interface for execute-in-place, encrypted Quad-SPI

<sup>5</sup> One-time programmable bits for secure key storage
PSoC® 64 Standard Secure MCU Line

**Applications**

IoT gateways, smart home, home appliances, HMI, audio processing, and industrial concentrators

**Features**

- **MCU Subsystem**
  - 150-MHz Arm® Cortex®-M4 with ultra-low-power (0.9 V) and low-power (1.1 V) operation mode
  - Up to 2MB Flash, 1MB SRAM with DMA

- **CY Secure Enclave**
  - Hardware isolated, 100-MHz Arm Cortex®-M0+ with privileged access to memory and peripherals
  - Hardware isolated keys, cryptographic functions and trusted applications
  - Hardware root-of-trust providing secure device identity
  - Secure boot with attestation and anti-rollback
  - Cypress ‘Just Works’ trusted O/S integrated with AWS/others cloud tool-kits (TLS, PKCS11 and FOTA)
  - Advanced hardware cryptographic acceleration and TRNG

- **Analog Blocks**
  - 2 x opamps, 2 x low-power comparators (CMP), 12-bit SAR ADC (1-Msps)
  - 12-bit DAC, CapSense® capacitive-sensing block

- **Digital Blocks and Communication Interfaces**
  - 12 x universal digital blocks (UDBs): custom digital peripherals
  - 24 x 16-bit and 8 x 32-bit timer/counter/pulse-width modulation blocks (TCPWM)¹
  - 8 x serial communication blocks (SCBs)², deep-sleep SCB
  - I²S and PDM-PCM³ converter, SMIF⁴
  - USB 2.0 (Host and Device)

- **I/O Subsystem**: Up to 104 GPIOs

**Collateral**

Preliminary Datasheet: [PSoC 6 Product Page](#)

**Availability (AWS Version)**

Sampling: Now  |  Production: Q320

1 Configurable as an 8-bit, 16-bit timer, or 32-bit counter or PWM
2 Configurable as a UART, SPI, or I²C interface
3 Digital microphone interface
4 Serial memory interface for execute-in-place, encrypted Quad-SPI
5 One-time programmable bits for secure key storage
6 Single-Precision Floating-Point Unit
**PSoC® 4000S**

**PSoC 4 MCU Entry Line**

**Applications**
Consumer devices (wearable, mobile, personal care) and small home appliances (coffee machine, juicer)

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - 32KB flash (maximum)
  - 4KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope ADC
  - Two low-power comparators (CMPs)
  - One CapSense® block that supports low-power operation and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) that are configurable as I2C, SPI, or UART

- **Packages**
  - 25-ball WLCSP, 24-pin QFN, 32-pin QFN, 48-pin TQFP

- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os

**Collateral**

- **Datasheet:** [PSoC 4000S](#)

**Availability**

- **Production:** Now

---

1. A simple ADC used to measure slow-moving signals
2. Embedded programmable digital logic in the I/O subsystem
**PSoc® 4100S**

**PSoc 4 MCU Base Line**

**Applications**
- Home appliances (washing machine, dishwasher) and industrial applications

**Features**
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB flash
  - 8KB SRAM
  - Real-time clock capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - One 10-bit, 46.8-ksps single-slope ADC¹
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
- **Packages**
  - 35-ball WLCSP, 32-pin QFN, 40-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 36 GPIOs, including 16 Smart I/Os²

**Collateral**
- Datasheet: [PSoc 4100S](#)

**Availability**
- Production: Now

---

¹ A simple ADC used to measure slow-moving signals
² Embedded programmable digital logic in the I/O subsystem
MCU PORTFOLIO – WKA

**PSOC® 4100S Plus**
**PSOC 4 MCU Base Line**

**Features**
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 128KB flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)
  - True random number generator (TRNG)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Mmps SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I2C, SPI, or UART
  - Segment LCD
- **One Controller Area Network (CAN) Controller**
- **Packages**
  - Up to 54 GPIOs, including 24 Smart I/Os
- **I/O Subsystem**
  - Up to 54 GPIOs, including 24 Smart I/Os

**Collateral**

Datasheet: [PSoc 4100s Plus](#)

**Availability**

Production: Now

---

1 Embedded programmable digital logic in the I/O subsystem
PSoc® 4100PS
PSoc 4 MCU Base Line

Applications
Consumer products and industrial applications

Features
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Up to 32KB flash, 4KB SRAM, RTC capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit/1-MspS SAR ADC
  - One 10-bit/11.6-kspS single-slope ADC
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIAs), etc.
  - Two low-power comparators
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 13-bit voltage output digital-to-analog converters (VDACs)
  - Two 7-bit current-output digital-to-analog converters (IDACs) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Eight 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
- **Packages**
  - 28-pin SSOP, 45-ball WL CSP, 48-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 38 GPIOs, including 8 Smart I/Os

Collateral
Datasheet: PSoC 4100PS

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem

PSoc® 4 One-Chip Solution

MCU Subsystem
- Arm® Cortex®-M0+ 48 MHz
- Flash (16KB to 32KB)
- SRAM (4KB)
- DMA
- WCO
- Serial Wire Debug

Programmable Analog Blocks
- Opamp x4
- SAR ADC
- CMP x2
- 7-bit IDAC x2
- AMUX x36
- Single-Slope ADC
- CapSense
- 13-bit VDAC x5

Programmable Digital Blocks
- TCPWM x8
- SCB x3
- GPIO x8
- GPIO x6

I/O Subsystem
- GPIO x8
- GPIO x8
- GPIO x6

Programmable Interconnect and Routing

Availability
Production: Now

MCU PORTFOLIO – WKA
PSOC® 4200DS

PSOC 4 MCU Programmable Line

Applications
Main system control with programmable communications, subsystem control with programmable
digital functions, digital sensor hub, low-end field oriented control (FOC) motor control, CPLD SoC,
and any other embedded control without ADC/DAC

Features
- 32-bit MCU Subsystem
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller
  - Up to 64KB flash, 8KB SRAM
- Programmable Analog Blocks
  - Two low-power comparators (CMPs)
- Programmable Digital Blocks
  - Four universal digital blocks (UDBs): customized digital functions for flexible designs
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - One Smart I/O supporting programmable digital logic in the I/O subsystem that works even in
depth sleep mode
- Packages
  - 25-pin WLCSP, 28-pin SSOP, 24-pin QFN
- I/O Subsystem
  - Up to 25 GPIOs

Collateral
Datasheet: PSoC 4200DS

Availability
Production: Now

Notes:
1 Embedded programmable digital logic in the I/O subsystem
**PSoC® 4A00**

**PSoC Analog Coprocessor**

### Applications

Industrial sensors (photoelectric sensors, displacement sensors), instrumentation and measurement (photometers, pH meters), and consumer products (wearables, grooming products)

### Features

- **Programmable Analog Blocks**
  - One universal analog block (UAB) configurable as a programmable analog filter, 14-bit Delta-Sigma ADC, or 13-bit voltage-output DAC (VDAC)
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), transimpedance amplifiers (TIA), etc.
  - One 12-bit/1-MspS SAR ADC
  - One 10-bit/11.6-kspS single-slope ADC
  - 38-channel analog multiplexer (AMUX)
  - One CapSense® block configurable as a capacitive-sensing controller, two 7-bit current-output DACs (IDACs), or two low-power CMPS
- **Signal Processing Engine**
  - 48-MHz Arm® Cortex®-M0+ with a DMA controller and watch crystal oscillator (WCO)
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Three serial communication blocks (SCBs) configurable as I²C, SPI, or UART
- **Packages**
  - 28-pin SSOP, 45-pin CSP, 48-pin QFN, 48-pin TQFP
- **I/O Subsystem**
  - Up to 38 GPIOs

### Collateral

**Datasheet:** [PSoC Analog Coprocessor](#)

---

1 A simple ADC used to measure slow-moving signals
**MCU Portfolio** – *WKA*

### PSoC® 4500S

**Applications**
Motor control and power factor correction (PFC) control in white goods
Industrial servo motor control

**Features**

- **MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - Two accelerator blocks for division and square-root computation
  - Up to 256KB flash and 32KB SRAM
  - External crystal oscillator with phase-locked loop (PLL)
- **Analog Blocks**
  - Two 12-bit SAR ADCs (1-Msps)
  - Three opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block
  - Two 7-bit current-output digital-to-analog converters (IDACs)
- **Digital Blocks and Communication Interfaces**
  - Eight timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs)
  - Segment LCD
- **Packages**
  - 48-TQFP, 64-TQFP (0.5-mm and 0.8-mm pitch)
- **I/O Subsystem**
  - Up to 53 GPIOs, including 16 Smart I/Os

**Collateral**

- Datasheet: [PSoC 4500S](https://www.cypress.com)

---

**Availability**

- **Production**: Now
**PSoC® 4100S Plus 256K**

**PSoC 4 MCU Base Line**

**Applications**
Main control and user interface for home appliance, consumer, and industrial applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - 256KB flash and 32KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - One CapSense® block
  - Two 7-bit current-output digital-to-analog converters (IDACs)

- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - Segment LCD

- **Packages**
  - 48-TQFP, 64-TQFP (0.5-mm and 0.8-mm pitch)

- **I/O Subsystem**
  - Up to 54 GPIOs, including 16 Smart I/Os

**Collateral**

Datasheet: [PSoC 4100S Plus 256K](#)

**Availability**

Production: Now

---

1 Embedded programmable digital logic in the I/O subsystem
**PSOC® 4100S Max**
**PSOC 4 MCU Base Line**

**Applications**
Main control and user interface for home appliance, consumer, and industrial applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with a DMA controller
  - 384KB flash and 32KB SRAM
  - External MHz oscillator (ECO) with PLL and 32-kHz watch crystal oscillator (WCO)
  - CRYPTO block including AES, TRNG, PRNG, CRC and SHA

- **Programmable Analog Blocks**
  - One 12-bit, 1-MspS SAR ADC
  - Two opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), etc.
  - Two low-power comparators
  - Two MSC (Multi-Sense Convertor) blocks for next-generation CapSense® technology

- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, or UART
  - Segment LCD
  - Two I2S Master channels

- **One CAN-FD (Controller Area Network with Flexible Data-rate) Controller**

- **Packages**
  - Up to 84 GPIOs, including 24 Smart I/Os

**Collateral**

Datasheet: [Contact Sales](#)

---

1 Embedded programmable digital logic in the I/O subsystem
**PSoC® 4100BLE**

**PSoC 4 MCU Base Line with BLE**

**Applications**

Sports and fitness monitors, wearable electronics, medical devices, home automation solutions, game controllers, and sensor-based low-power systems for the Internet of Things (IoT)

**Features**

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM

- **Programmable Analog Front Ends (AFEs)**
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Mmps SAR ADC

- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry's No. 1 capacitive-sensing solution with one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability

- **Programmable Digital Logic**
  - Four 16-bit configurable timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable I²C master or slave, SPI master or slave, or UART

- **Packages**
  - 56-pin QFN and 68-pin CSP

- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

**Datasheet:** PSoC 4100BLE

---

1 Bluetooth 4.2 is only available in the 256KB flash option device

**Availability**

Production: Now
PSOC® 4200BLE
PSOC 4 MCU Programmable Line with BLE

Applications
Sports and fitness monitors, wearable electronics, medical devices, home automation solutions, game controllers, and sensor-based low-power systems for the Internet of Things (IoT)

Features
- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU
  - Up to 256KB flash and 32KB SRAM
- **Programmable Analog Front Ends (AFEs)**
  - Four opamps, configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
- **CapSense® with SmartSense™ Auto-Tuning**
  - Industry's No. 1 capacitive-sensing solution including one Capacitive Sigma-Delta™ (CSD) controller with touchpad capability
- **Programmable Digital Logic**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Four configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Two serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 56-pin QFN and 68-pin CSP
- **Bluetooth Connectivity with Bluetooth 4.1 or Bluetooth 4.2**
  - Royalty-free stack and GUI-based Component to configure profiles, 2.4-GHz BLE radio with integrated balun

Datasheet: [PSOC 4200BLE](#)

1 Bluetooth 4.2 is only available in the 256KB flash option device

--

**Availability**
Production: Now
**PSoC® 4100M**

**PSoC 4 MCU Base Line**

**Applications**
User interface and host processor for home appliances, digital and analog sensor hubs, MCU and discrete analog replacement

**Features**

- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 128KB flash and 16KB SRAM

- **CapSense® with SmartSense™ Auto-Tuning**
  - Cypress Capacitive Sigma-Delta™ (CSD) controller
  - CapSense supported on up to 55 pins

- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)

- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as 16C master or slave, SPI master or slave, or UART

- **Packages**
  - 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN

**Collateral**

**Datasheet:** [PSoC 4100M](#)

---

**PSoC® 4 One-Chip Solution**

**MCU Subsystem**
- Arm Cortex®-M0
- 24 MHz
- Flash (64KB to 128KB)
- SRAM (8KB to 16KB)

**Programmable Analog Blocks**
- Opamp x4
- SAR ADC
- 8-bit IDAC x2
- 7-bit IDAC x2

**Programmable Digital Blocks**
- TCPWM x8
- SCB x4
- RTC
- DMA
- Segment LCD Drive

**I/O Subsystem**
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8

**Availability**

**Production:** Now

---

52 MCU PORTFOLIO – WKA
MCU PORTFOLIO – WKA

**PSoC® 4200M**

**PSoC 4 MCU Programmable Line**

### Applications

User interface and host processor for home appliances, digital and analog sensor hubs, LED control and communication for lighting systems

### Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 128KB flash and 16KB SRAM
- **CapSense® with SmartSense™ Auto-Tuning**
  - One Cypress capacitive Sigma-Delta™ (CSD) controller
  - CapSense supported on up to 55 pins
- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps, programmed as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)
- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Two Controller Area Network (CAN) Controllers**
- **Packages**
  - 48-pin LQFP, 64-pin TQFP (0.8-mm pitch), 64-pin TQFP (0.5-mm pitch), and 68-pin QFN

### Collateral

Datasheet: [PSoC 4200M](#)
**PSoc® 4200L**

**PSoc 4 MCU Programmable Line**

**Applications**

User interface and host processor for home appliances, digital and analog sensor hub, MCU and discrete analog replacement, and LED control and communication for lighting systems

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and RTC
  - Up to 256KB flash and 32KB SRAM
  - Up to 98 GPIOs supporting analog and digital interfaces

- **CapSense® With SmartSense™ Auto-Tuning**
  - Two Cypress Capacitive Sigma-Delta™ (CSD) controllers

- **Programmable Analog Blocks**
  - Two comparators (CMPs)
  - Four opamps configurable as programmable gain amplifiers (PGAs), comparators (CMPs), filters, etc.
  - One 12-bit/1-Msps SAR ADC
  - Four (2x 8-bit, 2x 7-bit) current-output DACs (IDACs)

- **Programmable Digital Blocks**
  - Eight universal digital blocks (UDBs): custom digital peripherals
  - Eight configurable 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I2C master or slave, SPI master or slave, or UART

- **Full-Speed USB 2.0 Controller and Transceiver**

- **Two Controller Area Network (CAN) Controllers**

- **Packages**
  - 48-pin TQFP, 64-pin TQFP, 68-pin QFN, and 124-pin VFBGA

**Collateral**

Datasheet: PSoC 4200L

**Available**

Production: Now
S6E1C-Series
FM0+ MCU Portfolio

Applications
- Industrial, healthcare, sensor hubs, wearable electronics, and mobile, battery-powered devices

Features
- **Ultra-Low-Power MCU Subsystem**
  - Up to 40-MHz Arm® Cortex®-M0+ CPU, 40-µA/MHz active current with 1.65–3.6-V operating voltage
  - Low-power 1.2-µA RTC operating current
  - Up to 128KB flash and 16KB SRAM
  - Near-zero wait-state flash access at up to 40 MHz
  - Fast 540-µs startup from power-on reset and 40 µs from standby

- **Analog and Digital Subsystems**
  - Two base timers, dual timer, CRC, and watch counter
  - Six channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, LIN, USB, and I²S
  - Two HDMI-CEC\(^1\) channels
  - Two Smart Card interface channels
  - 12-bit, 1-Msps ADC with a 24-channel multiplexer input

- **Packages**
  - 32-pin LQFP, 48-pin LQFP, 64-pin LQFP, 32-pin QFN, 48-pin QFN, 26-pin CSP (2.35-mm x 2.72-mm)

Collateral
- Datasheet: [S6E1C1-Series](#), [S6E1C3-Series](#)

Available at
- Production: Now

---

\(^1\) HDMI consumer electronics control signal
\(^2\) Low-voltage detect
\(^3\) Descriptor system transfer controller
\(^4\) Watchdog timer
S6E2C-Series
FM4 MCU Portfolio

Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

Applications

Features

- **High-Performance MCU Subsystem**
  - 675 CoreMark®, 200-MHz Arm® Cortex®-M4 CPU, 365-µA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low-power 1.0-µA RTC operating current
  - Up to 2MB flash and 256KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications

- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, four quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Sixteen channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
  - Two USB interfaces, two controller area network (CAN), CAN with flexible data rate (CAN-FD), IEEE 1588 Ethernet¹, high-speed Quad-SPI (HS-QSPI), I²S, and external bus interfaces
  - Three 12-bit/2-Mmps ADCs with a 32-channel multiplexer input
  - Two 12-bit DACs
  - Built-in Cryptographic Assist hardware coprocessor for encryption

- **Packages**
  - 144-pin LQFP, 176-pin LQFP, 216-pin LQFP, 192-pin BGA

Collateral

**Datasheet:** [S6E2CC-Series](#)

---

### MCU Subsystem

- **Cortex®-M4 200 MHz**
- **Flash** (1MB to 2MB)
- **SRAM** (128KB to 256KB)
- **MPU²**
- **LVD**
- **DMA**
- **DSTC³**
- **RTC**
- **Watch Counter**
- **WDT**
- **CRC**

### Digital Subsystem

- **MFT x3**
- **PPG x9**
- **Base Timer x16**
- **Dual Timer**
- **QPRC x4**
- **RTS**
- **CRC**
- **MDM**
- **External Bus Interface**
- **Crypto Assist**

### Analog Subsystem

- **12-bit ADC x3**
- **12-bit DAC x2**

### I/O Subsystem

- **GPIO x8**
- **GPIO x16**
- **GPIO x11**
- **GPIO x15**
- **GPIO x16**
- **GPIO x15**
- **GPIO x16**
- **GPIO x16**
- **GPIO x13**

---

1. Ethernet communications solution that supports the Precision Time Protocol (PTP) standard
2. Memory protection unit
3. Descriptor system transfer controller

---

**Availability**

**Production:** Now

---

**MCU PORTFOLIO – WKA**

56
**S6E2G-Series**

**FM4 MCU Portfolio**

**Applications**
Motor control, factory automation, industrial, Internet of Things (IoT), and building management systems and automation

**Features**

- **High-Performance MCU Subsystem**
  - 608 CoreMark®, 180-MHz Arm® Cortex®-M4 CPU, 244-μA/MHz active current with 2.7–5.5-V operating voltage
  - Up to 1MB flash and 192KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications

- **Analog and Digital Subsystems**
  - Two multifunction timers (MFTs), nine programmable pulse generators (PPGs), sixteen base timers, two quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Ten channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
  - Two USB interfaces, controller area network (CAN), IEEE 1588 Ethernet\(^1\), I²S, two SD Card interfaces, and an external bus interface
  - Three 12-bit/2-Msps ADCs with a 32-channel multiplexer input
  - Built-in Cryptographic Assist hardware coprocessor for encryption

- **Packages**
  - 144-pin LQFP and 176-pin LQFP

**Collateral**

- **Datasheet**: [S6E2G-Series](#)

---

1 Ethernet communications solution that supports the Precision Time Protocol (PTP) standard

2 Memory protection unit

3 Descriptor system transfer controller

---

**Availability**

**Production**: Now

---

**Datasheet**:

[S6E2G-Series](#)
**S6E2H-Series**

**FM4 MCU Portfolio**

**Applications**
Motor control, factory automation, industrial, IoT, DSLR lens MCU and home appliance

**Features**

- **High-Performance MCU Subsystem**
  - 540 CoreMark®, 160-MHz Arm® Cortex®-M4 CPU, 188-μA/MHz active current with 2.7–5.5-V operating voltage
  - Ultra-low power 1.3-μA RTC operating current
  - Up to 512KB flash and 64KB SRAM with 16KB flash accelerator
  - Error-correcting code (ECC) support, hardware watchdog timer (WDT), low-voltage detect (LVD), and clock supervisor blocks for safety-critical applications

- **Analog and Digital Subsystems**
  - Three multifunction timers (MFTs), nine programmable pulse generators (PPGs), eight base timers, three quadrature position/revolution counters (QPRCs), a dual timer, CRC, and watch counter
  - Eight channels of multifunction serial (MFS) interfaces configurable as SPI, UART, I²C, or LIN
  - Two controller area network (CAN), SD Card, and external bus interfaces
  - Three 12-bit/2-Msps ADCs with a 24-channel multiplexer input
  - Two 12-bit DACs

- **Packages**
  - 80-pin LQFP, 100-pin LQFP, 120-pin LQFP, 121-pin BGA

**Collateral**

- Datasheet: [S6E2H-Series](#)

**Availability**

- Production: Now

---

1. Memory protection unit
2. Descriptor system transfer controller
### MCU Development Kits

<table>
<thead>
<tr>
<th>Kit Number</th>
<th>Kit Name</th>
<th>Key Features</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8CKIT-049 or</td>
<td>PSoC Prototyping Kits</td>
<td>Ultra-low-cost prototyping, Breadboard-compatible, Serial wire debug (SWD) or</td>
<td>$4–$10</td>
</tr>
<tr>
<td>CY8CKIT-059</td>
<td></td>
<td>bootload for program/debug</td>
<td></td>
</tr>
<tr>
<td>CY8CKIT-042-BLE</td>
<td>Bluetooth Low Energy (BLE) Pioneer Development Kit</td>
<td>Arduino form factor compatible, Access to all PSoC 4 BLE I/Os, Full SWD program and debug</td>
<td>$49</td>
</tr>
<tr>
<td>CY8CPROTO-062-4343W</td>
<td>PSoC6 WiFi-BT Prototyping Kit</td>
<td>Low-cost prototyping kit, Breadboard-compatible, PSoC 6 Host MCU, CYW4343W Wi-Fi BT module</td>
<td>$30</td>
</tr>
<tr>
<td>CY8CKIT-062-WIFI-BT</td>
<td>PSoC6 WiFi-BT Pioneer Kit</td>
<td>Arduino form factor compatible, Full SWD program and debug</td>
<td>$99</td>
</tr>
<tr>
<td>CY8CKIT-062-BLE</td>
<td>PSoC 6 BLE Pioneer Kit</td>
<td>Arduino form factor compatible, Full SWD program and debug</td>
<td>$75</td>
</tr>
</tbody>
</table>

Learn more or buy a kit today at [www.cypress.com/kits](http://www.cypress.com/kits)
## MCU Packages

<table>
<thead>
<tr>
<th>Package</th>
<th>LOFP</th>
<th>PDIP</th>
<th>QFN</th>
<th>SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>48</td>
<td>8</td>
<td>20</td>
<td>28</td>
</tr>
<tr>
<td>PSoC 1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 5LP</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 6</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CapSense</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package</th>
<th>SSOP</th>
<th>TOFP</th>
<th>WLCSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>8</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>PSoC 1</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 5LP</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 6</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>CapSense</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package</th>
<th>WLCSP</th>
<th>Multi-Die WLCSP (M-WLCSP)</th>
<th>µBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>49</td>
<td>68</td>
<td>72</td>
</tr>
<tr>
<td>PSoC 1</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>PSoC 3</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>PSoC 4</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>PSoC 5LP</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>PSoC 6</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>CapSense</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>
### Additional MCU Packages

<table>
<thead>
<tr>
<th>Package</th>
<th>SSOP</th>
<th>TSSOP</th>
<th>SDIP</th>
<th>QFN</th>
<th>LQFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>8</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>48</td>
<td>64</td>
<td>32</td>
<td>48</td>
</tr>
<tr>
<td>8FX</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FM0+</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FM3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FM4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package</th>
<th>LQFP</th>
<th>QFP</th>
<th>TQFP</th>
<th>BGA</th>
<th>WLCSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>144</td>
<td>176</td>
</tr>
<tr>
<td></td>
<td>216</td>
<td>100</td>
<td>120</td>
<td>96</td>
<td>112</td>
</tr>
<tr>
<td></td>
<td>121</td>
<td>161</td>
<td>192</td>
<td>26</td>
<td>80</td>
</tr>
<tr>
<td>8FX</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FM0+</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FM3</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FM4</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

---

**Note:** The table above lists the additional MCU packages available, including their pin counts and compatibility with various package types such as SSOP, TSSOP, SDIP, QFN, LQFP, LQFP, QFP, TQFP, BGA, and WLCSP. The ✓ symbol indicates compatibility.
USB Portfolio
## USB Portfolio

### USB 3.1

<table>
<thead>
<tr>
<th>Device</th>
<th>Hub</th>
<th>Bridge</th>
<th>Storage</th>
<th>Type-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYUSB3011/2/3/4</td>
<td>CYUSB3xx</td>
<td>CYUSB306x</td>
<td>CYUSB303x</td>
<td>CYPD2xx</td>
</tr>
<tr>
<td>FX3</td>
<td>HX3</td>
<td>CX3</td>
<td>FX3S</td>
<td>CCG2</td>
</tr>
<tr>
<td>Peripheral Controller</td>
<td>32-Bit Bus to USB 3.1 Gen 1 ARM9, 512KB RAM</td>
<td>USB 3.1 Gen 1, Shared Link™, BC 1.2, Ghost Charge™</td>
<td>16-Bit Bus to USB 3.1 Gen 1 RAID³, Dual SDXC®/eMMC²</td>
<td>USB Type-C Cable Controller 1 PD Port, Termination, ESD</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>4</td>
<td>2</td>
<td>30V, PPS, QC4, 64KB Flash</td>
</tr>
<tr>
<td>CY7C6801x/53</td>
<td>CYUSB43xx</td>
<td>CYUSB361x</td>
<td>CYUSB302x</td>
<td>CYPD31xx</td>
</tr>
<tr>
<td>FX2LP</td>
<td>HX3PD</td>
<td>US5</td>
<td>SD3</td>
<td>CCG3</td>
</tr>
<tr>
<td>16-Bit Bus to USB 2.0</td>
<td>USB 3.1 Gen 2 Type-C Hub</td>
<td>USB 3.1 Gen 1 to GigaE Energy Efficient Ethernet</td>
<td>USB 3.1 Gen 1 to SD/SIO SDXC®/eMMC², RAID⁶</td>
<td>USB Type-C Port Controller 20V, Crypto, Billboard</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>1</td>
<td>1</td>
<td>PD Port, Termination, ESD</td>
</tr>
<tr>
<td>CYUSB201x</td>
<td>CY7C656x4</td>
<td>CYUSB202x</td>
<td>CYUSB202x</td>
<td>CYPD32xx</td>
</tr>
<tr>
<td>FX2G2</td>
<td>HX2VL</td>
<td>SD2</td>
<td>SD2</td>
<td>CCG4</td>
</tr>
<tr>
<td>32-Bit Bus to USB 2.0</td>
<td>4 Ports</td>
<td>USB 2.0 HS to SD/SIO SDXC®/eMMC², RAID⁶</td>
<td>Contact Sales</td>
<td>USB Type-C Port Controller 2 PD Ports, 128KB Flash, TBT</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>1</td>
<td>1</td>
<td>PD Port, Termination, ESD</td>
</tr>
</tbody>
</table>

### USB 2.0

<table>
<thead>
<tr>
<th>Device</th>
<th>Hub</th>
<th>Bridge</th>
<th>Storage</th>
<th>Type-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY7C656x1</td>
<td>CY7C656x4</td>
<td>CY7C6521x</td>
<td>CYUSB202x</td>
<td>CYPD31xx</td>
</tr>
<tr>
<td>HX2L</td>
<td>HX2VL</td>
<td>USB Serial</td>
<td>SD2</td>
<td>CCG4</td>
</tr>
<tr>
<td>4 Ports</td>
<td>4 Ports</td>
<td>UART/SPI/PC to USB 2 Channels, CapSense⁴</td>
<td>Contact Sales</td>
<td>USB Type-C Port Controller 2 PD Ports, 128KB Flash, TBT</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>1</td>
<td>1</td>
<td>PD Port, Termination, ESD</td>
</tr>
<tr>
<td>CYUSB24xx</td>
<td>CY7C656x1</td>
<td>CYUSB202x</td>
<td>CYUSB202x</td>
<td>CYPD31xx</td>
</tr>
<tr>
<td>eRT2</td>
<td>eUSB2 Repeater</td>
<td>SD2</td>
<td>SD2</td>
<td>CCG4</td>
</tr>
<tr>
<td>Contact Sales</td>
<td>Contact Sales</td>
<td>Contact Sales</td>
<td>Contact Sales</td>
<td>PD Port, Termination, ESD</td>
</tr>
</tbody>
</table>

### USB 1.1

<table>
<thead>
<tr>
<th>Device</th>
<th>Hub</th>
<th>Bridge</th>
<th>Storage</th>
<th>Type-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY7C638xx</td>
<td>CY7C652x1</td>
<td>CY7C6521x</td>
<td>CYUSB202x</td>
<td>CYPD31xx</td>
</tr>
<tr>
<td>64215/6423</td>
<td>USB-to-UART (Gen 2)</td>
<td>USB Serial</td>
<td>SD2</td>
<td>CCG4</td>
</tr>
<tr>
<td>1 or 2 UART/SPI/PC channels</td>
<td>3 Mbps, 8 GPIOs</td>
<td>UART/SPI/PC to USB 2 Channels, CapSense⁴</td>
<td>Contact Sales</td>
<td>USB Type-C Port Controller 2 PD Ports, 128KB Flash, TBT</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>1</td>
<td>1</td>
<td>PD Port, Termination, ESD</td>
</tr>
</tbody>
</table>

### USB 1.0

<table>
<thead>
<tr>
<th>Device</th>
<th>Hub</th>
<th>Bridge</th>
<th>Storage</th>
<th>Type-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY7C6521</td>
<td>CY7C6521</td>
<td>CY7C6521</td>
<td>CYUSB202x</td>
<td>CYPD31xx</td>
</tr>
<tr>
<td>7</td>
<td>USB-to-UART (Gen 2)</td>
<td>USB Serial</td>
<td>SD2</td>
<td>CCG4</td>
</tr>
<tr>
<td>3 Mbps, 8 GPIOs</td>
<td>UART/SPI/PC to USB 2 Channels, CapSense⁴</td>
<td>Contact Sales</td>
<td>Contact Sales</td>
<td>PD Port, Termination, ESD</td>
</tr>
<tr>
<td>NEW</td>
<td>Q202</td>
<td>1</td>
<td>1</td>
<td>PD Port, Termination, ESD</td>
</tr>
</tbody>
</table>

### Type-C Products

- **NEW**: Indicates new products.
- **Q202**: Indicates availability for Q2 2022.
- **Q420**: Indicates availability for Q4 2022.
- **Contact Sales**: Indicates contact sales for further information.

**Notes:**
- **1**: Simultaneous USB 2.0 and SuperSpeed traffic on the same port
- **2**: Battery Charging specification v1.2
- **3**: Enables USB charging without host connection
- **4**: Camera Serial Interface v2.0
- **5**: Redundant array of independent disks
- **6**: SD extended capacity
- **7**: Embedded Multimedia Card

### Type-C Products

- **NEW**: Indicates new products.
- **Q202**: Indicates availability for Q2 2022.
- **Q420**: Indicates availability for Q4 2022.
- **Contact Sales**: Indicates contact sales for further information.

**Notes:**
- **1**: Simultaneous USB 2.0 and SuperSpeed traffic on the same port
- **2**: Battery Charging specification v1.2
- **3**: Enables USB charging without host connection
- **4**: Camera Serial Interface v2.0
- **5**: Redundant array of independent disks
- **6**: SD extended capacity
- **7**: Embedded Multimedia Card

### Status Availability

- **Development**: Indicates products in development.
- **Sampling**: Indicates products in sampling.
- **Production**: Indicates products in production.

---

**Cypress Roadmap: USB**
<table>
<thead>
<tr>
<th>Timeline</th>
<th>Power</th>
<th>Cable</th>
<th>PC Host</th>
<th>Devices, Dock &amp; Monitors</th>
<th>Automotive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Source</td>
<td>Sink</td>
<td>Active / Passive</td>
<td>Single port</td>
<td>Dual Port</td>
</tr>
<tr>
<td>Production</td>
<td>CYPD3xxx CCG3 USB Type-C Port Controller 20-V, Crypto, Billboard</td>
<td>CYPD3xxx CCG3 USB Type-C Port Controller 20-V, Crypto, Billboard</td>
<td>CYPD2xxx CCG2 USB-C Active Cable Controller 1 PD Port, Termination, ESD</td>
<td>CYPD1xxx CCG1 USB Type-C Port Controller 1 PD Port, 5 Profiles, 100 W</td>
<td>CYUSB333x HX3C 4 Ports: 1 Type-C, 3 Type-A USB PD, Billboard, BC1.2</td>
</tr>
<tr>
<td></td>
<td>CYPD317x/CCPD118x USB Type-C Port Controller 30V, PPS, QC4, 64/128KB Flash</td>
<td>CYPD317x CCG3PA USB Type-C Port Controller 30V, PPS, QC4, 64/128KB Flash</td>
<td>CYPD27xx CCG1 USB-C EMCA Passive Ctrlr PD 3.0, Vbus short protection</td>
<td>CYPD5xxx CCG5 USB Type-C Port Controller 2 PD Ports, Vbus short protection</td>
<td>CYPD319x CCG3PA USB Type-C Port Controller 30V, PPS, QC4, 64KB Flash</td>
</tr>
<tr>
<td></td>
<td>CYPAS1xx PAG1S Secondary-side Controller 1 PD Port, SR, PWM, PPS</td>
<td>CYPD3177 BCR USB Type-C UFP Controller PD 3.0, 5 PDOs, power sink</td>
<td>CYPD612x CCG6 USB Type-C Port Controller 1 PD Port, Load S/W, UCSI</td>
<td>CYPD562x CCG6D USB Type-C Port Controller 2 PD Ports, Load S/W FET, TBT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CYPAP11xx PAG1P Primary-side Start-up Controller 90 – 264V</td>
<td></td>
<td>CYAC11xx AC61F USB Type-C only Port Controller 1 Type-C port, Load S/W, UCSI</td>
<td>CY7C85210/7 USB Billboard ARM Cortex M0 1 or 2 UART/SPI/PCI channels</td>
<td></td>
</tr>
<tr>
<td>Q2’20</td>
<td>CYPD72xx CCG7D USB Type-C Port Controller 2 PD Ports, DC–DC Buck Boost</td>
<td></td>
<td>CYPD612x CCG6SF USB Type-C Port Controller 1 PD Port, Load S/W FET, TBT</td>
<td>CYUSB43xx HX3P USB 3.1 Gen 2 Type-C Hub 7 Ports, PD, Billboard, 10 Gbps</td>
<td></td>
</tr>
<tr>
<td>Q3’20</td>
<td></td>
<td></td>
<td></td>
<td>CYD72xx CCG7D USB Type-C Port Controller 2 PD Ports, DC–DC Buck Boost</td>
<td></td>
</tr>
<tr>
<td>&gt;Q3’20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Status**: Development
**Availability**: Q2’20

NEW

Cypress Roadmap: USB
**EZ-PD ACG1F**

Single Port Type-C controller with BC1.2, Load Switch

### Features
- **Type-C 1.2 Controller**
- $V_{BUS}$ to CC/SBU short protection
- **Integrated Analog Blocks**
  - Configurable $V_{BUS}$ over-voltage protection and over-current protection
  - High-side current sense$^3$ amplifier across 5mohms
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
  - VCONN FET per CC with VCONN OCP limit of up to 550 mA
- **Integrated Digital Blocks**
  - 4x GPIOs
  - One SCB$^1$ for configurable master/slave I2C, SPI, or UART
  - Arm® Cortex®-M0 with MCU Subsystem and 16KB flash
- **Power System**
  - Integrated 15-W provider load switch capable of 5 V, 3A
  - $V_{BUS}$ over-voltage protection and Reverse Current Protection on provider path
- **Packages**
  - 24-QFN (4x4 mm)

### Collateral
- Datasheet: [ACG1F Datasheet](#)
PAG1S
USB-C Power Delivery Secondary-Side Controller

Applications
USB PD chargers, power adapters

Features
- PPS/PD3.0/QC4.0 integrated flyback controller for mobile chargers
- Works with both primary side-controlled and secondary-side-controlled flyback designs
- Integrated secondary-side regulation, synchronous rectifier, and charging port controller offering a single-chip secondary-side controller
- Supports Quasi-Resonant (QR)/Critical Conduction (CrCM), valley switching, discontinuous conduction (DCM), and Burst Modes
- Integrated digital blocks
  - One timer/counter/pulse-width modulator (TCPWM) block, 6x GPIOs
- Integrated analog blocks
  - Configurable VBUS overvoltage protection (OVP), overcurrent (OCP) protection, undervoltage protection (UVP), and short-circuit protection (SCP)
  - Integrated 2xVBUS discharge FETs and a NFET gate driver to drive the load switch
  - Low-side current sense\(^1\) capable of detecting 100-mA change
  - One legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^2\))
- Low-Power Operation
  - High-voltage (3–30 V, 30-V maximum) VBUS voltage inputs
  - No load power consumption of less than 20 mW
- Package
  - 24 QFN (16 mm\(^2\))

Collateral
Preliminary Datasheet: [PAG1S Datasheet]

\(^1\) Circuit to measure the current flowing on the VBUS
\(^2\) Adaptive Fast Charging
\(^3\) Termination resistors: R\(_P\) read as a DFP, R\(_D\) as a UFP

Availability
Production: Now

PAG1S: USB Type-C PD Secondary Controller

System Resource
- 1x TCPWM

Integrated Digital Blocks
- System Resource
- 1x TCPWM

USB PD Subsystem
- Low side Sync Rectifier Driver
- Primary PWM Driver
- Baseband MAC PHY
- V\(_{\text{bus}}\)-to-CC Short Protection
- 30-V–Tolerant Regulator
- 1x NFET Gate Driver
- OCP and OVP
- Low-Side Current Sense
- 1x Charge-Detect (BC 1.2, AC, QC4.0, AFC)
- Integrated Resistors (R\(_P\), R\(_D\))\(^3\)
- Feedback Control Circuitry for Voltage (V\(_{\text{bus}}\)) Regulation
- 1x 8-bit SAR ADC

I/O Subsystem
- Programmable I/O Matrix
- CC
- 6x GPIO Ports

MCU Subsystem
- Logic Controller
- Advanced High-Performance Bus (AHB)

Logic Controller
- System Resource
- 1x TCPWM

USB PD Subsystem
- Low side Sync Rectifier Driver
- Primary PWM Driver
- Baseband MAC PHY
- V\(_{\text{bus}}\)-to-CC Short Protection
- 30-V–Tolerant Regulator
- 1x NFET Gate Driver
- OCP and OVP
- Low-Side Current Sense
- 1x Charge-Detect (BC 1.2, AC, QC4.0, AFC)
- Integrated Resistors (R\(_P\), R\(_D\))\(^3\)
- Feedback Control Circuitry for Voltage (V\(_{\text{bus}}\)) Regulation
- 1x 8-bit SAR ADC

I/O Subsystem
- Programmable I/O Matrix
- CC
- 6x GPIO Ports

MCU Subsystem
- Logic Controller
- Advanced High-Performance Bus (AHB)
PAG1P
USB-C Power Delivery Primary Start Up Controller

Applications
USB PD chargers, power adapters

Features
- Works across universal AC mains input 85 VAC to 265 VAC
- Operates with PWM inputs from a secondary-side controller
- Low-side gate driver to drive primary FET (1-A Source)
- Soft-start with duty-cycle clamping
- Integrates high-voltage start-up and shunt regulator
- Line undervoltage and overvoltage protection
- Overcurrent protection against load short-circuit
- Operates over a temperature range of -40 ºC to 105 ºC
- Package – 10-pin SOIC (4.9 x 3.9 mm²)

Collateral
Preliminary Datasheet: PAG1S Datasheet

Availability
Production: Now
EZ-USB HX3PD
USB 3.1 Gen 2 Type-C Hub with Power Delivery

Applications
Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

Features
- USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD
  - Upstream (US) ports:
    - 10 Gbps; Type-A or Type-C plus PD (UFP)
  - Downstream (DS) ports:
    - 7 ports: 5x 10 Gbps, 2x 480 Mbps
    - 3 Type-C ports: 1 PD port (DFP), 2 Type-C only
- Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction
  - Integrated termination resistors ($R_P$ and $R_D$)\(^1\)
  - Integrated USB Billboard Controller\(^2\), USB Type-C Bridge Controller
  - Integrated V\(_{CONN}\) FETs and ADC for overvoltage and overcurrent protection
- Charging Support
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- Ghost Charge™: Charging DS without US connection
- Dock Management Controller for secured firmware download
  - Firmware upgradable over USB
- System-Level ESD on Configuration Channel (CC) Pins: 8 kV Contact, 15 kV Air
- Package: 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

Collateral
Datasheet: HX3PD Datasheet
Kit: HX3PD Evaluation Kit

Availability
Samples: Now  Production: Q3 2020

\(^1\) Termination resistors: $R_P$ read as a DFP, $R_D$ as a UFP
\(^2\) A USB Device controller that is used to implement the USB Billboard Device Class
\(^3\) Transaction Translator

Informs the USB Host of the supported Alternate Modes as well as any failures
**EZ-PD BCR**

**USB Type-C Power-Sink Port Controller**

### Applications

- **Portable electronics** – cameras, camcorders, smart speakers, toys, gaming, shavers, powered tools and any battery-powered devices.
- **Industrial** – LED lighting, scanner, printer, drones, IoT

Any electronics device consuming less than 100W

### Features

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power the BCR controller
  - One serial communication blocks (SCB) for slave I²C

- **Integrated Analog**
  - \( V_{BUS} \) overvoltage (OVP) and undervoltage (UVP) protection
  - Fault detection for PDO mismatch
  - Slew rate-controlled PMOS FET gate driver
  - Minimum 25-V–tolerant CC pins and FET control pins

- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) \( V_{BUS} \) voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC

- **System-Level ESD on CC, and \( V_{BUS} \)**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C

- **Package**
  - 24-QFN (16 mm²), supporting extended Industrial temp (-40 °C to 105 °C)

### Collateral

- **Datasheet:** CY3177 Datasheet
- **Evaluation Kit:** CY4533 Kit
- **Product Brochure:** [EZ-PD Barrel Connector Replacement Product Overview](https://www.cypress.com)

---

1 Analog feedback voltage control circuit to control \( V_{BUS} \)
2 Circuit to measure the current flowing on the \( V_{BUS} \)
3 Termination resistors: \( R_D \) as a UFP, \( R_D\_DB \) as a UFP supporting dead battery

### EZ-PD BCR: USB Type-C Power-Sink Port Controller

#### I/O Subsystem

<table>
<thead>
<tr>
<th>CC</th>
<th>1x SCB (I²C)</th>
<th>Fault Detection</th>
</tr>
</thead>
</table>

#### USB PD Subsystem

<table>
<thead>
<tr>
<th>Baseband MAC</th>
<th>Baseband PHY</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>30-V Regulator</th>
<th>Integrated Resisters ((R_D, R_D_DB))</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>OVP and UVP</th>
<th>1x 9-bit SAR ADC</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>VBus-CC Short Protection</th>
<th>VBus Discharge</th>
</tr>
</thead>
</table>

### Availability

**Production:** Now
EZ-PD CCG6
Single-Port USB Type-C Port Controller With PD

Applications
Thunderbolt / USB-C Notebook, Desktop PCs

Features
- USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode and USB platforms
- \( V_{BUS} \) to CC/SBU short protection
- Integrated high-voltage 20V-regulator to power CCG6
- Integrated Analog Blocks
  2x1 SBU analog mux, 2x2 USB analog mux
  Configurable \( V_{BUS} \) over-voltage protection and over-current protection
  High-side current sense amplifier across 5 mΩ
  Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- Integrated Digital Blocks
  Two timers, counters, and pulse-width modulators, 17x GPIOs
  Four SCBs for configurable master/slave I2C, SPI, or UART
- Arm® Cortex®-M0 with MCU Subsystem and 128KB flash
- Power System
  High-voltage (4 - 21.5 V, 26 V Max) \( V_{BUS} \) voltage inputs
  2x \( V_{CONN} \) FETs supporting up to 500 mA, Supports Dead Battery mode operation
  Integrated PFET gate drivers and Slew Rate Control
  \( V_{BUS} \) over-voltage protection and Reverse Current Protection on provider path
- Packages
  40 QFN (6x6 mm)

Collateral
Datasheet: CCG6 Datasheet

Availability
Production: Now

Note: Serial communication block configurable as UART, SPI or I2C
Cypress Roadmap: USB

**EZ-PD CCG6F**

Single-Port USB Type-C Port Controller With PD

**Features**

- USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode, and USB platforms
- $V_{BUS}$ to CC/SBU short protection
- Integrated high-voltage 20V-regulator to power CCG6
- Integrated Analog Blocks
  - 2x1 SBU analog mux, 2x2 USB analog mux
  - Configurable $V_{BUS}$ over-voltage protection and over-current protection
  - High-side current sense amplifier across 5 mΩ
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- Integrated Digital Blocks
  - Two timers, counters, and pulse-width modulators, 17x GPIOs
  - Four SCBs\(^1\) for configurable master/slave I2C, SPI, or UART
- Arm® Cortex®-M0 with MCU Subsystem and 128KB flash
- Power System
  - High-voltage (4 - 21.5 V, 26 V Max) $V_{BUS}$ voltage inputs
  - 2x $V_{CONN}$ FETs supporting up to 500 mA, Supports Dead Battery mode operation
  - Integrated PFETs for provider path
  - $V_{BUS}$ over-voltage protection and Reverse Current Protection on provider path
- Packages
  - 96 BGA (6x6 mm)

**Collateral**

Datasheet: [CCG6F Datasheet](#)

\(^1\) Serial communication block configurable as UART, SPI or I2C

**Applications**

Thunderbolt / USB-C Notebook, Desktop PCs

**Availiability**

Production: Now
**EZ-PD CMG1**

USB Type-C Passive EMCA Controller

### Applications
- USB-C EMCA

### Features
- USB-C PD Controller, PD 3.0 Transceiver
- $V_{BUS}$-to-CC Short Protection
- $V_{BUS}$-to-$V_{CONN}$ Short Protection
- Power from $V_{CONN}$ range 3.0 to 5.5-V
- Termination Resistor $R_A$
- Supports $R_A$ Weakening to Reduce Power Consumption
- Configurable 32-byte Storage for Configuration Over Type-C Interface
- Integrated oscillator eliminating the need for external clock
- Power Operation
  - 2.7-V to 5.5-V operation ($V_{CONN}$ pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, $V_{CONN}$ Pins
  - ±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm²)
  - Supports industrial temperature range (-40°C to +85°C)

### Collateral
- Preliminary Datasheet: [CMG1 Datasheet](#)

### Availability
- Production: Now

### CMG1: USB Type-C Passive EMCA Controller

![CMG1 Diagram]

- **USB PD Subsystem**
  - $V_{BUS}$-to-CC Short Protection
  - $V_{BUS}$-to-$V_{CONN}$ Short Protection
  - $V_{BUS}$-to-$V_{CONN}$ Short Protection, $R_A$

- **Storage**
  - 32-Byte Storage for Configuration

- **System Resources**
  - Oscillator
  - Reset
  - $V_{REF}$
  - $I_{REF}$

- **EMCA Protocol Engine**
- **USB PD & Type-C PHY**
**EZ-PD CCG3PA2**

**USB Type-C and PD Port Controller**

### Applications
- Power adapters, chargers, power banks

### Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable VBUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for VBUS control
  - Low side current sense² capable of detecting 100-mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)
- **32-bit Arm® Cortex®-M0 CPU with 128KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) VBUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / VCONN, VBUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm²), 30-ball CSP (7.5 mm²)

### Collateral
- Datasheet: [Contact Sales](#)

1. Analog feedback voltage control circuit to control VBUS
2. Circuit to measure the current flowing on the VBUS
3. Adaptive Fast Charging
4. Termination resistors: R₁ as a DFP, R₂ as a UFP, R₃ as an EMCA

### Availability
- **Production:** Now

---

**CCG3PA2: USB Type-C Port Controller with PD**

#### MCU Subsystem
- Arm Cortex-M0
- 48 MHz

#### Integrated Digital Blocks
- 4x TCPWM
- 2x SCB (I²C, SPI, UART)

#### I/O Subsystem
- Programmable I/O Matrix
- 14x GPIO Ports

#### USB PD Subsystem
- Baseband MAC
- 2x VCONN FETs
- OCP and OVP
- Low-Side Current Sense
- 2x Charge-Detect (BC v1.2, AC, QC, AFC)
- Integrated Resistors (R₁, R₂)
- Error Amplifier
- 1x 9-bit SAR ADC

---

1. Analog feedback voltage control circuit to control VBUS
2. Circuit to measure the current flowing on the VBUS
3. Adaptive Fast Charging
4. Termination resistors: R₁ as a DFP, R₂ as a UFP, R₃ as an EMCA
EZ-PD CCG3PA
USB Type-C and PD Port Controller

Applications
- Power adapters, mobile chargers, car chargers, power banks, and power sinks

Features
- USB-C PD Controller, PD 3.0 Transceiver and Qualcomm QC 4.0
- \( V_{BUS} \) to-CC Short Protection
- Integrated High-Voltage 30-V Tolerant LDO to Power CCG3PA
- Integrated Digital Blocks
  - Four timer/counter/pulse-width modulator (TCPWM) blocks, 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I\(^2\)C, SPI, or UART
- Integrated Analog Blocks
  - Configurable \( V_{BUS} \) overvoltage protection (OVP) and overcurrent protection (OCP)
  - Integrated voltage regulation\(^1\) with analog output and PFET gate drivers
  - Low-side current sense\(^2\) capable of detecting 100-mA change
  - Two legacy charge-detect blocks (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^3\))
- Arm\(^\circledast\) Cortex\(^\circledast\)-M0 with MCU Subsystem and 64KB Flash
- Low-Power Operation
  - High-voltage (3-30 V, 30-V maximum) \( V_{BUS} \) Voltage inputs
  - Sleep: 3 mA; Deep Sleep: 30 \( \mu \)A with wake-on-CC
- System-Level ESD on CC, Dp / Dn\(^4\) and \( V_{BUS} \) Pins
  - \( \pm 8 \)-kV contact, \( \pm 15 \)-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 24 QFN (16 mm\(^2\)), 16-SOIC (60 mm\(^2\))

Collateral
- Datasheet: [CCG3PA Datasheet](#)

Availability
- Production: Now

---
\(^1\) Analog feedback control circuit to regulate \( V_{BUS} \)
\(^2\) Adaptive Fast Charging
\(^3\) Circuit to measure the current flowing on the \( V_{BUS} \)
\(^4\) USB-C bus wires used to transmit and receive USB 2.0 data
\(^5\) Termination resistors: \( R_p \) read as a DFP, \( R_c \) as a UFP
**EZ-PD CCG5**
Dual-Port USB Type-C and PD Port Controller

### Applications
- Notebooks, docks, Thunderbolt devices

### Features
- **Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports**
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI¹-compliant Interface with WHQL²-certified driver
  - Support for UEFI³ driver with Microsoft capsule firmware download
- **Integrated Analog**
  - Integrated high-voltage LDO and 4x \( V_{\text{CONN}} \) FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC⁴)
  - Integrated Type-C termination resistors (\( R_p, R_o, R_{DB} \))
  - 25-V tolerance on CC1/2 and SBU pins
- **Arm® Cortex®-M0 CPU with 128KB Flash and 12KB SRAM**
  - 4x serial communication blocks (SCB) - I²C, SPI or UART
  - Firmware upgradeable over SWD/I²C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2µs response time; Integrated \( V_{\text{BUS}}/V_{\text{CONN}} \) overcurrent protection (OCP)
- **System-Level ESD on CC/\( V_{\text{CONN}} \), \( V_{\text{BUS}} \), and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Discharge IEC61000-4-2 Level 4C
- **Packages**
  - 2-Port in 96-BGA (6 mm²), 1-Port in 40-QFN (6 mm²)

### Collateral
- **Datasheet:** [CCG5 Datasheet](#)

---

**CCG5: USB Type-C Port Controller with PD**

**MCU Subsystem**
- Arm Cortex-M0 48 MHz
- Flash (128KB)
- SRAM (12KB)

**Integrated Digital Blocks**
- 2x TCPWM
- SCB (I²C, SPI, UART)
- SCB (I²C, SPI, UART)

**I/O Subsystem**
- Programmable I/O Matrix: CC
- V_{\text{CONN}}
- 4x GPIO Port

**USB PD Subsystem x2**
- Baseband MAC
- Baseband PHY
- 2x2 USB Analog Switch
- 2x USB Charge Detect (BC v1.2, Apple Charging)

**System Resources**
- 2x SBU Analog Pass through / Mux
- 2x V_{\text{CONN}} FETs
- 4x 8-bit SAR ADC
- \( V_{\text{BUS}} \) OVP

**HV Protection**
- On CC, SBU
- V_{\text{CONN}} OCP

---

¹ USB Type-C Connector System Software Interface  
² Unified Extensible Firmware Interface  
³ Termination resistors: \( R_p \) read as a DFP, \( R_o \) as a UFP, \( R_{DB} \) as UFP in Dead-Battery scenario  
⁴ Adaptive Fast Charging

---

**Availability**
- **Production:** Now
EZ-PD CCG4/4M
Dual-Port USB Type-C and PD Port Controller

**Applications**
Notebooks, tablets, monitors, docking stations

**Features**
- Integrated USB Type-C Transceivers Support Two Type-C Ports
  - Integrated 2x 1-W VCONN FETs and 2x FET control signals, per port programmable R_P¹ and removable R_P and R_D² terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- Increased Flash Enables Fail-Safe Bootup
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- Integrated Digital Blocks for Inter-Chip Communications
  - Four serial communication blocks (SCBs) master or slave configurable to I²C, SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- Low-Power Operation
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA
  - Deep Sleep: 2.5 μA with wake-on-I²C or wake-on-configuration channel (CC)
- System-Level ESD on CC Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- 32-bit Arm® Cortex®-M0 CPU with MCU Subsystem
  - 128KB Flash, upgradable over CC lines or I²C interface
- Packages
  - 40-pin QFN, 96-ball BGA (CCG4M)

**Collateral**
Datasheet: [CCG4 Datasheet](#)

**Availability**
Production: Now

1 Termination resistor read as a DFP
2 Termination resistor read as a UFP
EZ-PD CCG3
USB Type-C and PD Port Controller

Applications
Accessories and power adapters

Features
- One Type-C Port with Integrated Transceiver
  - Alternate Modes\(^1\), Crypto Engine\(^2\) for USB Authentication\(^3\)
- Power Delivery (PD) Support for Standard Power Profiles
- Integrated Digital Blocks for V\(_{BUS}\) Power and MUX Interface
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave I\(^2\)C, SPI or UART
  - USB Billboard Controller\(^4\) with Billboard Device Class\(^5\) support
- Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - 21.5-V OVP and OCP; 2:2 cross-bar switch
- 32-bit Arm\(^\circledR\) Cortex\(^\circledR\)-M0 CPU with MCU Subsystem
  - 2x64KB Flash for fail-safe updates over CC, I\(^2\)C or USB interfaces
- Low-Power Operation
  - 2x V\(_{BUS}\) Gate Drivers\(^6\), for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) V\(_{BUS}\) voltage inputs
  - Sleep: 2.0 mA; Deep Sleep: 2.5 μA with wake-on-I\(^2\)C or wake-on-CC
- System-Level ESD on CC/V\(_{CONN}\), V\(_{BUS}\), and SBU Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- Packages
  - 42-ball (8.38 mm\(^2\)) CSP, 40-pin (36 mm\(^2\)) QFN and 32-pin (25 mm\(^2\)) QFN

Collateral
Datasheet: CCG3 Datasheet

Availability
Production: Now

CCG3: USB Type-C Port Controller with PD

- MCU Subsystem
  - Cortex-M0
  - 48 MHz
  - 4x TCPWM
  - 4x SCB (I\(^2\)C, SPI, UART)
- I/O Subsystem
  - Programmable I/O Matrix
  - CC
- USB PD Subsystem
  - Baseband MAC
  - Baseband PHY
  - 21.5-V Regulator
  - 2x V\(_{CONN}\) FETs
  - OCP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers
  - OVP
  - Integrated Resistors (R\(_P\), R\(_D\), R\(_A\))\(^6\)
  - 2x 6-bit SAR ADC

- System Resources
  - Full-Speed USB Billboard Controller
  - Advanced High-Performance Bus (AHB)
  - SRAM (8KB)
  - Flash (64KB)

- Advanced Digital Blocks
  - Crypto Engine
  - Flash (64KB)
  - SRAM (8KB)

- System Resources
  - 2x V\(_{CONN}\) FETs
  - OCP
  - OVP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers
  - 2x 6-bit SAR ADC

- Enhanced Security
  - Crypto Engine
  - OCP
  - OVP

- Enhanced Power Management
  - 2x V\(_{CONN}\) FETs
  - OCP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers

- Enhanced Interface Capabilities
  - 2x V\(_{CONN}\) FETs
  - OCP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers

- Enhanced Security
  - Crypto Engine
  - OCP
  - OVP

- Enhanced Power Management
  - 2x V\(_{CONN}\) FETs
  - OCP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers

- Enhanced Interface Capabilities
  - 2x V\(_{CONN}\) FETs
  - OCP
  - 2x 20V V\(_{BUS}\) FET Gate Drivers

1 Mode of operation in which the data lines are repurposed to transmit non-USB data
2 The encryption hardware and software required to implement USB Authentication
3 A USB-I/F specification that defines the authentication protocol for Type-C accessories
4 A USB Device controller that informs the USB Host of the supported Alternate Modes
5 A specification that defines the method for a USB Device to communicate the supported Alternate Modes
6 Circuits to control the gates of external power Field-Effect Transistors (FETs) on V\(_{BUS}\) (5-20 V)
7 Termination resistors: R\(_P\) read as a DFP, R\(_D\) as a UFP, R\(_A\) as an EMCA
EZ-PD CCG2
USB Type-C and PD Port Controller

Applications
USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

Features

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with 32KB Flash and 4KB SRAM
- **Integrated Digital Blocks**
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs¹ configurable to I²C, SPI or UART modes
- **Type-C Support**
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (R_P, R_D, R_A)²
- **Power Delivery (PD) Support**
  - Standard power profiles
- **Low-Power Operation**
  - Two independent V_CONN fails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation; Sleep: 2.0 mA; Deep Sleep: 2.5 µA
- **System-Level ESD on CC and VDD Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 20-ball CSP (3.3 mm²) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm²) with 0.55-mm pin pitch

Collateral

- **Datasheet:** CCG2 Datasheet
- **Reference Design Kit:** CCG2 RDK
- **Evaluation Kit:** CCG3 EVK

CCG2: USB Type-C Port Controller With PD

**MCU Subsystem**
- arm® Cortex-M0
- 48 MHz

**Integrated Digital Blocks**
- TCPWM
- SCB (I²C, SPI, UART)
- Profiles and Configurations
- Baseband MAC
- Baseband PHY
- Integrated R_P, R_D, R_A

**I/O Subsystem**
- CC
- VCONN1
- VCONN2
- VDDIO
- GPIO
- Port

**Availability**

- **Production:** Now

---

¹ Serial communication block configurable as UART, SPI or I²C
² Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA
EZ-USB FX3
USB 3.1 Gen 1 Peripheral Controller

Applications
Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras, document and fingerprint scanners, videoconferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz Arm® 926EJ Core
  - 512KB of embedded SRAM for code space and buffers
- 32-bit, 100-MHz, flexible GPIF II Interface
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
Datasheet: FX3 Datasheet
Development Kit: FX3 SuperSpeed Explorer Kit
Software Development Kit: EZ-USB FX3 SDK

Availability
Production: Now
EZ-USB FX3S
USB 3.1 Gen 1 RAID\(^1\)-on-Chip

**Applications**
- Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders, and data logging devices

**Features**
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz Arm\(^\circledR\) 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I\(^2\)C, I\(^2\)S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
- **Two SDXC\(^2\), eMMC\(^3\) 4.4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations
- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Packages**
  - 121-ball BGA (10 mm\(^2\)), 131-ball WLCSP (4.7 x 5.1 mm)

**Collateral**
- Datasheet: [FX3S Datasheet](#)
- Kit: [FX3S RAID\(^1\)-on-Chip Boot Disk Kit](#)
- Software Development Kit: [EZ-USB FX3 SDK](#)

**Availability**
- Production: Now

---

\(^1\) Redundant array of independent disks
\(^2\) SD extended capacity
\(^3\) Embedded Multimedia Card
EZ-USB CX3
MIPI® CSI-2 to USB 3.1 Gen 1 Bridge

Applications
Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

Features
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz Arm® 926EJ core**
  - 512KB of embedded SRAM for code space and buffers
- **Four-Lane MIPI® Camera Serial Interface v2.0 (CSI-2) Input**
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I²C, UART, SPI, and 12 GPIOs
- **Supports Industry-Standard Video Data Formats**
  - RAW8/10/12/14², YUV422/444³, RGB888/666/565⁴
- **Supports Uncompressed Streaming Video**
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- **Packages**
  - 121-ball BGA (10 x 10 x 1.7 mm)

Collateral
- **Datasheet:** CX3 Datasheet
- **Reference Design Kit:** CX3 Reference Design Kit
- **Software Development Kit:** EZ-USB FX3 SDK

Availability
- **Production:** Now

1 Mobile Industry Processor Interface
2 Video format for luminance and chrominance components
3 Video format for raw video data
4 Video format for red, green and blue pixel components
EZ-USB GX3
USB 3.1 Gen 1 to GigE\(^1\) Bridge

**Applications**
USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs, and other embedded systems

**Features**
- One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC\(^2\)
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- IEEE 802.3az\(^3\) Support for Low-Power Idle State
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN\(^4\) features
- Supports Optional EEPROM to Store USB Descriptors
  - Integrates on-chip power-on-reset (POR) circuitry
- Packages
  - 68-QFN (8 x 8 x 0.85 mm)

**Collateral**
- Datasheet: [GX3 Datasheet](#)
- Reference Design Kit: [GX3 Reference Design Kit](#)
- Software & Drivers: [GX3 Drivers](#)

**Availability**
Production: Now

GX3: USB 3.1 Gen 1 to GigE\(^1\) Bridge

1 Gigabit Ethernet
2 Media access controller that provides the address to an Ethernet node
3 A new-energy efficient Ethernet standard
4 An Ethernet standard that allows a computer to be turned on by a network message
**Applications**

Docking stations for notebook PCs and tablets, PC motherboards, servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

**Features**

- **USB 3.1 Gen 1-Compliant Four-Port Hub Controller**
  - USB-IF certified (Test ID: 33000047)
  - WHQL certified for Windows 7, Window 8, Windows 8.1
- **Shared Link™**
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- **Ghost Charge™**
  - Enables USB charging while the hub is disconnected from a USB Host
- **Charging Standard support**
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- **Programming of External EEPROM via USB**
- **Configurable USB SS and USB 2.0 PHY (drives 11″ trace)**
- **Packages**
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

**Collateral**

**Datasheet:** [HX3 Datasheet](#)

**Kit:** [CY4609, CY4603, CY4613](#)

**Configuration Utility:** [Blaster Plus](#)

**App Notes:** [HX3 Hardware Design Guide (AN91378)](#)

---

1. A Cypress GUI-based PC application for setting HX3 configuration parameters
2. Transaction translator

---

**Availability**

**Production:** Now
EZ-USB HX3C
USB 3.1 Gen 1 Type-C PD Hub

Applications
USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features
- **USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD**
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- **Integrated Type-C Transceivers, Supporting Two Type-C Ports**
  - Integrated termination resistors (R_P and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\)
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- **Ghost Charge™**
  - Charging DS without US connection
- **Firmware Upgradable Over USB**
- **System-Level ESD on Configuration Channel (CC) Pins**
  - 8 kV Contact, 15 kV Air
- **Configurable USB SS and USB 2.0 PHY (drives 11" trace)**
- **Packages**
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral

<table>
<thead>
<tr>
<th>Datasheet:</th>
<th>HX3C Datasheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Design:</td>
<td>HX3C Type-C Monitor/Dock Reference Design</td>
</tr>
</tbody>
</table>

Availability

Production: Now

\(^1\) Termination resistors: R_P read as a DFP, R_D as a UFP
\(^2\) A USB Device controller that is used to implement the USB Billboard Device Class
\(^3\) Transaction Translator

Informs the USB Host of the supported Alternate Modes as well as any failures
Cypress Roadmap: RAM Solutions
## Table of Contents

<table>
<thead>
<tr>
<th>Page</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>87</td>
<td>Nonvolatile RAM: F-RAM™, nvSRAM</td>
</tr>
<tr>
<td>95</td>
<td>Asynchronous SRAM: Low-Power (MoBL®), Fast, PowerSnooze™</td>
</tr>
<tr>
<td>103</td>
<td>HyperRam: High-performance Pseudo-static RAM</td>
</tr>
<tr>
<td>106</td>
<td>Synchronous SRAM: Std Sync, NoBL®, QDR/DDR-II, QDR-IV</td>
</tr>
</tbody>
</table>
Nonvolatile RAM

F-RAM, nvSRAM
<table>
<thead>
<tr>
<th>LPC™ F-RAM</th>
<th>Processor Companion</th>
<th>Parallel F-RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>F-RAM™ Portfolio</strong>&lt;br&gt;Low Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Low Power</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>High Endurance</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>512Kb–16Mb</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>4Kb–256Kb</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>4Mb–256Mb</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Up to 16Mb</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>1.8 V, 108-MHz QSPI</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>256Kb</strong></td>
<td><strong>FM25V02A</strong>&lt;br&gt;2Mb; 2.0–3.6 V&lt;br&gt;40-MHz SPI; Ind</td>
<td><strong>FM25V202A</strong>&lt;br&gt;2Mb; 2.0–3.6 V&lt;br&gt;40-MHz SPI; Ind&lt;br&gt;60 ns; x16; Auto A</td>
</tr>
<tr>
<td><strong>1Mb</strong></td>
<td><strong>CY15B102Q</strong>&lt;br&gt;2Mb; 2.0–3.6 V&lt;br&gt;25-MHz SPI; Auto E</td>
<td><strong>CY15B102N</strong>&lt;br&gt;2Mb; 2.0–3.6 V&lt;br&gt;60 ns; x16; Auto A</td>
</tr>
<tr>
<td><strong>512Kb</strong></td>
<td><strong>FM25V05</strong>&lt;br&gt;512Kb; 2.0–3.6 V&lt;br&gt;40-MHz SPI; Ind, Auto A</td>
<td><strong>CY15B101N</strong>&lt;br&gt;1Mb; 2.0–3.6 V&lt;br&gt;60 ns; x16; Auto A</td>
</tr>
<tr>
<td><strong>128Kb</strong></td>
<td><strong>FM25V01A</strong>&lt;br&gt;128Kb; 2.0–3.6 V&lt;br&gt;40-MHz SPI; Ind, Auto A</td>
<td></td>
</tr>
<tr>
<td><strong>FM25640/B/CL64B</strong>&lt;br&gt;64Kb; 3.3, 5.0 V&lt;br&gt;20-MHz SPI; Ind, Auto E</td>
<td><strong>FM18W08</strong>&lt;br&gt;64Kb; 2.7–5.5 V&lt;br&gt;70 ns; x8; Ind</td>
<td></td>
</tr>
<tr>
<td><strong>FM25C160/L16</strong>&lt;br&gt;16Kb; 3.3, 5.0 V&lt;br&gt;20-MHz SPI; Ind, Auto E</td>
<td><strong>FM3164/31(L)/276</strong>&lt;br&gt;64Kb; 3.3, 5.0 V&lt;br&gt;1-MHz SWP; Ind, RTC; Power Fail; Watchdog; Counter</td>
<td></td>
</tr>
<tr>
<td><strong>FM25M040/L04</strong>&lt;br&gt;4Kb; 3.3, 5.0 V&lt;br&gt;20-MHz SPI; Ind, Auto E</td>
<td><strong>FM31256/31(L)/278</strong>&lt;br&gt;256Kb; 3.3, 5.0 V&lt;br&gt;1-MHz SWP; Ind, RTC; Power Fail; Watchdog; Counter</td>
<td></td>
</tr>
<tr>
<td><em>Low-pin-count</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>Industrial grade -40 °C to +85 °C</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>Quad serial peripheral interface</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>Ultra-low-energy</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>AEC-Q001 -40 °C to +85 °C</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>AEC-Q001 -40 °C to +125 °C</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>Real-time clock</em></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1. Low-pin-count
2. Industrial grade -40 °C to +85 °C
3. Quad serial peripheral interface
4. Ultra-low-energy
5. AEC-Q001 -40 °C to +85 °C
6. AEC-Q001 -40 °C to +125 °C
7. Real-time clock
## Cypress Roadmap: RAM Solutions

### Excelon™ F-RAM Portfolio

#### Ultra Low Power | High Speed | High Endurance

<table>
<thead>
<tr>
<th>Excelon Auto</th>
<th>Excelon Ultra</th>
<th>Excelon LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY15B116QSN</td>
<td>CY15V116QSN</td>
<td>CY15B116QI/N</td>
</tr>
<tr>
<td>16Mb; 1.8–3.6 V</td>
<td>16Mb; 1.7–1.99 V</td>
<td>16Mb; 1.6–3.6 V</td>
</tr>
<tr>
<td>24-ball FBGA</td>
<td>24-ball FBGA</td>
<td>24-ball FBGA</td>
</tr>
<tr>
<td>108-MHz QSPI</td>
<td>108-MHz QSPI</td>
<td>20/40-MHz SPI, Comm4, Ind</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CY15B110QSN</th>
<th>CY15V108QSN</th>
<th>CY15B108QI/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Mb; 1.8–3.6 V</td>
<td>8Mb; 1.7–1.89 V</td>
<td>8Mb; 1.7–1.89 V</td>
</tr>
<tr>
<td>24-ball FBGA</td>
<td>24-ball FBGA</td>
<td>24-ball FBGA</td>
</tr>
<tr>
<td>108-MHz QSPI</td>
<td>108-MHz QSPI</td>
<td>20/40-MHz SPI, Comm4, Ind</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CY15B104QSN</th>
<th>CY15V104QSN</th>
<th>CY15B104QI/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb; 1.8–3.6 V</td>
<td>4Mb; 1.7–1.89 V</td>
<td>4Mb; 1.7–1.89 V</td>
</tr>
<tr>
<td>8-pin SOIC</td>
<td>8-pin SOIC</td>
<td>8-pin SOIC</td>
</tr>
<tr>
<td>50-MHz SPI</td>
<td>50-MHz SPI</td>
<td>20/50-MHz SPI, Comm4, Ind</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CY15B102QSN</th>
<th>CY15V102QSN</th>
<th>CY15B102QI/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Mb; 1.8–3.6 V</td>
<td>2Mb; 1.7–1.89 V</td>
<td>2Mb; 1.8–3.6 V</td>
</tr>
<tr>
<td>8-pin SOIC</td>
<td>8-pin SOIC</td>
<td>8-pin SOIC</td>
</tr>
<tr>
<td>50-MHz SPI</td>
<td>50-MHz SPI</td>
<td>50-MHz SPI, Ind</td>
</tr>
</tbody>
</table>

1. Quad serial peripheral interface  
2. AEC-Q100 -40°C to +105°C  
3. Industrial grade -40°C to +85°C  
4. Commercial grade 0°C to +70°C  
5. AEC-Q100 -40°C to +85°C  
6. AEC-Q100 -40°C to +125°C
### nvSRAM Portfolio

**High Density | High Speed**

<table>
<thead>
<tr>
<th>Parallel nvSRAM</th>
<th>LPC(^1) nvSRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY14B116R/S 16Mb, 3.0 V 25, 45 ns; x32; Ind(^2) RTC(^3)</td>
<td>CY14B116F/G 16Mb, 3.0, 1.8 V I/O 30 ns, QFP1, 1.0 x8, x16, Ind</td>
</tr>
<tr>
<td>CY14B104NA 4Mb, 3.0 V 25, 45 ns; x8, RTC</td>
<td>CY14B108M/N 16Mb, 3.0 V 25, 45 ns; x16, Ind</td>
</tr>
<tr>
<td>CY14B104K/L 4Mb, 3.0 V 25, 45 ns; x8, RTC</td>
<td>CY14B108K/L 8Mb, 3.0 V 25, 45 ns; x8, Ind</td>
</tr>
<tr>
<td>CY14B101KA/LA 1Mb, 3.0 V 25, 45 ns; x8, Ind</td>
<td>CY14B101M/NA 4Mb, 3.0 V 25, 45 ns; x8, Ind</td>
</tr>
<tr>
<td>CY14B256KLA/NA 256Kb, 3.0 V 25, 45 ns; x8, Ind</td>
<td>CY14B256PA 256Kb, 3.0 V 40-MHz SPI; Ind RTC</td>
</tr>
<tr>
<td>CY14E256LA 256Kb, 5.0 V 25, 45 ns; x8, Ind</td>
<td>CY14B064PA 64Kb, 3.0 V 40-MHz SPI; Ind RTC</td>
</tr>
<tr>
<td>CY14B256LA 256Kb, 5.0 V 35 ns; x8, Ind</td>
<td>CY14B256I 256Kb, 3.0 V 3.4-MHz SPI; Ind RTC</td>
</tr>
<tr>
<td>CY14E256LA 256Kb, 5.0 V 35 ns; x8, Ind</td>
<td>CY14B064I 64Kb, 3.0 V 3.4-MHz SPI; Ind RTC</td>
</tr>
</tbody>
</table>

1. Low-pin-count
2. Industrial grade -40 °C to +85 °C
3. Real-time clock
4. Open NAND flash interface
5. Error-correcting code
6. AEC-Q100 -40 °C to +125 °C
7. Quad serial peripheral interface
8. Extended Industrial grade -40 °C to +105 °C
9. Military grade -55 °C to +125 °C

- **Concept**: Development Sampling Production
- **Industrial Automotive**: Development Sampling Production
# Nonvolatile RAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(ES) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Excelon F-RAM</td>
<td>Ultra</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>Auto</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>LP</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Serial F-RAM</td>
<td>SPI, SPI</td>
<td>1.71–1.89 V</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td></td>
<td>1.8–3.6 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Serial F-RAM</td>
<td>SPI, I²C</td>
<td>4Kb–4Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3/5 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Processor Companion</td>
<td>I²C</td>
<td>64Kb, 256Kb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3/5 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Parallel F-RAM</td>
<td>x8, x16</td>
<td>64Kb–4Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3/5 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Parallel nvSRAM</td>
<td>x8, x16</td>
<td>256Kb–16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 V, 5 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>Serial nvSRAM</td>
<td>I²C, SPI, QSPI</td>
<td>64Kb–1Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 V, 5 V</td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
</tbody>
</table>

---

**Legend:**
- **CONCEPT**
- **SAMPLES**
- **PRODUCTION**
- **EOL**
2Mb-to-16Mb Excelon™ F-RAM Family

**Applications**
- Medical devices, wearables, industrial control and automation, and automotive

**Features**

- **Excelon Ultra**
  - 2Mb to 16Mb
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - Industrial temperature range grade “I”: -40 °C to +85 °C

- **Excelon Auto**
  - 4Mb to 16Mb Auto “A”, 8Mb to 16Mb Auto “S”, 2Mb to 8Mb Auto “E”
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - 40/50-MHz Serial Peripheral Interface (SPI)
  - Automotive temperature range grade “A”: -40 °C to +85 °C
  - Automotive temperature range grade “S”: -40 °C to +105 °C
  - Automotive temperature range grade “E”: -40 °C to +125 °C

- **Excelon LP**
  - 2Mb to 16Mb
  - 20-MHz SPI (Commercial/Industrial), 40/50-MHz SPI (Industrial)
  - Ultra low (0.75 µA) deep power down current
  - Ultra low (0.1 µA) hibernate current
  - Commercial temperature range grade “C”: 0 °C to +70 °C
  - Industrial temperature range grade “I”: -40 °C to +85 °C

- **Common features for Excelon Ultra/Auto/LP**
  - Operating voltage ranges: 1.71 V to 1.89 V, 1.80 V to 3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

**Collateral**
- Datasheets: 4Mb Excelon Ultra; 2Mb Excelon Auto; 8Mb Excelon LP

---

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>Standby Current (Typ.)</th>
<th>Active Current (Typ.)</th>
<th>Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Mb</td>
<td>2.3 µA</td>
<td>2.4 mA</td>
<td>SOIC (8), TDFN (8)</td>
</tr>
<tr>
<td>4Mb</td>
<td>2.3 µA</td>
<td>2.4 mA</td>
<td>SOIC (8), GQFN (8)</td>
</tr>
<tr>
<td>8Mb</td>
<td>3.5 µA</td>
<td>2.6 mA</td>
<td>SOIC (8), GQFN (8)</td>
</tr>
<tr>
<td>16Mb</td>
<td>7.3 µA</td>
<td>3.0 mA</td>
<td>FBGA (24)</td>
</tr>
</tbody>
</table>

**Availability**

- **Sampling:** Now (2Mb Ind), Q420 (8Mb Auto S, 16Mb)
- **Production:** Now (2Mb Auto E, 4Mb Auto A/Ultra/LP & 8Mb LP), Q220 (2Mb Ind), Q221 (16Mb, 8Mb Auto S)

1 Quad SPI has 4 I/Os
# F-RAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>8-pin SOIC</th>
<th>8-pin DFN</th>
<th>8-pin GQFN</th>
<th>8-pin EIAJ</th>
<th>14-pin SOIC</th>
<th>28-pin SOIC</th>
<th>28-pin TSOP I</th>
<th>32-pin TSOP I</th>
<th>44-pin TSOP II</th>
<th>24-ball FBGA</th>
<th>48-ball FBGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SPI</strong></td>
<td>4Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Kb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PC</strong></td>
<td>4Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>16Kb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>64Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Processor Companion</strong></td>
<td>64Kb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Parallel</strong></td>
<td>64Kb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
# nvSRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>8-pin SOIC</th>
<th>8-pin DFN</th>
<th>16-pin SOIC</th>
<th>28-pin SOIC</th>
<th>28-pad LCC</th>
<th>32-pin SOIC</th>
<th>44-pin TSOP II</th>
<th>48-ball FBGA</th>
<th>48-pin SSOP</th>
<th>48-pin TSOP I</th>
<th>54-pin TSOP II</th>
<th>60-ball FBGA</th>
<th>165-ball FBGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SPI</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PC</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Parallel Asynchronous SRAM

Low-Power (MoBL®), Fast, PowerSnooze™
## Parallel Asynchronous SRAM Portfolio

**High Density** | **Wide Voltage Range** | **Automotive A¹, E²** | **On-Chip ECC**

### Fast SRAM

<table>
<thead>
<tr>
<th>Density</th>
<th>32Mb–64Mb</th>
<th>2Mb–16Mb</th>
<th>64Kb–1Mb</th>
</tr>
</thead>
<tbody>
<tr>
<td>32Mb–64Mb</td>
<td>CY7C107x</td>
<td>CY7C106xGN</td>
<td>CY7C105s</td>
</tr>
<tr>
<td>2Mb–16Mb</td>
<td>CY7C1012</td>
<td>CY7C105s</td>
<td>CY7C104x</td>
</tr>
<tr>
<td>64Kb–1Mb</td>
<td>CY7C1020</td>
<td>CY7C1019/21</td>
<td>CY7C1019/21</td>
</tr>
</tbody>
</table>

### Low-Power SRAM (MoBL®)

<table>
<thead>
<tr>
<th>Non-ECC (≥90 nm)</th>
<th>ECC (65 nm)</th>
<th>Non-ECC (≥90 nm)</th>
<th>ECC (65 nm)</th>
<th>ECC (65 nm) ULP®</th>
<th>ECC (65 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY6218x</td>
<td>64Mb: 1.8, 3.0 V</td>
<td>55 ns; x16, x32</td>
<td>64Mb: 1.8, 3.0 V</td>
<td>55 ns; x16, x32</td>
<td>64Mb: 1.8, 3.0 V</td>
</tr>
<tr>
<td>CY6217x</td>
<td>32Mb: 1.8–5.0 V</td>
<td>55 ns; x16</td>
<td>32Mb: 1.8–5.0 V</td>
<td>55 ns; x16</td>
<td>32Mb: 1.8–5.0 V</td>
</tr>
<tr>
<td>CY6216x</td>
<td>16Mb: 1.8–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>16Mb: 1.8–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>16Mb: 1.8–5.0 V</td>
</tr>
<tr>
<td>CY6215x</td>
<td>8Mb: 1.8, 3.0, 5.0 V</td>
<td>45 ns; x8, x16</td>
<td>8Mb: 1.8, 3.0, 5.0 V</td>
<td>45 ns; x8, x16</td>
<td>8Mb: 1.8, 3.0, 5.0 V</td>
</tr>
<tr>
<td>CY6214x</td>
<td>4Mb: 1.8–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>4Mb: 1.8–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>4Mb: 1.8–5.0 V</td>
</tr>
<tr>
<td>CY6213x</td>
<td>2Mb: 1.8, 2.5–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>2Mb: 1.8, 2.5–5.0 V</td>
<td>45 ns; x8, x16</td>
<td>2Mb: 1.8, 2.5–5.0 V</td>
</tr>
<tr>
<td>CY7S106x</td>
<td>8Mb: 1.8V, 3.0V</td>
<td>45 ns; x8, x16, x32</td>
<td>8Mb: 1.8V, 3.0V</td>
<td>45 ns; x8, x16, x32</td>
<td>8Mb: 1.8V, 3.0V</td>
</tr>
</tbody>
</table>

### PowerSnooze™

1 AEC-Q100 –40°C to +85°C
2 AEC-Q100 –40°C to +125°C
3 More Battery Life
4 A Fast SRAM with a deep-sleep mode in addition to the conventional standby
5 Ultra-Low-Power

---

¹ AEC-Q100
² AEC-Q100
³ Ultra-Low-Power
⁴ More Battery Life

---

96 Cypress Roadmap: RAM Solutions – DMIT
# Parallel Asynchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>MoBL SRAM ULP 65 nm, ECC Parallel Asynchronous</td>
<td>8Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
<tr>
<td></td>
<td>16Mb, 32Mb, 64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MoBL SRAM 65 nm, ECC Parallel Asynchronous</td>
<td>4Mb, 8Mb, 16Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
<tr>
<td>MoBL SRAM ≥ 90 nm, Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
<tr>
<td>PowerSnooze SRAM 65 nm, ECC Parallel Asynchronous</td>
<td>4Mb, 16Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
<tr>
<td>Fast SRAM 65 nm, ECC Parallel Asynchronous</td>
<td>2Mb, 4Mb, 8Mb, 16Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
<tr>
<td>Fast SRAM ≥ 90 nm Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
<td>Q4</td>
</tr>
</tbody>
</table>
Low-Power SRAM Family with ECC

**Applications**

Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers and automotive.

**Features**

- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC\(^1\) logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS\(^2\)-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

**Collateral**

Datasheet: [Asynchronous SRAM with ECC](#)

---

1. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation.
2. Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components.

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Standby Current (Maximum at 85°C)</th>
<th>Standby Current (Typical at 25°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY6214x</td>
<td>8.7 µA</td>
<td>3.5 µA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY6215x</td>
<td>16.0 µA</td>
<td>5.9 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY6216x</td>
<td>16.0 µA</td>
<td>5.9 µA</td>
</tr>
</tbody>
</table>

**Availability**

Production: Now
Ultra Low-Power MoBL®1 SRAM Family with ECC²

**Applications**
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, automotive, and computation servers

**Features**

- **Speed**
  - Access time: 45/55 ns
  - Bus-width configurations: x8 and x16
- **Low Power**
  - Standby current: 8.0 µA max for 16Mb
- **Operating Voltage Range**
  - 2.2 V to 3.6 V, 1.65V to 2.25V (8Mb)
- **Features**
  - ECC² logic to detect and correct single-bit errors
- **Temperature Grades**
  - 8Mb, 16Mb, 32Mb, 64Mb; Industrial grade: -40 °C to +85 °C
  - 8Mb; Automotive A grade: -40 °C to +85 °C
  - 8Mb; Automotive E grade: -40 °C to +125 °C
- **RoHS³-compliant Packages**
  - All existing MoBL packages supported

**Collateral**
Datasheet: 64Mb contact sales; 32Mb contact sales
16Mb ULP SRAM; 8Mb contact sales

---

**SRAM with ECC**

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Standby Current (Max at 85°C)</th>
<th>Standby Current (Typ at 25°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Mb</td>
<td>CY6215x</td>
<td>6.5 µA</td>
<td>1.4 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY6216x</td>
<td>8.0 µA</td>
<td>1.5 µA</td>
</tr>
<tr>
<td>32Mb</td>
<td>CY6217x</td>
<td>19.0 µA</td>
<td>3.0 µA</td>
</tr>
<tr>
<td>64Mb</td>
<td>CY6218x</td>
<td>38.0 µA</td>
<td>6.0 µA</td>
</tr>
</tbody>
</table>

---

1 MoBL: More Battery Life
2 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
3 Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
Fast SRAM Family with PowerSnooze™

Applications
Programmable logic controllers, handheld devices, multifunction printers, computation servers and automotive

Features
- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS-Compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

Datasheet: Asynchronous SRAM with ECC

1 A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
2 Error-correcting code
3 Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (Maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>10 ns</td>
<td>15 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
</tbody>
</table>

Production: Now
Fast SRAM Family with ECC

**Applications**

Switches and routers, IP phones, test equipment, computation servers, automotive, military and aerospace systems

**Features**

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS²-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

**Collateral**

Datasheet: [Asynchronous SRAM with ECC](#)

---

1. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2. Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

**SRAM with ECC**

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Operating Current (Maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7C104x</td>
<td>10 ns</td>
<td>45 mA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY7C105X</td>
<td>10 ns</td>
<td>110 mA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7C106x</td>
<td>10 ns</td>
<td>110 mA</td>
</tr>
</tbody>
</table>

**Availability**

Production: Now
# Asynchronous SRAM Packages

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast</td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-Power</td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
HyperRAM

High-performance Pseudo-static RAM
# HyperRAM™ Portfolio

<table>
<thead>
<tr>
<th>Density</th>
<th>Initial Access/DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>64Mb</strong></td>
<td>36 ns/100 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td><strong>128Mb</strong></td>
<td>36 ns/166 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td><strong>256Mb</strong></td>
<td>35 ns/200 MHz</td>
<td>I, A, V, B</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Density</th>
<th>Initial Access/DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>64Mb</strong></td>
<td>36 ns/100 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td><strong>128Mb</strong></td>
<td>36 ns/166 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td><strong>256Mb</strong></td>
<td>35 ns/200 MHz</td>
<td>I, A, V, B</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>HyperRAM 1.0 S27KL-1</th>
<th>HyperRAM 1.0 S27KS-1</th>
<th>HyperRAM 2.0 S27KL-2</th>
<th>HyperRAM 2.0 S27KS-2</th>
<th>HyperRAM 2.0 S27KL-3</th>
<th>HyperRAM 2.0 S27KS-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-nm DR, 3.0 V HyperBus I/F</td>
<td>63-nm DR, 1.8 V HyperBus I/F</td>
<td>38-nm DR, 3.0 V HyperBus I/F</td>
<td>38-nm DR, 1.8 V HyperBus I/F</td>
<td>38-nm DR, 3.0 V Octal SPI I/F</td>
<td>38-nm DR, 1.8 V Octal SPI I/F</td>
</tr>
</tbody>
</table>

* I = Industrial: -40 °C to +85 °C  
  A = Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C  
  V = Industrial-plus: -40 °C to +105 °C  
  B = Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C

1 Stacked die
HyperRAM™ Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S27KS-1 (1.8 V)</td>
<td>128Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KL-1 (3.0 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperRAM 1.0</td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63-nm PS-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KS-2/3 (1.8 V)</td>
<td>128Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KL-2/3 (3.0 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperRAM 2.0</td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>38-nm PS-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Stacked die

Products supported by Longevity Program unless noted

- **Concept**
- **Production**
- **Samples**
- **EOL - LTB**
- **EOL - LTS**
Synchronous SRAM

Std Sync, NoBL® , QDR-II, DDR-II, QDR-IV
Synchronous SRAM Portfolio

High Random Transaction Rate (RTR) | Low Latency | High Bandwidth

<table>
<thead>
<tr>
<th>Standard Sync and NoBL</th>
<th>Standard Sync and NoBL with ECC</th>
<th>QDR®-II/DDR-II</th>
<th>QDR-II+/DDR-II+</th>
<th>QDR-II+/DDR-II+X</th>
<th>QDR-IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTR: 250 MT/s (max.)</td>
<td>RTR: 250 MT/s (max.)</td>
<td>RTR: 666 MT/s (max.)</td>
<td>RTR: 666 MT/s (max.)</td>
<td>RTR: 900 MT/s (max.)</td>
<td>RTR: 2.1 GT/s (max.)</td>
</tr>
<tr>
<td>BW: 18 Gbps (max.)</td>
<td>BW: 18 Gbps (max.)</td>
<td>BW: 47.6 Gbps (max.)</td>
<td>BW: 79.2 Gbps (max.)</td>
<td>BW: 91.1 Gbps (max.)</td>
<td>BW: 153.5 Gbps (max.)</td>
</tr>
<tr>
<td>Latency: 1 Cycle</td>
<td>Latency: 1 Cycle</td>
<td>Latency: 1.5 Cycles</td>
<td>Latency: 2 or 2.5 Cycles</td>
<td>Latency: 2.5 Cycles</td>
<td>Dual-Port Bidirectional</td>
</tr>
<tr>
<td>Pipeline and Flow Modes</td>
<td>Pipeline and Flow Modes</td>
<td>CIO and SIO^4, ODT</td>
<td>CIO, ODT</td>
<td>Pipeline and Flow Modes</td>
<td></td>
</tr>
</tbody>
</table>

Density

<table>
<thead>
<tr>
<th>CY7C147/8xB</th>
<th>CY7C144/6xK</th>
<th>CY7C137/8xD/K</th>
<th>CY7C135/6xC</th>
<th>CY7C134/2xG</th>
</tr>
</thead>
<tbody>
<tr>
<td>256 Mb: 133–250 MHz</td>
<td>36 Mb: 133–250 MHz</td>
<td>16 Mb: 100–250 MHz</td>
<td>9 Mb: 100–250 MHz</td>
<td>2–4 Mb: 100–250 MHz</td>
</tr>
<tr>
<td>2.5 V; x18, x36</td>
<td>2.5 V; x18, x36</td>
<td>3.3 V; x18, x32, x36</td>
<td>3.3 V; x18, x32, x36</td>
<td>3.3 V; x18, x32, x36</td>
</tr>
</tbody>
</table>

Density

<table>
<thead>
<tr>
<th>CY7C161/2xKV18</th>
<th>CY7C151/2xKV18</th>
<th>CY7C141/2xKV18</th>
<th>CY7C131/2x9xKV18</th>
<th>CY7C1911xKV18</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8 V; x9, x18, x36</td>
<td>1.8 V; x18, x36</td>
<td>1.8 V; x8, x18, x36</td>
<td>1.8 V; x8, x18, x36</td>
<td>1.8 V; x9</td>
</tr>
<tr>
<td>Burst 2, 4</td>
<td>Burst 2, 4</td>
<td>Burst 2, 4</td>
<td>Burst 2, 4</td>
<td>Burst 2, 4</td>
</tr>
</tbody>
</table>

Random Transaction Rate

1 Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
2 Error-correcting code
3 Common I/O
4 Separate I/O
5 On-die termination
6 Radiation hardened, military grade
7 AEC-Q100: -40 °C to +125 °C

Density

107 Cypress Roadmap: RAM Solutions – DMIT
## Synchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>QDR®-IV SRAM</strong></td>
<td>65 nm, ECC</td>
<td>72Mb, 144Mb</td>
</tr>
<tr>
<td></td>
<td>2.1 GT/s, 153.5 Gbps</td>
<td></td>
</tr>
<tr>
<td><strong>QDR-II-X SRAM</strong></td>
<td>65 nm, ECC</td>
<td>36Mb, 72Mb</td>
</tr>
<tr>
<td></td>
<td>900 MT/s, 91.1 Gbps</td>
<td></td>
</tr>
<tr>
<td><strong>QDR-II+ SRAM</strong></td>
<td>65 nm, ECC</td>
<td>18Mb, 36Mb, 72Mb(^1), 144Mb</td>
</tr>
<tr>
<td></td>
<td>666 MT/s, 79.2 Gbps</td>
<td></td>
</tr>
<tr>
<td><strong>QDR-II SRAM</strong></td>
<td>65 nm</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
</tr>
<tr>
<td></td>
<td>666 MT/s, 47.9 Gbps</td>
<td></td>
</tr>
<tr>
<td><strong>Standard Sync and NoBL® SRAM</strong></td>
<td>65 nm, ECC</td>
<td>18Mb, 36Mb</td>
</tr>
<tr>
<td></td>
<td>250 MT/s, 18 Gbps</td>
<td></td>
</tr>
<tr>
<td><strong>Standard Sync and NoBL SRAM</strong></td>
<td>65 nm/90 nm</td>
<td>2Mb, 4Mb, 9Mb(^2), 18Mb(^3), 36Mb(^3), 72Mb</td>
</tr>
<tr>
<td></td>
<td>250 MT/s, 18 Gbps</td>
<td></td>
</tr>
</tbody>
</table>

1 Radiation hardened, military grade
2 AEC-Q100 -40 °C to +125 °C
3 65-nm

### Notes:
- **QDR®** - Quad Data Rate
- **EOL** - End of Life
- **SRAM** - Synchronous Random Access Memory
- **ECC** - Error Correcting Code
- **Q1** - First Quarter
- **Q2** - Second Quarter
- **Q3** - Third Quarter
- **Q4** - Fourth Quarter

### Temperature Ranges:
- **AEC-Q100** - -40 °C to +125 °C
Standard Synchronous SRAM With On-Chip ECC

**Applications**
Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

**Features**
- **Speed**
  - Available in two modes: Pipeline and Flow-Through
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

**Collateral**
Datasheets: [36M Sync SRAM](#), [18M Sync SRAM](#)

**Synchronous SRAM**

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with On-Chip ECC Pipeline</td>
<td>18Mb</td>
<td>CY7C1370/2K</td>
<td>250 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>CY7C1440/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync with On-Chip ECC Flow-Through</td>
<td>18Mb</td>
<td>CY7C1371/3K</td>
<td>133 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>CY7C1441/3K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2. Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
3. Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
4. The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data
NoBL® SRAM With On-Chip ECC¹

Applications
Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

Features
- **Speed**
  - Available in two modes²: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18, x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral
Datasheets: 36M NoBL SRAM, 18M NoBL SRAM

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
<td>CY7C1380/2K</td>
<td>250MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Pipeline</td>
<td>36Mb</td>
<td>CY7C1460/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
<td>CY7C1381/3K</td>
<td>133MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Flow-Through</td>
<td>36Mb</td>
<td>CY7C1461/3K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
² Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
³ The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

Availability
Production: Now
QDR®-IV SRAM

**Applications**
- Switches and routers, high-performance computing, military and aerospace systems, test and measurement

**Features**
- **Speed**
  - Available in two options: QDR-IV HP (RTR 1,334 MT/s) and QDR-IV XP (RTR 2,132 MT/s)
  - Two independent, bidirectional DDR1 data ports
  - Bus widths: x18, x360.13
- **Features**
  - ECC² to reduce soft error rate to less than 0.01 FIT/Mb³
  - Bus inversion to reduce simultaneous switching I/O noise
  - On-die termination (ODT) to reduce board complexity
  - De-skew training⁴ to improve signal-capture timing
  - I/O levels: 1.2–1.25 V (HSTL/SSTL), 1.1–1.2 V (POD⁵)
- **Package**
  - 361-pin FCBGA⁶

**Collateral**
- **Datasheets:** CY7C4122KV13/CY7C4142KV13
  CY7C4121KV13/CY7C4141KV13
  CY7C4022KV13/CY7C4042KV13
  CY7C4021KV13/CY7C4041KV13

---

1. Double Data Rate: Two data transfers per clock cycle
2. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors
3. Failures in Time per Megabit
4. An iterative algorithm for assessing and eliminating the skew between multiple data signals
5. Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up drive strength
6. Flip-Chip Ball Grid Array

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>Maximum Frequency</th>
<th>RTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDR-IV HP</td>
<td>72Mb</td>
<td>CY7C40x1KV13</td>
<td>667 MHz</td>
<td>1,334 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x1KV13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-IV XP</td>
<td>72Mb</td>
<td>CY7C40x2KV13</td>
<td>1,066 MHz</td>
<td>2,132 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td>CY7C41x2KV13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Availability**
- **Production:** Now
## Synchronous SRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>100-pin TQFP</th>
<th>119-ball BGA</th>
<th>165-ball BGA</th>
<th>209-ball BGA</th>
<th>361-ball BGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Std Sync</td>
<td>18Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>NoBL</td>
<td>2Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>9Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>QDR</td>
<td>9Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
Timing Solutions Portfolio
## Clock Synthesizer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27430</td>
<td>4-PLL; Maximum Frequency: 700 MHz 12 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EM1; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; IndP; 48-QFN</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY27410</td>
<td>4-PLL; Maximum Frequency: 700 MHz 8 Outputs; Diff &amp; SE; PCIe 3.0; VCXO; EM1; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A S; 48-QFN</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCY254x/CY251x</td>
<td>1-4 PLL; Maximum Frequency: 200 MHz 3-9 Outputs; I2C; EM1; Low Power 100-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Maximum Frequency: 166 MHz 3-8 Outputs; CMOS; Low Power 200-ps PVJ V; VCXO; Ind; 3.3 V/5 V 8/16/20-SOIC; 16-TSSOP</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2429x</td>
<td>1-PLL; Maximum Frequency: 200 MHz 2-5 Outputs; HC5L, CMOS; EM1 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2239x</td>
<td>3-4 PLL; Maximum Frequency: 400 MHz 5-8 Outputs; LVPECL, CMOS; I2C 400-ps PVJ; VCXO; 3.3 V Ind; Auto A E; 16-TSSOP; 32-QFN</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Maximum Frequency: 200 MHz 1-3 Outputs; CMOS; EM1 110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY22050/150</td>
<td>1-PLL; Maximum Frequency: 200 MHz 6 Outputs; CMOS; IC 250-ps PPJ; Ind 2.5 V/3.3 V; 16-TSSOP</td>
<td>2020 Q1 2021 Q1 2022 Q1 2023 Q1 2024 Q1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Differential and single-ended outputs
2. Voltage-controlled crystal oscillation
3. Electro Magnetic Interference reduction using Lexmark profile
4. Integrated phase noise across 12-kHz to 20-MHz offset
5. Industrial grade: -40°C to +85°C
6. AEC-Q100: -40°C to +85°C
7. AEC-Q100: -40°C to +105°C
8. Power management options
9. Cycle-to-cycle jitter
10. Peak-to-peak period jitter
11. AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted.
# Oscillator Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High Performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY294x</td>
<td>1-PLL; Maximum Frequency: 2.1 GHz 1 Output; Diff &amp; SE; 40/100 GbE; VCXO; 0.11-ps RMS Jitter; Ind; 8-LCC (7 x 5, 5 x 3.2); 16-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY51x7</td>
<td>1-PLL; Maximum Frequency: 2.1 GHz 1 Output; Diff &amp; SE; 40/100 GbE; VCXO; 0.11-ps RMS Jitter; Ind; 1.8 V/2.5/3.3 V; WAFFER/DIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY22x (FleXO™)</td>
<td>1 PLL; Maximum Frequency: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL Frequency Margining; 0.6-ps RMS Jitter; Ind; 6-LCC (7 x 5, 5 x 3.2); 8-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY25701</td>
<td>1-PLL; Maximum Frequency: 166 MHz 1 Output; CMOS; EMI; 85-ps CCJ; Ind; 3.3 V; 4-LCC (5 x 3.2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2037/5037</td>
<td>1-PLL; Maximum Frequency: 133 MHz 1 Output; CMOS; 100-ps CCJ; Ind; 3.3 V/5.0 V; WAFER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY5077</td>
<td>1-PLL; Maximum Frequency: 166 MHz 1 Output; CMOS; 75-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V; WAFER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY5057</td>
<td>1-PLL; Maximum Frequency: 170 MHz 1 Output; CMOS; EMI; &lt;200-ps CCJ; Ind; 3.3 V/5.0 V; WAFER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Differential and single-ended outputs  4 Industrial grade: -40°C to +85°C  
2 Voltage-controlled crystal oscillation  5 Electromagnetic interference reduction using Lexmark profile  
3 Integrated phase noise across 12-kHz to 20-MHz offset  6 Cycle-to-cycle jitter

---

**Products supported by Longevity Program unless noted**

<table>
<thead>
<tr>
<th></th>
<th>Concept</th>
<th>Samples</th>
<th>EOL - LTB</th>
<th>EOL - LTS</th>
</tr>
</thead>
</table>

---

115 Timing Solutions - DMIT
# Clock Buffer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High Performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2Dpx/CPx</td>
<td>Maximum Frequency: 1.5 GHz; 2-10 Outputs; LVPECL; 2.5 V/3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.11-ps Additive Jitter; Ind</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8/20-TSSOP; 8-SOIC; 32-TQFP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2Dmx/DLx</td>
<td>Maximum Frequency: 1.5 GHz; 2-10 Outputs; LVDS, CML; 2.5 V/3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.11-ps Additive Jitter; Ind</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8/20-TSSOP; 32-TQFP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY230x/EP0x</td>
<td>Maximum Frequency: 220 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Zero Delay)</td>
<td>2-9 Outputs; LVC莫斯; 2.5 V/3.3 V/5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>22-ps CCJ; Ind; Auto A+</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8/16-SOIC; 16-TSSOP; WAFER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY230xNZ/2994x</td>
<td>Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Non-Zero Delay)</td>
<td>4-18 Outputs; LVCmos</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100-ps Op-Op Skew; Ind</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5 V/3.3 V; 8-TSSOP, 16-SOIC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY23FS04/08/FP12</td>
<td>Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Zero Delay)</td>
<td>4-12 Outputs; LVCmos; Fail Safe</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>200-ps CCJ; Ind; 2.5 V/3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16/28-SSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY23S0x</td>
<td>Maximum Frequency: 133 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Zero Delay)</td>
<td>5-9 Outputs; LVCmos</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Spread Aware; 90-ps CCJ; Ind</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY7B99x (RoboClock™)</td>
<td>Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8-13 Outputs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Configurable Skew; 2.5 V/3.3 V/5.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Additive RMS phase jitter
2 Cycle-to-cycle jitter
3 Industrial grade: -40°C to +85°C
4 AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted.
# Timing Solutions Portfolio

## Programmable | High-Performance | EMI Reduction | Automotive

### Clock Synthesizers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY24940</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
</tr>
<tr>
<td>CY27410</td>
<td>4-PLL; Max Freq: 700 MHz</td>
</tr>
<tr>
<td>CY27430</td>
<td>4-PLL; Max Freq: 700 MHz</td>
</tr>
</tbody>
</table>

### Oscillators

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY24940</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
</tr>
<tr>
<td>CY2941x/2x</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
</tr>
</tbody>
</table>

### Clock Buffers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY29430</td>
<td>4-PLL; Max Freq: 700 MHz</td>
</tr>
<tr>
<td>CY27430</td>
<td>4-PLL; Max Freq: 700 MHz</td>
</tr>
</tbody>
</table>

---

1. Differential and single-ended outputs
2. Voltage-controlled crystal oscillation
3. Electromagnetic interference reduction using Lexmark profile
4. Integrated phase noise across 12-kHz to 20-MHz offset
5. Industrial grade: -40°C to +85°C
6. AEC-Q100: -40°C to +85°C
7. AEC-Q100: -40°C to +105°C
8. Additive RMS phase jitter
9. Power management options
10. Cycle-to-cycle jitter
11. Peak-to-peak period jitter
12. AEC-Q100: -40°C to +125°C

---

**Status**

- Concept
- Development
- Sampling
- Production
- EOL

**Availability**

- Q100
- Q077
- Q077
- Q120
CY27410: High-Performance 4-PLL Clock Generator

Applications
Multifunction printers, digital TVs, Blu-ray recorders, home gateways, femtocells, routers and switches

Features
- Twelve Outputs
  - Eight configurable (differential or single-ended)
  - Four single-ended
- Specifications
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0 and 10 GbE
  - Industrial temperature grade
- Additional Features
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency Select option to choose from eight pre-programmed configurations
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- RoHS-Compliant Package
  - Available in a 7 mm x 7 mm 48-pin QFN package

Collateral
Datasheet: 4-PLL High-Performance Clock Generator (CY274X)

Availability
Production: Now

Diagram:
Four-PLL Spread-Spectrum Clock Generator

1 Crystal input  2 Crystal output  3 Reference clock inputs  4 Serial port  5 Voltage input pin for VCFS  6 Frequency select inputs

Datasheet: 4-PLL High-Performance Clock Generator (CY274X)
CY2941x/2x: High-Performance 1-PLL Programmable Oscillator

Applications

- Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

Features

- Outputs
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\) and CML\(^4\) outputs
- Specifications
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): \(\sim 110\) fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Pin select and I\(^2\)C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- RoHS-Compliant Packages
  - Available in a 5 mm x 7 mm, 5 mm x 3.2 mm 8-pin LCC\(^9\) package

Collateral

Datasheet: **1-PLL High-Performance Programmable Oscillator (CY2941x/2x)**

---

\(^1\) Low-voltage positive emitter coupled logic
\(^2\) Low-voltage differential signaling
\(^3\) High-speed current steering logic
\(^4\) Current mode logic
\(^5\) The uncertainty of the clock rising and falling edge timing
\(^6\) Voltage input pin for VCFS
\(^7\) Frequency select inputs
\(^8\) I\(^2\)C input
\(^9\) Leadless ceramic chip carrier
CY29430: High-Performance 1-PLL Clock Synthesizer

**Applications**
Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

**Features**
- **Outputs**
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\), CML\(^4\) and LVCMOS outputs
- **Specifications**
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Frequency Select option to choose from four pre-programmed configurations
  - Pin select and I\(^2\)C programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- **RoHS-Compliant Package**
  - Available in a 3 mm x 3 mm 16-pin QFN\(^9\) package

**Collateral**
Datasheet: [1-PLL High-Performance Clock Synthesizer (CY29430)](#)

---

\(^1\) Low-voltage positive emitter coupled logic
\(^2\) Low-voltage differential signaling
\(^3\) High-speed current steering logic
\(^4\) Current mode logic
\(^5\) The uncertainty of the clock rising and falling edge timing
\(^6\) I\(^2\)C input
\(^7\) Voltage input pin for VCFS
\(^8\) Frequency select inputs
\(^9\) Quad flat no-leads
Cypress Roadmap: Flash Memory
NOR Flash Memory Family
NOR Flash Memory Family Decoder

Technology:  
- J = 110-nm Floating Gate (FG)
- K = 90-nm FG
- L = 65-nm FG
- M = 50-nm FG
- P = 90-nm MB
- R, S = 65-nm MB
- T = 45-nm MB

Density:  
- 008 = 8Mb
- 016 = 16Mb
- 032 = 32Mb
- 064 = 64Mb
- 128 = 128Mb
- 256 = 256Mb
- 512 = 512Mb
- 01G = 1Gb
- 02G = 2Gb
- 04G = 4Gb

Voltage:  
- D = 2.5 V
- L = 3.0 V
- S = 1.8 V

Family:  
- A = Standard ADP (Address-Data Parallel)
- C = Burst Mode ADP (Address-Data Parallel)
- F = Serial
- G = Page Mode
- H = High-Performance Serial
- J = Simultaneous Read/Write ADP (Address-Data Parallel)
- K = HyperBus™
- P = Page Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- V = Burst Mode Simultaneous Read/Write ADM (Address-Data Multiplexed)
- W = Burst Mode Simultaneous Read/Write ADP (Address-Data Parallel)
- X = Burst Mode Simultaneous Read/Write AADM (Address-Address-Data Multiplexed)

Series:  
- 25 = SPI
- 35 = SPI with Security
- 26 = HyperBus
- 36 = HyperBus with Security
- 29 = Parallel
- 70 = Stacked Die
- 28 = Octal
- 38 = Octal with Security
- 79 = Dual Quad SPI

Prefix:  
- S
## NOR Flash Memory Product Portfolio: New Products

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Sector</th>
<th>Series</th>
<th>Voltage</th>
<th>Densities</th>
<th>Lead</th>
<th>Tech</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semper™ Flash</td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S25HS-T</td>
<td>1.8 V</td>
<td>128Mb–4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S25HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HyperBus™</td>
<td>Hybrid</td>
<td>S26HS-T</td>
<td>1.8 V</td>
<td>128Mb–4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Octal</td>
<td>Hybrid</td>
<td>S28HS-T</td>
<td>1.8 V</td>
<td>128Mb–4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S28HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper Secure Flash</td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S35HS-T</td>
<td>1.8 V</td>
<td>128–512Mb</td>
<td>256Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S35HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HyperBus™</td>
<td>Hybrid</td>
<td>S36HS-T</td>
<td>1.8 V</td>
<td>128–512Mb</td>
<td>256Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S36HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Octal</td>
<td>Hybrid</td>
<td>S38HS-T</td>
<td>1.8 V</td>
<td>128–512Mb</td>
<td>256Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S38HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quad SPI</td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S25FS-S</td>
<td>1.8 V</td>
<td>64Mb–1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S25FL-S</td>
<td>3.0 V</td>
<td>128Mb–1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Uniform 4KB</td>
<td>S25FL-L</td>
<td>3.0 V</td>
<td>64–256Mb</td>
<td>-</td>
<td>65-nm FG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S79FS-S</td>
<td>1.8 V</td>
<td>256Mb–1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S79FL-S</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperFlash</td>
<td>HyperBus™</td>
<td>Hybrid</td>
<td>S26KS-S</td>
<td>1.8 V</td>
<td>128–512Mb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26KL-S</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel</td>
<td>Parallel</td>
<td>Hybrid</td>
<td>S29GL-T</td>
<td>3.0 V</td>
<td>512Mb–2Gb</td>
<td>-</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Production</th>
<th>Samples</th>
<th>Concept</th>
<th>EOL</th>
</tr>
</thead>
</table>

2020-07-13  Copyright © Infineon Technologies LLC 2020. All rights reserved.
## x8 Serial NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S28HS-T(^{1}) (1.8 V)</td>
<td>4Gb(^{2})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S28HL-T(^{1}) (3.0 V)</td>
<td>2Gb(^{2})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper™ Flash with Octal Interface</td>
<td>1Gb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm MB(^{3})</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256Mb</td>
<td>128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26HS-T(^{1}) (1.8 V)</td>
<td>4Gb(^{2})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26HL-T(^{1}) (3.0 V)</td>
<td>2Gb(^{2})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper Flash with HyperBus™ Interface</td>
<td>1Gb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm MB(^{3})</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256Mb</td>
<td>128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26KS-S (1.8 V)</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26KL-S (3.0 V)</td>
<td>256Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperFlash</td>
<td>128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65-nm MB(^{3})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S79FS-S (1.8 V)</td>
<td>1Gb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>512Mb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65-nm MB(^{3})</td>
<td>256Mb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S79FL-S (3.0 V)</td>
<td>1Gb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>512Mb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65-nm MB(^{3})</td>
<td>256Mb(^{5})</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1. JEDEC xSPI Compliant
2. Hybrid Sector
3. Stacked Die
4. 1.8 V only in production
5. S79 Series (stacked die)

---

Products supported by Longevity Program unless noted

<table>
<thead>
<tr>
<th>Concept</th>
<th>Samples</th>
<th>Production</th>
<th>EOL - LTB</th>
<th>EOL - LTS</th>
</tr>
</thead>
</table>

---

2020-07-13
## x8 Serial NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Temperature Range</th>
<th>All parts supported by Longevity Program unless noted</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual Quad SPI S79FL-S1, 2</td>
<td>65-nm MB, 3.0 V</td>
<td>* I, A, V, B</td>
</tr>
<tr>
<td>HyperFlash S26KL-S1</td>
<td>65-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>Semper™ Flash S26HL-T1</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>Semper Flash S28HL-T1</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI S79FS-S1, 2</td>
<td>65-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>HyperFlash S26KS-S1</td>
<td>65-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>Semper Flash S26HL-T1</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>Semper Flash S28HL-T1</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
</tbody>
</table>

### S79FL01GS
133 MHz/80 MHz
- I, A, V, B

### S79FL512S
133 MHz/80 MHz
- I, A, V, B, M

### S79FL256S
133 MHz/80 MHz
- I, A, V, B

### S26KL512S
-100 MHz
- I, A, V, B, M

### S26KL256S
-100 MHz
- I, A, V, B, M

### S26KL128S
-100 MHz
- I, A, V, B, M

### S26HL512T
-166 MHz
- I, A, V, B

### S26HL256T
-166 MHz
- I, A, V, B

### S26HL128T
-166 MHz
- I, A, V, B

### S26FL01GT
166 MHz/166 MHz
- I, A, V, B

### S26FL02GT
133 MHz/133 MHz
- I, A, V, B, M

### S26FL04GT
166 MHz/166 MHz
- I, A, V, B

### S26FS01GS
133 MHz/102 MHz
- I, A, V, B

### S26FS512S
133 MHz/80 MHz
- I, A, V, B

### S26FS02GT
133 MHz/80 MHz
- I, A, V, B

### S26FS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S26FS512T
200 MHz/200 MHz
- I, A, V, B, M

### S26HS01GT
200 MHz/200 MHz
- I, A, V, B

### S26HS02GT
200 MHz/200 MHz
- I, A, V, B, M

### S26HS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S26HS512T
200 MHz/200 MHz
- I, A, V, B

### S26HS525T
200 MHz/200 MHz
- I, A, V, B

### S26HS256T
200 MHz/200 MHz
- I, A, V, B

### S26HS02GT
200 MHz/200 MHz
- I, A, V, B, M

### S26HS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S26HS02GT
166 MHz/166 MHz
- I, A, V, B, M

### S26HS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S79FS01GS
133 MHz/102 MHz
- I, A, V, B

### S79FS512S
133 MHz/80 MHz
- I, A, V, B

### S79FS02GT
133 MHz/80 MHz
- I, A, V, B

### S79FS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S79FS512T
200 MHz/200 MHz
- I, A, V, B

### S79FS02GT
200 MHz/200 MHz
- I, A, V, B, M

### S79FS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S79FS512T
200 MHz/200 MHz
- I, A, V, B

### S79FS02GT
200 MHz/200 MHz
- I, A, V, B, M

### S79FS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S79FS512T
200 MHz/200 MHz
- I, A, V, B

### S79FS02GT
200 MHz/200 MHz
- I, A, V, B, M

### S79FS04GT
166 MHz/166 MHz
- I, A, V, B, M

### S79FS512T
200 MHz/200 MHz
- I, A, V, B
## x4 Serial NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S25HS-T (1.8 V)</td>
<td>4Gb&lt;sup&gt;4&lt;/sup&gt;</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S25HL-T (3.0 V)</td>
<td>2Gb&lt;sup&gt;4&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb&lt;sup&gt;4&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb&lt;sup&gt;4&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb&lt;sup&gt;4&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb&lt;sup&gt;4&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S25FS-S (1.8 V)</td>
<td>1Gb&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S25FL-S (3.0 V)</td>
<td>512Mb&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>256Mb&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb&lt;sup&gt;5&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S25FL-L (3.0 V)</td>
<td>256Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>128Mb&lt;sup&gt;6&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb&lt;sup&gt;6&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

1. Hybrid Sector  
2. VIO 1.8 V to 3.0 V  
3. Uniform Sector  
4. Stacked Sector  
5. 3.0 V only in production  
6. S70 Series (stacked die)  
7. S25FL127S & S25FL128S  
8. FS-S only
x4 Serial NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>SDR Clock/DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S25FL-L</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL-S</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL256L</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL128L</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL064L</td>
<td>108 MHz/54 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL01GS1</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL512S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL256S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S70FL01GS1</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL128S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL127S</td>
<td>108 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL02GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FL04GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL512T</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL256T</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL01GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL02GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL128T</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL127S</td>
<td>108 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL04GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HL02GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS01GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS02GT</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S70FS01GS1</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FS512S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FS256S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FS01GS1</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FS128S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25FS064S</td>
<td>133 MHz/80 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS128T</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS01GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS02GT</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS01GT</td>
<td>166 MHz/102 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
<tr>
<td>S25HS02GT</td>
<td>133 MHz/66 MHz</td>
<td>* I, A, V, B, M</td>
</tr>
</tbody>
</table>

1. Uniform Sector
2. Hybrid Sector
3. With QSPI
4. Stacked die
5. St70 series (stacked die)
6. Contact Sales

* I = Industrial: -40°C to +85°C
  A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
  V = Industrial-plus: -40°C to +105°C
  B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
  M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

2020-07-13
# Semper™ Secure Serial NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S35HS-T¹ (1.8 V)</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S35HL-T¹ (3.0 V)</td>
<td>256Mb</td>
<td>(Q421)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper Secure</td>
<td>128Mb</td>
<td>(Q322)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash with QSPI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>45-nm MB²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S36HS-T¹ (1.8 V)</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S36HL-T¹ (3.0 V)</td>
<td>256Mb</td>
<td>(Q222)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper Secure</td>
<td>128Mb</td>
<td>(Q422)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash with</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperBus™</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>45-nm MB²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S38HS-T¹ (1.8 V)</td>
<td>512Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S38HL-T¹ (3.0 V)</td>
<td>256Mb</td>
<td>(Q122)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper™ Secure</td>
<td>128Mb</td>
<td>(Q322)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash with</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Octal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>45-nm MB²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ JEDEC xSPI Compliant
² Hybrid Sector

Products supported by Longevity Program unless noted.

- Concept
- Samples
- Production
- EOL - LTB
- EOL - LTS

2020-07-13
## Semper™ Secure Serial NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>SDR Clock/DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semper Secure Flash</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S35HL-T²</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S36HL-T²</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S38HL-T²</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>S35HS-T²</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>S36HS-T²</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>S38HS-T²</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
</tbody>
</table>

### Note
- All parts supported by Longevity Program unless noted.

1. With QSPI
2. Hybrid Sector
3. HyperBus Interface (xSPI Profile 2.0)
4. Octal Interface (xSPI Profile 1.0)

### Parameters
- **Density (Name)**
- **Temperature Range**
- **Product Family Number**
- **SDR Clock/DDR Clock**

### Additional Details
- **I** = Industrial: -40°C to +85°C
- **A** = Automotive, AEC-Q100 Grade 3: -40°C to +125°C
- **V** = Industrial-plus: -40°C to +105°C
- **B** = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- **M** = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

### Status
- **Concept**
- **Development**
- **Sampling**
- **Production**

### Availability
- **EOL (Last-Time-Ship)**

2020-07-13

Copyright © Infineon Technologies LLC 2020. All rights reserved.
# Parallel NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod)</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(EOL)</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S29GL-T³ (3.0 V)</td>
<td>45-nm MB</td>
<td>2Gb³</td>
<td>1Gb</td>
<td>512Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29GL-S³ (3.0 V)</td>
<td>65-nm MB</td>
<td>2Gb³</td>
<td>1Gb</td>
<td>512Mb</td>
<td>256Mb</td>
<td>128Mb</td>
<td></td>
</tr>
<tr>
<td>S29GL-P³ (3.0 V)</td>
<td>90-nm MB</td>
<td>256Mb</td>
<td>128Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29GL-N³ (3.0 V)</td>
<td>110-nm MB</td>
<td>64Mb</td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29PL-J¹,² (3.0 V)</td>
<td>110-nm FG</td>
<td>128Mb</td>
<td>64Mb</td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29JL-J² (3.0 V)</td>
<td>110-nm FG</td>
<td>64Mb</td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29AL-J (3.0 V)</td>
<td>110-nm FG</td>
<td>16Mb</td>
<td>8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29AS-J (1.8 V)</td>
<td>110-nm FG</td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Supports Page Mode
2 Supports simultaneous read/write operation
3 S70 series (stacked die)
## Parallel NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>S29AS-J</th>
<th>S29AL-J</th>
<th>S29JL-J 1</th>
<th>S29PL-J 1, 2</th>
<th>S29GL-N 2</th>
<th>S29GL-P 2</th>
<th>S29GL-S 2</th>
<th>S29GL-T 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>110-nm FG, 1.8 V</td>
<td>110-nm FG, 3.0 V</td>
<td>110-nm FG, 3.0 V</td>
<td>110-nm MB, 3.0 V</td>
<td>90-nm MB, 3.0 V</td>
<td>65-nm MB, 3.0 V</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
</tbody>
</table>

### All parts supported by Longevity Program unless noted

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>70 ns/20 ns</td>
<td>55 ns/20 ns</td>
<td>55 ns/20 ns</td>
<td>90 ns/25 ns</td>
<td>90 ns/25 ns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>55 ns/20 ns</td>
<td>55 ns/20 ns</td>
<td>55 ns/20 ns</td>
<td>55 ns/20 ns</td>
<td>90 ns/25 ns</td>
</tr>
</tbody>
</table>

### Status

- **Concept**: QQYY
- **Development**: QQYY
- **Sampling**: QQYY
- **Production**: QQYY
- **Availability**: N/A
- **EOL (Last-Time-Shipping)**: N/A

### Notes

1 Supports simultaneous read/write operation
2 Supports Page Mode
3 S70 series (stacked die)

* I = Industrial: -40°C to +85°C
* V = Industrial-plus: -40°C to +105°C
* N = Extended: -40°C to +125°C

A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
## Burst NOR Flash Memory Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod)</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S29WS-P1 (1.8 V) 90-nm MB</td>
<td>512Mb</td>
<td>128Mb</td>
<td>[EOL]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29VS-R3 (1.8 V) 65-nm MB</td>
<td>256Mb</td>
<td>128Mb</td>
<td>[Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29VS-R3 (1.8 V) 65-nm MB</td>
<td>64Mb</td>
<td></td>
<td>[Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29XS-R3 (1.8 V) 65-nm MB</td>
<td>256Mb</td>
<td></td>
<td>[Q320]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29CD-J1 (1.8 V) 110-nm MB</td>
<td>32Mb</td>
<td>16Mb</td>
<td>[EOL]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29CL-J1 (3.0 V) 110-nm MB</td>
<td>32Mb</td>
<td>16Mb</td>
<td>[EOL]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Address Data Parallel (ADP) Burst
2 Address high, Address low, Data Multiplex (AADM) Burst
3 Address Data Multiplex (ADM) Burst

Products supported by Longevity Program unless noted

- **Samples**
- **Concept**
- **Production**
- **EOL - LTB**
- **EOL - LTS**
## Burst NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial Access/SDR Clock</th>
<th>Temp Range</th>
<th>Access Data Parallel (ADP) Burst</th>
<th>Address high, Address low, Data Multiplex (AADM) Burst</th>
<th>Address Data Multiplex (ADM) Burst</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29CL-J^1</td>
<td>110-nm FG, 3.0 V</td>
<td>≥256 Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>64–128 Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤32 Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29CD-J^1</td>
<td>110-nm FG, 2.5 V</td>
<td>65-nm MB</td>
<td>54 ns/75 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29XS-R^2</td>
<td>65-nm MB, 1.8 V</td>
<td></td>
<td>54 ns/68 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29VS-R^3</td>
<td>65-nm MB, 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29WS-P^1</td>
<td>90-nm MB, 1.8 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* W = Wireless: -25°C to +85°C  
I = Industrial: -40°C to +85°C  
A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C  
N = Extended: -40°C to +125°C  
M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C  
T = Automotive, AEC-Q100 Grade 0: -40°C to +150°C  

---

1. Product Family Number  
2. Initial Access/SDR Clock  
3. Temp Range  
4. Address Data Parallel (ADP) Burst  
5. Address high, Address low, Data Multiplex (AADM) Burst  
6. Address Data Multiplex (ADM) Burst

© Infineon Technologies LLC 2020. All rights reserved.
## KGD/KGW NOR Flash Memory Portfolio

<table>
<thead>
<tr>
<th>HyperFlash 3.0 V</th>
<th>HyperFlash 1.8 V</th>
<th>Quad SPI 3.0 V</th>
<th>Quad SPI 1.8 V</th>
<th>Parallel 3.0 V</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Product Family Number</strong></td>
<td><strong>Initial Access/DDR Clock</strong></td>
<td><strong>Temperature Range</strong></td>
<td><strong>Product Family Number</strong></td>
<td><strong>SDR Clock/DDR Clock</strong></td>
</tr>
<tr>
<td>S26KS125S</td>
<td>96 ns/166 MHz</td>
<td>* I, V</td>
<td>S25FL512S</td>
<td>133 MHz/80 MHz</td>
</tr>
<tr>
<td>S26KL256S</td>
<td>96 ns/100 MHz</td>
<td>* I, V</td>
<td>S25F5256L</td>
<td>133 MHz/66 MHz</td>
</tr>
<tr>
<td>S26KL512S</td>
<td>96 ns/100 MHz</td>
<td>* I, V</td>
<td>S25FS256S</td>
<td>80 MHz</td>
</tr>
<tr>
<td>S25FL128S</td>
<td>96 ns/166 MHz</td>
<td>* I, V</td>
<td>S25FS256T</td>
<td>104 MHz</td>
</tr>
<tr>
<td>S25FS064S</td>
<td>108 MHz/54 MHz</td>
<td>* I, V</td>
<td>S29AL016J</td>
<td>55 ns/-</td>
</tr>
<tr>
<td>S25FS064S</td>
<td>136 MHz/80 MHz</td>
<td>* I, V, N</td>
<td>S29AL008J</td>
<td>55 ns/-</td>
</tr>
</tbody>
</table>

- **≥256 Mb**
- **64–128 Mb**
- **≤32 Mb**

* C = Commercial: 0°C to +70°C
* I = Industrial: -40°C to +85°C
* V = Industrial-plus: -40°C to +105°C
* N = Extended: -40°C to +125°C

* Contact Sales for KGD datasheets

---

1. Contact Sales for KGD datasheets
Flash and RAM Memory MCP
Flash and RAM Memory MCP Decoder

- **RAM Density:**
  - A = 16Mb
  - B = 32Mb
  - C = 64Mb
  - D = 128Mb
  - E = 256Mb

- **Flash Technology:**
  - N = 110-nm MirrorBit (MB)
  - P = 90-nm MB
  - R, S = 65-nm MB
  - T = 45-nm MB

- **Flash Density:**
  - 032 = 32Mb
  - 128 = 128Mb
  - 512 = 512Mb
  - 064 = 64Mb
  - 256 = 256Mb
  - 01G = 1Gb

- **Voltage:**
  - L = 3.0 V
  - S = 1.8 V

- **Family:**
  - G = Page Mode
  - H = High-Performance Serial
  - K = HyperFlash
  - V = Burst Mode Simultaneous Read/Write Address-Data Multiplexed (ADM)
  - W = Burst Mode Simultaneous Read/Write Address-Data Parallel (ADP)
  - X = Burst Mode Simultaneous Read/Write Address-Address-Data Multiplexed (AADM)

- **Series:**
  - 71, 98 = NOR Flash + pSRAM
  - 72 = NOR Flash + DRAM
  - 76 = HyperBus Interface (xSPI Profile 2.0) NOR Flash + HyperRAM™
  - 78 = Octal Interface (xSPI Profile 1.0) NOR Flash + HyperRAM

- **Prefix:**
  - S
# Serial Flash and RAM Memory MCP Roadmap

<table>
<thead>
<tr>
<th>Product Family Flash/RAM</th>
<th>Flash/RAM Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S78HS-T (1.8 V)&lt;sup&gt;1&lt;/sup&gt; 45-nm Semper™ Flash/HyperRAM™</td>
<td>1Gb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S76HS-T (1.8 V)&lt;sup&gt;2&lt;/sup&gt; 45-nm Semper Flash/HyperRAM</td>
<td>1Gb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb (Q221)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71KS-S (1.8 V)&lt;sup&gt;3&lt;/sup&gt; 65-nm HyperFlash/HyperRAM</td>
<td>512Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S78HL-T (3.0 V)&lt;sup&gt;1&lt;/sup&gt; 45-nm Semper Flash/HyperRAM</td>
<td>1Gb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S76HL-T (3.0 V)&lt;sup&gt;2&lt;/sup&gt; 45-nm Semper Flash/HyperRAM</td>
<td>1Gb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb (Q421)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb (Q122)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71KL-S (3.0 V)&lt;sup&gt;3&lt;/sup&gt; 65-nm HyperFlash/HyperRAM</td>
<td>512Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb/64Mb (TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Octal Interface (xSPI Profile 1.0)
2 HyperBus Interface (xSPI Profile 2.0)
3 HyperBus Interface

Products supported by Longevity Program unless noted.

- **Concept**
- **Production**
- **EOL - LTB**
- **EOL - LTS**

Copyright © Infineon Technologies LLC 2020. All rights reserved.
Parallel Flash and RAM Memory MCP Roadmap

<table>
<thead>
<tr>
<th>Product Family Flash/RAM</th>
<th>Flash/RAM Density</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S98GL-N (3.0 V) 110-nm MB/pSRAM</td>
<td>64Mb/32Mb [Q320]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72XS-R (1.8 V) 65-nm MB/DRAM</td>
<td>256Mb/256Mb [Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72VS-R (1.8 V) 65-nm MB/DRAM</td>
<td>256Mb/256Mb [Q121]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS-R (1.8 V) 65-nm MB/pSRAM</td>
<td>256Mb/128Mb [Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS-R (1.8 V) 65-nm MB/pSRAM</td>
<td>256Mb/64Mb [Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS-R (1.8 V) 65-nm MB/pSRAM</td>
<td>128Mb/32Mb [Q321]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS-R (1.8 V) 65-nm MB/pSRAM</td>
<td>64Mb/32Mb [Q320]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71WS-P (1.8 V) 90-nm MB/pSRAM</td>
<td>256Mb/64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Products supported by Longevity Program unless noted.

Concept - Production - EOL - LTB - EOL - LTS
# Serial Flash and RAM Memory MCP Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>RAM Density / DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S71KL-S</td>
<td>65-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S76HL-T</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S78HL-T</td>
<td>45-nm MB, 3.0 V</td>
<td></td>
</tr>
<tr>
<td>S71KS-S</td>
<td>65-nm MB, 1.8 V</td>
<td></td>
</tr>
<tr>
<td>S76HS-T</td>
<td>45-nm MB, 1.8 V</td>
<td></td>
</tr>
</tbody>
</table>

## 256Mb

<table>
<thead>
<tr>
<th>Q121</th>
<th>Q421</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HL01GD2³</td>
<td>128Mb³ / 133MHz</td>
</tr>
<tr>
<td>I, A, V, B</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q021</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HS01GD2³</td>
</tr>
<tr>
<td>I, A, V, B</td>
</tr>
</tbody>
</table>

## 128Mb

<table>
<thead>
<tr>
<th>Q321</th>
<th>Q122</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HL512TC2³</td>
<td>64Mb³ / 166MHz</td>
</tr>
<tr>
<td>* I, A, V, B</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q221</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HS512TC³</td>
</tr>
<tr>
<td>* I, A, V, B</td>
</tr>
</tbody>
</table>

## 64–128Mb

<table>
<thead>
<tr>
<th>Q420</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HL01GD2³</td>
</tr>
<tr>
<td>* I, A, V, B</td>
</tr>
</tbody>
</table>

## Additional Information

1. HyperFlash
2. HyperBus Interface (xSPI Profile 2.0)
3. Octal Interface (xSPI Profile 1.0)

* I = Industrial: -40°C to +85°C
A = Automotive, AEC-Q100 Grade 3: -40°C to +105°C
V = Industrial-plus: -40°C to +105°C
B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C

---

2020-07-13

Copyright © Infineon Technologies LLC 2020. All rights reserved.
## Parallel Flash and RAM Memory MCP Portfolio

<table>
<thead>
<tr>
<th>Product Family</th>
<th>RAM Density</th>
<th>Temperature Range</th>
<th>Status</th>
<th>Availability</th>
<th>EOL (Last-Time-Ship)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S71WS-P¹</td>
<td>90-nm MB, 1.8 V</td>
<td>All parts supported by Longevity Program unless noted</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS-R²</td>
<td>65-nm MB, 1.8 V</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72VS-R³</td>
<td>65-nm MB, 1.8 V</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72XS-R³</td>
<td>65-nm MB, 1.8 V</td>
<td>* W, I</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S98GL-N⁴</td>
<td>110-nm MB, 3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS256RD</td>
<td>128Mb</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS256RC</td>
<td>64Mb</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS128RB</td>
<td>32Mb</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71VS064RB</td>
<td>32Mb</td>
<td>* W</td>
<td>Q320</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71WS256PC</td>
<td>64Mb</td>
<td>* W</td>
<td>Q321</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72VS256RE</td>
<td>256Mb</td>
<td>*</td>
<td>Q121</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72VS128RE</td>
<td>128Mb</td>
<td>*</td>
<td>Q121</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S72VS512RE</td>
<td>512Mb</td>
<td>*</td>
<td>Q121</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S98GL064NB</td>
<td>32Mb</td>
<td>*</td>
<td>Q320</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ Address Data Parallel (ADP) Burst
² Address Data Multiplex (ADM) Burst
³ Address High, Address Low, Data Multiplex (AADM) Burst
⁴ Parallel, Page Mode
⁵ DRAM Version 2
⁶ DRAM Version 1

* W = Wireless: -25°C to +85°C
I = Industrial: -40°C to +85°C

2020-07-13

Copyright © Infineon Technologies LLC 2020. All rights reserved.
Package Offerings
## x8 1.8V Serial Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>SOIC-16 300 mil</th>
<th>BGA24 8 x 8 mm/5 x 5 Ball</th>
<th>BGA24 8 x 6 mm/5 x 5 Ball</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semper™ Flash</strong></td>
<td>HyperBus™</td>
<td>HS-T¹</td>
<td>256Mb</td>
<td>S28HS256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S28HS512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S28HS01GT</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S28HS02GT</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S28HS04GT</td>
<td></td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td><strong>HyperFlash</strong></td>
<td>KS-S³</td>
<td>256Mb</td>
<td>S26HS256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26HS512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S26HS01GT</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S26HS02GT</td>
<td></td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S26HS04GT</td>
<td></td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td><strong>Quad SPI</strong></td>
<td>QSPI</td>
<td>FS-S Dual Quad</td>
<td>256Mb</td>
<td>S79FS256S</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S79FS512S</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S79FS01GS</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

¹ Octal Interface (xSPI Profile 1.0)
² HyperBus Interface (xSPI Profile 2.0)
³ HyperBus Interface

CF = Contact Factory
UD = Under Development
# x8 3.0V Serial Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>SOIC-16 300 mil</th>
<th>BGA24 8 x 8 mm/5 x 5 Ball</th>
<th>BGA24 8 x 6 mm/5 x 5 Ball</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semper™ Flash</strong></td>
<td>HyperBus™</td>
<td>HL-T¹</td>
<td>256Mb</td>
<td>S28HL256T</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S28HL512T</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S28HL01GT</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S28HL02GT</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S28HL04GT</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td><strong>HyperFlash</strong></td>
<td></td>
<td>HL-T²</td>
<td>256Mb</td>
<td>S26HL256T</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26HL512T</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S26HL01GT</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S26HL02GT</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S26HL04GT</td>
<td>CF</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td><strong>Quad SPI</strong></td>
<td>QSPI</td>
<td>KL-S³</td>
<td>128Mb</td>
<td>S26KL128S</td>
<td>✓</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>256Mb</td>
<td>S26KL256S</td>
<td>✓</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26KL512S</td>
<td>✓</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td><strong>Quad SPI</strong></td>
<td>QSPI</td>
<td>FL-S</td>
<td>256Mb</td>
<td>S79FL256S</td>
<td>✓</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dual Quad</td>
<td>512Mb</td>
<td>S79FL512S</td>
<td>✓</td>
<td></td>
<td></td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S79FL01GS</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
</tr>
</tbody>
</table>

¹ Octal Interface (xSPI Profile 1.0)
² HyperBus Interface (xSPI Profile 2.0)
³ HyperBus Interface

CF = Contact Factory
UD = Under Development
<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>SOIC-8 208 mil</th>
<th>SOIC-16 300 mil</th>
<th>WSON 4 x 4 mm</th>
<th>WSON 6 x 5 mm</th>
<th>WSON 8 x 6 mm</th>
<th>BGA24 8 x 8 mm 5 x 5 Ball</th>
<th>BGA24 8 x 6 mm 5 x 5 Ball</th>
<th>BGA24 8 x 6 mm 4 x 6 Ball</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semper™ Flash</td>
<td>HS-T</td>
<td>256Mb</td>
<td>S25HS256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25HS512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S25HS01GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2Gb</td>
<td>S25HS02GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4Gb</td>
<td>S25HS04GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>HL-T</td>
<td>256Mb</td>
<td>S25HL256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25HL512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S25HL01GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2Gb</td>
<td>S25HL02GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4Gb</td>
<td>S25HL04GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td>Quad SPI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QSPI</td>
<td>FS-S</td>
<td>64Mb</td>
<td>S25FS064S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FS128S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FS256S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25FS512S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S70FS01GS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>FL-S</td>
<td>128Mb</td>
<td>S25FL127S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL128S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FL256S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25FL512S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S70FL01GS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>FL-L</td>
<td>64Mb</td>
<td>S25FL064L</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL128L</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FL256L</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
</tbody>
</table>

CF = Contact Factory  
UD = Under Development
## Parallel NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>Device</th>
<th>48-Ball FBGA (0.8-mm pitch)</th>
<th>48-Ball FBGA (0.5-mm pitch)</th>
<th>56-Ball BGA (0.8-mm pitch)</th>
<th>64-Ball BGA (0.8-mm pitch)</th>
<th>64-Ball Fortified BGA (1.0-mm pitch)</th>
<th>48-Pin TSOP</th>
<th>56-Pin TSOP</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL-T</td>
<td>512Mb</td>
<td>S29GL512T</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>S29GL01GT</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Gb</td>
<td>S70GL02GT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GL-S</td>
<td>64Mb</td>
<td>S29GL064S</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29GL128S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29GL256S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>S29GL512S</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>S29GL01GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Gb</td>
<td>S70GL02GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GL-P</td>
<td>128Mb</td>
<td>S29GL128P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29GL256P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GL-N</td>
<td>32Mb</td>
<td>S29GL032N</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29GL064N</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PL-J</td>
<td>32Mb</td>
<td>S29PL032J</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29PL064J</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29PL127J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JL-J</td>
<td>32Mb</td>
<td>S29JL032J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29JL064J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AL-J</td>
<td>8Mb</td>
<td>S29AL008J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td>S29AL016J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AS-J</td>
<td>16Mb</td>
<td>S29AS016J</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Burst NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>Device</th>
<th>44-Ball FBGA (0.5-mm pitch)</th>
<th>64-Ball BGA (0.5-mm pitch)</th>
<th>84-Ball Fortified BGA (0.8-mm pitch)</th>
<th>80-Ball FBGA (1.0-mm pitch)</th>
<th>80-Pin PQFP</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>WS-P</td>
<td>128Mb</td>
<td>S29WS128P</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29WS256P</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>S29WS512P</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VS-R</td>
<td>64Mb</td>
<td>S29VS064R</td>
<td>EOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29VS128R</td>
<td>EOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29VS256R</td>
<td>EOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XS-R</td>
<td>256Mb</td>
<td>S29XS256R</td>
<td>EOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD-J</td>
<td>16Mb</td>
<td>S29CD016J</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td>S29CD032J</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL-J</td>
<td>16Mb</td>
<td>S29CL016J</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td>S29CL032J</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Flash and RAM Memory MCP Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Flash Density</th>
<th>RAM Density</th>
<th>BGA24 8 x 6 mm 5 x 5 Ball</th>
<th>BGA24 8 x 8 mm 5 x 5 Ball</th>
<th>56-Ball Very Thin FBGA (0.5-mm pitch)</th>
<th>56-Ball FBGA (0.8-mm pitch)</th>
<th>84-Ball FBGA (0.8-mm pitch)</th>
<th>133-Ball FBGA (0.5-mm pitch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HS-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S76HL-T</td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S78HS-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S78HL-T</td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S71KS-S</td>
<td>128Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S71KL-S</td>
<td>128Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S98GL-N</td>
<td>64Mb</td>
<td>32Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S72XS-R</td>
<td>256Mb</td>
<td>256Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S72VS-R</td>
<td>256Mb</td>
<td>256Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S71VS-R</td>
<td>256Mb</td>
<td>128Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>64Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>64Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>32Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>32Mb</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
<tr>
<td>S71WS-P</td>
<td>256Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>✓</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
<td>EOL</td>
</tr>
</tbody>
</table>

CF = Contact Factory
UD = Under Development

EOL = End of Life
Military Memory Portfolio
# Military Memory Portfolio

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Product Code</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Async SRAM</td>
<td>CY7C41xKV13</td>
<td>144Mb, 1.8 V, 250 MHz, x18x36, Burst 2/4, M</td>
</tr>
<tr>
<td>Sync SRAM</td>
<td>CYPT62xKV18</td>
<td>144Mb, 1.8 V, 250 MHz, x18x36, Burst 2/4, M</td>
</tr>
<tr>
<td>Nonvolatile SRAM</td>
<td>CYPT154xAV18</td>
<td>72Mb, 1.8 V, 250 MHz, x18x36, Burst 2/4, M</td>
</tr>
<tr>
<td>F-RAM™</td>
<td>CY7C144/6xK</td>
<td>36Mb, 133-250 MHz, 2.5 V/3.3 V x18x36, M</td>
</tr>
<tr>
<td></td>
<td>CY7C137/8xK</td>
<td>18Mb, 100-250 MHz, 2.5 V/3.3 V x18x36, M</td>
</tr>
<tr>
<td></td>
<td>CY7C136xK</td>
<td>9Mb, 100-250 MHz, 2.5 V/3.3 V x18x36, M</td>
</tr>
<tr>
<td>NOR Flash</td>
<td>S70/7FL-S</td>
<td>1Gb, 1.8-3.0 V, 25 ns/45 ns x8x16x32, M, RTC</td>
</tr>
<tr>
<td></td>
<td>S29GL-S</td>
<td>128Mb/256Mb, 3.0 V, 133-MHz QSPI, Auto E, M</td>
</tr>
<tr>
<td></td>
<td>S29FL-S</td>
<td>512Mb, 3.0 V, 133-MHz QSPI, Auto E, M</td>
</tr>
<tr>
<td></td>
<td>S29GL-S</td>
<td>128Mb/256Mb, 3.0 V, 130ns, x16, Auto E, M</td>
</tr>
<tr>
<td></td>
<td>S29GL-S</td>
<td>64Mb, 3.0 V, 130 ns/15 ns, x16, Auto E, M</td>
</tr>
</tbody>
</table>

1 Error-correcting code  
2 No Bus Latency  
3 Quad Data Rate  
4 Military Temperature: -55°C to +125°C  
5 AEC-Q100 -40°C to +125°C  
6 Real-time clock  
7 Qualified Manufacturers List Level Q, per MIL-PRF-38535  
8 Military Temperature: -55°C to +125°C
256Kb/1Mb Military nvSRAM

**Applications**
Military communication and real-time controls, avionics real-time controls and high-reliability data logging

**Features**
- Fast Nonvolatile Memory
  - Access time 35 ns
  - Available in parallel interface for 256Kb and 1Mb densities
  - Unlimited read/write endurance
  - One million store cycles on power fail
- Specifications
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- Packages: Ceramic 32-pin DIP

**Collateral**
- Datasheets: STK14C88C, STK14CA8C
- DLAM\(^3\) Datasheets: 5962-18211, 5962-18212

**Availability**
- Production: Now

---

\(^1\) External capacitor connection
\(^2\) Hardware STORE busy
\(^3\) Defense Logistics Agency Land and Maritime (DLAM)
72Mb QDR®-II+ SRAM

Applications
Payload processing and reconfigurable computing platforms

Features
- High Performance Memory
  - Maximum frequency of operation/throughput: 250 MHz/36 Gbps
  - Two independent unidirectional data ports for read and write enable concurrent transactions
  - Maximum throughput with double data rate (DDR) data ports
  - Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
  - Bit-interleaving to eliminate multi-bit errors
  - I/O signaling standards: 1.5–1.8 V (HSTL)
- Specifications
  - Burst sizes: 2 or 4
  - Bus-width configurations: x18 or x36
  - Military temperature grade: -55°C to +125°C
- Controllers available for Altera/Xilinx/Microsemi FPGAs
- Package: 165-pin CCGA

Collateral
Datasheets: CYPT1542AV18/CYPT1544AV18
CYPT1543AV18/CYPT1545AV18

Availability
Production: Now

1 Quad Data Rate: Four data transfers per clock cycle
2 Ceramic column grid array package
QDR®-IV SRAM

**Applications**
Switches and routers, high-performance computing, test equipment, military and aerospace systems

**Features**
- **Highest Performance Memory**
  - Available in two options: High Performance (RTR 1334 MT/s) and Extreme Performance (RTR 2132 MT/s)
  - Two independent, bidirectional double data rate (DDR) data ports
  - Error-correcting code (ECC) to detect and correct single-bit errors (<0.01 FIT/Mb²)
  - On-die termination (ODT) to reduce board complexity
  - De-skew training³ to improve signal-capture timing
- **Specifications**
  - I/O Levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD⁴)
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **RoHS²-Compliant Package**
- **Package**: 361-ball flip-chip ball grid array (FCBGA)

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>Maximum Frequency</th>
<th>RTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDR-IV HP</td>
<td>72Mb</td>
<td>CY7C40x1KV13/CY7C41x1KV13</td>
<td>667 MHz</td>
<td>1,334 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-IV XP</td>
<td>72Mb</td>
<td>CY7C40x2KV13/CY7C41x2KV13</td>
<td>1,066 MHz</td>
<td>2,132 MT/s</td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Collateral**

Datasheets: CY7C4121KV13/CY7C4141KV13

**Availability**

Production: Now

---

1. Two data transfers per clock cycle
2. The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
3. An iterative algorithm for assessing and eliminating the skew (differences in arrival times) between data signals
4. Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up
**Synchronous SRAM with On-Chip ECC**

**Applications**
- Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

**Features**
- **New Features**
  - Available in two modes: Pipeline and Flow-Through
  - SCD and DCD deselect options
  - Error-correcting code (ECC) to detect and correct single-bit errors
- **Specifications**
  - Voltage options: 2.5 V and 3.3 V
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages:** 165-ball BGA (w/ and w/o leaded balls) and 100-pin TQFP

**Collateral**
- Datasheets: CY7C135XKV33/CY7C136XKV33
  CY7C137XKV33/CY7C138XKV33
  CY7C144XKV33/CY7C146XKV33

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb³</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with ECC</td>
<td>9Mb</td>
<td>CY7C1360/2K</td>
<td>250MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Pipeline</td>
<td>18Mb</td>
<td>CY7C1370/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync with ECC</td>
<td>9Mb</td>
<td>CY7C1361/3K</td>
<td>133MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Flow-Through</td>
<td>18Mb</td>
<td>CY7C1371/3K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync with ECC</td>
<td>9Mb</td>
<td>CY7C1440/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flow-Through</td>
<td>18Mb</td>
<td>CY7C1441/3K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
2 Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
3 The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data

**Availability**
- **Production:** Now
Fast SRAM Family with PowerSnooze

Applications
Programmable logic controller, handheld devices, multifunction printers, computation servers and automotive

Features
- Error Detection and Correction
  - Error-correcting code (ECC) logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- Specifications
  - Access time: 10 ns
  - Deep-sleep current: 15 µA for 4Mb
  - Bus-width configurations: x8, x16, and x32
  - Industrial and automotive temperature grades
  - Military temperature grade: -55°C to +125°C
- Packages: 48-ball BGA (w/ and w/o leaded balls)

Collateral
Datasheets: CY7S1049G/CY7C1049G
CY7S1051H/CY7C1051H
CY7S1061G/CY7C1061G

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>10 ns</td>
<td>15 µA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY7S105x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
</tbody>
</table>

Fast SRAM with PowerSnooze

<table>
<thead>
<tr>
<th>CE</th>
<th>DS</th>
<th>OE</th>
<th>WE</th>
<th>BHE</th>
<th>BLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC Encoder</td>
<td>I/O Mux</td>
<td>SRAM Array</td>
<td>Power Management Block (enables PowerSnooze)</td>
<td>Control Logic</td>
<td></td>
</tr>
</tbody>
</table>

Availability

Production: Now

Footnote: 1 A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode
16Mb Parallel nvSRAM

**Applications**

- Industrial automation, programmable logic controllers, gaming machines, industrial data logging, telecom equipment, networking and storage

**Features**

- **Fast Nonvolatile Memory**
  - Access time (25 ns)
  - Optional real-time clock (RTC) functionality
  - Available in parallel and open NAND Flash Interface (ONFI) Version 1.0 interfaces
  - Unlimited read/write endurance
  - One million store cycles on power fail

- **Specifications**
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C

- **Packages**: 44-pin TSOP, 54-pin TSOP, 165-ball BGA (w/ and w/o leaded balls)

**Collateral**

- Datasheet: [CY14X116L/CY14X116N/CY14X116S](#)

**Availability**

- **Sampling**: Now
- **Production**: Contact Sales

---

1 Crystal connection input
2 Crystal connection output
3 Interrupt output/calibration/square wave
4 External capacitor connection
5 Hardware STORE busy

---

156 MILITARY MEMORY – HRP
2Mb Military SPI F-RAM

Applications
Multifunction printers, industrial controls and automation, medical wearables, test and measurement equipment, smart meters, aerospace and defense applications, missiles and launchers

Features
- Ultra-Low Power Memory
  - 40-MHz SPI interface
  - 100-trillion read/write cycle endurance
- Specifications
  - Operating voltage range: 2.0–3.6 V
  - Low (20-µA) sleep current at +125°C
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- Packages: 8-pin TDFN and 8-pin SOIC

Datasheet: CY15B102Q

Availability
Production: Now
**Applications**

- Military systems boot memory
- Avionics boot memory

**Features**

- **High-Reliability Boot Flash Memory**
  - 100 program\(^1\)/sector erase\(^2\) endurance cycles\(^3\) at +125°C
  - >10 years data retention at +125°C

- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Initial access time: 120 ns
  - Page access time: 15 ns
  - Program time (512B): 0.4 ms (typical)
  - Sector erase time (128KB): 410 ms (typical)
  - Military temperature grade: -55°C to +125°C

- **Packages**: 64-ball fortified\(^4\) BGA (9 x 9 mm and 13 x 11 mm, w/ and w/o leaded balls)

**Collateral**

**Datasheet**: [S29GLXXXS](#) (128M/256M/512M/1G)

**Availability**

- **Samples**: Now
- **Production**: Now (128Mb/256Mb/512Mb) / Q2’20 (1Gb/2Gb) / Q3’20 (64Mb)

---

1. The operation required to change a NOR Flash memory cell state from “1” to “0”
2. The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
3. The number of times a NOR Flash memory sector can be programmed or erased before it wears out
4. Fortified BGA supports a 1-mm ball pitch
5. Write protect input
6. Ready/busy output
128Mb/256Mb/512Mb/1Gb SPI NOR Flash

**Applications**
- Military systems boot memory
- Avionics boot memory

**Features**
- **High-Reliability Boot Flash Memory**
  - 100 program\(^1\)/sector erase\(^2\) endurance cycles\(^3\) at +125°C
  - >10 years data retention at +125°C
- **Specifications**
  - Operating voltage range: 2.7–3.6 V
  - Single data rate (SDR)\(^4\) clock rate: 104-MHz quad input/output (QIO)\(^5\)
  - Double data rate (DDR)\(^6\) clock rate: 80-MHz QIO
  - Program time (512B): 0.340 ms (typical)
  - Sector erase time (256KB): 520 ms (typical)
  - Military temperature grade: -55°C to +125°C
- **Packages**: 24-ball BGA (6 x 8 mm, w/ and w/o leaded balls)

**Datasheets**: S25FL512S (512Mb), S25FL128/256S (128Mb/256Mb)

**Availability**
- **Sampling**: Now
- **Production**: Now

---

\(^1\) The operation required to change a NOR Flash memory cell state from “1” to “0”
\(^2\) The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously
\(^3\) The number of times a NOR Flash memory sector can be programmed/erased before it wears out
\(^4\) A mode of data transfer in which data is transferred once per clock cycle
\(^5\) An interface that transfers addresses or data on four I/O’s simultaneously
\(^6\) A mode of data transfer in which data is transferred twice per clock cycle
\(^7\) Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
\(^8\) RESET# is an optional signal available on 16-pin SOIC and BGA packages
Aerospace Memory Portfolio
# Aerospace Memory Portfolio

Radiation Hardened | Latch-up Immune | QML-V\(^1\) Certified

<table>
<thead>
<tr>
<th>Fast Async SRAM</th>
<th>Sync SRAM</th>
<th>FRAM</th>
<th>NOR Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-ECC(^2)</td>
<td>ECC(^2)</td>
<td>QDR(^\text{®}-)II+/IV</td>
<td>Serial/Parallel I/O</td>
</tr>
</tbody>
</table>

## 256Mb-1Gb

- **CYRS274x**
  - 268Mb; 1.8 V; 250 MHz
  - x18, x36; Burst 2,4

## 16Mb-144Mb

- **CYRS4141x**
  - 144Mb; 1.2 V; 667 MHz
  - x18, x36; Burst 2

- **CYRS264x**
  - 144Mb; 1.8 V; 250 MHz
  - x18, x36; Burst 2,4

## 2Mb-4Mb

- **CYRS104x**
  - 4Mb; 3.3 V
  - 10 ns; x8

- **CYRS154x**
  - 72Mb; 1.8 V; 250 MHz
  - x18, x36; Burst 2,4

## NOR Flash

- **RH CYRS17B012**
  - 512Mb; 3.0/1.8 V
  - SDR QSPI; 133MHz

- **RT CYRS16B256**
  - 256Mb; 3.0 V
  - SDR QSPI; 133MHz

- **RH CYRS17B01G**
  - 1Gb; 3.0/1.8 V
  - SDR Dual QSPI; 133MHz

---

\(^1\) Qualified Manufacturers List Level V, per military specification MIL-PRF-38535

\(^2\) Error-correcting code

---

161 AEROSPACE MEMORY – HRP
72Mb QDR®-II+ SRAM with RadStop™

Applications
Payload processing and reconfigurable computing platforms

Features
- Maximum frequency of operation/throughput: 250 MHz/36 Gbps
- Burst sizes: 2, 4
- Bus-width configurations: x18, x36
- Military temperature grade: −55°C to +125°C
- Two independent unidirectional data ports for read/write enable concurrent transactions
- Maximum throughput with double data rate (DDR) data ports
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Bit-interleaving to eliminate multi-bit errors
- I/O signaling standards: 1.5 –1.8 V (HSTL)
- Controller available for Xilinx and Microsemi FPGAs
- Total ionizing dose: 300 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm²/mg
- Heavy-ION single-event upset (SEU): 1.34E-07 (geosynchronous) error/bit-day
- QML-V qualified (DLAM² part number: 5962F11201/02VXA)

Collateral
Cypress Datasheet: 72-Mbit SRAMs w/ RadStop™
DLAM Datasheet: 72-Mbit SRAMs w/ RadStop™

1 Cypress’s proprietary design and process technology that increases radiation-resistance
2 Defense Logistics Agency Land and Maritime, Columbus, OH
144Mb QDR®-II+ SRAM with RadStop™

**Applications**
Payload processing and reconfigurable computing platforms

**Features**
- Maximum frequency of operation/throughput: 250 MHz/36 Gbps
- Burst sizes: 2, 4
- Bus-width configurations: x18, x36
- Military temperature grade: -55°C to +125°C
- Two independent unidirectional data ports for read/write enable concurrent transactions
- Maximum throughput with double data rate (DDR) data ports
- Output impedance matching input (ZQ) matches the device outputs to system data bus impedance
- Featuring On-Die-Termination
- I/O signaling standards: 1.5 – 1.8 V (HSTL)
- Controller available for Xilinx and Microsemi FPGAs
- Total ionizing dose: 200 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg
- Heavy-ION single-event upset (SEU): 3.34E-07 (geosynchronous) error/bit-day
- QML-V qualified (DLAM part number: 5962R18214/15VXF)

**Availability**
Non-Space-Qualified Prototypes (CYPT264x/164x): Now
QML-V Space-Qualified Devices (CYRS264x/164x): Now

**Collateral**
Cypress Datasheet: [144-Mbit SRAMs w/ RadStop™](#)
DLAM Datasheet: [144-Mbit SRAMs w/ RadStop™](#)

![Diagram](#)
4Mb Fast SRAM with RadStop™

**Applications**
Payload processing, sensors and switches

**Features**
- Access time: 10 ns (85°C), 12 ns (125°C)
- Bus-width configuration: x8
- Operating voltage: 3.3 V
- Military temperature grade: −55°C to +125°C
- Bit-interleaving to eliminate multi-bit errors
- Package: 36-pin ceramic flat pack (CFP)
- Total ionizing dose: 300 Krad
- Heavy-ION single-event latch-up (SEL): 120 linear energy transfer (LET) MeV-cm sq/mg
- Heavy-ION single-event upset (SEU): 5.0E-08 (geosynchronous) error/bit-day
- QML-V qualified (DLAM part number: 5962F1123501VXC)

**Collateral**
- Cypress Datasheet: 4-Mbit SRAM w/ RadStop™
- DLAM Datasheet: 4-Mbit SRAM w/ RadStop™

**Availability**
- Non-Space-Qualified Prototypes (CYPT1049): Now
- QML-V Space-Qualified Devices (CYRS1049): Now
16Mb Fast SRAM with RadStop™

**Applications**
Payload processing, sensors and switches

**Features**
- Access time: 10 ns (125°C)
- Bus-width configuration: x8, x16, x32
- Operating voltage: 1.8 V – 5.0 V
- Military temperature grade: –55°C to +125°C
- Embedded ECC (SEC)
- Package: 54-pin ceramic TSOP (CTSOP)
- Total ionizing dose: 200 Krad
- Heavy-ION single-event latch-up (SEL): 60 linear energy transfer (LET) MeV-cm sq/mg
- Heavy-ION single-event upset (SEU): 3.0E-12 (geosynchronous) error/bit-day
- QML-V qualified (DLAM part number: 5962R2020201VXC)

**Collateral**
- Cypress Datasheet: [16-Mbit SRAM w/ RadStop™](#)
- DLAM Datasheet: [16-Mbit SRAM w/ RadStop™](#)

**Availability**
- Non-Space-Qualified Prototypes (CYPT1061): Now
- QML-V Space-Qualified Devices (CYRS1061): Now
Energy Harvesting PMIC Portfolio
# Energy Harvesting PMIC\(^1\) Portfolio

<table>
<thead>
<tr>
<th>Market Segment</th>
<th>Wearable Activity Monitor</th>
<th>Residential WSNs(^2) for HVAC(^3), Level of Light Emitted, Temperature, Humidity, Motion</th>
<th>Building WSNs for HVAC, Level of Light Emitted, Temperature, Humidity, Motion, BLE(^4) Beacon(^5)</th>
<th>Industrial WSNs for Infrastructure, Agriculture, Transportation, Factory Automation, Animal Monitoring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indoor/Outdoor</td>
<td>S6AE101A Linear, Power Gating(^6), Multiplexer(^7), 10-pin QFN</td>
<td>S6AE101A Linear, Power Gating, Multiplexer, 10-pin QFN</td>
<td>S6AE102A Linear, Power Gating, Multiplexer, LDO(^8), Comparator, 20-pin QFN</td>
<td>CY39C831 Boost DC/DC, MPPT(^9), Li-ion Protection, 40-pin QFN</td>
</tr>
<tr>
<td>Indoor</td>
<td></td>
<td></td>
<td></td>
<td>S6AE103A Linear, PowerGating, Multiplexer, LDO, Timer, Comparator, 24-pin QFN</td>
</tr>
<tr>
<td>Outdoor</td>
<td></td>
<td></td>
<td></td>
<td>CY39C831 Boost DC/DC, MPPT, Li-ion Protection, 40-pin QFN</td>
</tr>
</tbody>
</table>

### Power Management IC
- S6AE101A
- S6AE102A
- S6AE103A

### Energy Harvesting Devices
- Series Solar Cell by Panasonic (AM-1801)
- Single Solar Cell by Ningbo Hebe Solar (HSC125155)
- TEG by Micropelt (TGP-651)

### Notes
1. Power Management IC
2. Wireless sensor nodes
3. Heating, ventilation, air conditioning
4. Bluetooth Low Energy
5. A wireless device that transmits data (e.g., signal strength and ID) over a periodic radio signal from a known location
6. Output power control circuit that controls power provided to the system load
7. Power source switch circuit for primary battery or energy harvesting device
8. Low dropout regulator
9. Maximum power point tracking

---

167 Energy Harvesting PMIC
S6AE101A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications
Series solar cell energy harvesting\(^1\) and wireless sensor nodes\(^2\)

Features
- **Ultra-Low Power**
  - Enables 1 cm\(^2\) minimum solar cell size for startup operation\(^3\)
- **Input Voltage Range**
  - 2.0–5.5 V (series solar cell and primary battery)
- **Output Voltage Range**
  - 1.1–5.2 V
- **250-nA Quiescent Current**\(^4\)
- **1.2-µW Startup Power**
- **Power Gating**\(^5\) Switch Circuit
- **Storage Control Circuit**
- **Multiplexer**\(^6\) Circuit (battery vs. solar cell)
- **Overvoltage Protection (OVP)**
- **Packages**
  - 3.0 mm x 3.0 mm 10-pin SON

Collateral
- **Datasheet:** [S6AE101A Datasheet](#)
- **Development Kits:**
  - [Solar-Powered IoT Device Kit](#)
  - [S6AE10xA Evaluation Board](#)

Availability
**Production:** Now

1. The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
2. A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits data to a control unit, such as a PC or a mobile device
3. Estimate based on solar cell power = 2 µW/cm\(^2\) at 100 lx
4. Current consumed at no load condition
5. Output power control circuit that controls power provided to the system load
6. Power source switch circuit for primary battery and Energy Harvesting Device
7. Voltage reference circuit for internal block
S6AE102A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

**Applications**
- Series solar cell energy harvesting¹ and wireless sensor nodes²

**Features**
- **Ultra-Low Power**
  - Enables 1 cm² minimum solar cell size for startup operation³
- **Input Voltage Range**
  - Series solar cell: 2.0–5.5 V (series solar cell and primary battery)
  - 1.1–5.2-V Output Voltage Range
- **280-nA Quiescent Current⁴**
- **1.2-µW Startup Power**
- **400-nA Low Quiescent Current Low Dropout Regulator (LDO)**
- **Dual-Channel Power Gating Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management**
- **Signal Output Circuit of Power Gating Switch Control**
- **Multiplexer Circuit (battery vs. solar cell)**
- **Hybrid Storage Control Circuit⁷ and Overvoltage Protection (OVP)**
- **Packages**
  - 4.0 mm x 4.0 mm 20-pin QFN

**Collateral**
- **Datasheet:** [S6AE102A Datasheet](#)
- **Development Kits:** [S6AE10xA Evaluation Board, CYALKIT-E04](#)

**Availability**
- **Production:** Now

---

¹ The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
² A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
³ Estimate based on solar cell power = 2 µW/cm² at 100 lx
⁴ Current consumed at no load condition
⁵ Output power control circuit that controls power provided to the system load
⁶ Power source switch circuit for primary battery or series solar cell
⁷ Uses a small and large capacitor to automatically store excess power for backup
⁸ Voltage reference circuit for internal block
S6AE103A
Solar-Optimized Energy Harvesting Power Management IC (PMIC)

Applications
Series solar cell energy harvesting\(^1\) and wireless sensor nodes\(^2\)

Features
- Ultra-Low Power
  - Enables 1 cm\(^2\) minimum solar cell size for startup operation\(^3\)
- Input Voltage Range
  - 2.0-5.5 V (series solar cell and primary battery)
- 1.1–5.2 V Output Voltage Range
- 280 nA Quiescent Current\(^4\)
- 1.2 µW Startup Power
- 400 nA Low Quiescent Current Low Dropout Regulator (LDO)
- 30 nA Low Consumption Current CR Timer\(^5\)
- 20 nA General-Purpose Low Consumption Current Comparator
- Dual-Channel Power Gating\(^6\) Switch Circuit with Interrupt Request (IRQ) Control Function for Power Management
- Signal Output Circuit of Power Gating Switch Control
- Multiplexer\(^7\) Circuit (battery vs. solar cell)
- Hybrid Storage Control Circuit\(^8\) and Overvoltage Protection (OVP)
- Packages
  - 4.0 mm x 4.0 mm 20-pin QFN

Collateral
Datasheet: [S6AE103A Datasheet](#)
Development Kits: [S6AE10xA Evaluation Board, CYALKIT-E04](#)

Availability
Production: Now

---

\(^1\) The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
\(^2\) A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
\(^3\) Estimate based on solar cell power = 2 µW/cm\(^2\) at 100 lx
\(^4\) Current consumed at no load condition
\(^5\) Output power control circuit that controls power provided to the system load
\(^6\) Power source switch circuit for primary battery or series solar cell
\(^7\) Uses a small and large capacitor to automatically store excess power for backup
\(^8\) Voltage reference circuit for internal block
**CY39C831**

**General Purpose Energy Harvesting Power Management IC (PMIC)**

### Applications

- Single solar cell energy harvesting\(^1\), thermoelectric generator\(^2\) energy harvesting and wireless sensor nodes\(^3\)

### Features

- **Ultra-Low-Voltage Startup Boost DC/DC Converter**
- 0.3–4.75-V Input Voltage Range
- 0.35-V Startup Voltage
- Output Voltage (constant voltage mode only)
  - 3.0 V, 3.3 V, 3.6 V, 4.1 V, 4.5 V and 5.0 V
- 32-µA Quiescent Current\(^4\)
- Output Current
  - 8 mA ($V_{DD} = 0.6$ V, $V_{OUT} = 3.3$ V) and 80 mA ($V_{DD} = 3.0$ V, $V_{OUT} = 3.3$ V)
- 200-mA Input Peak Current Limit
- Built-In Maximum Power Point Tracking (MPPT)\(^5\) Function
- Built-In Li-ion Charge Function
- Input and Output Power Good Monitoring
- Package
  - 6.0 mm x 6.0 mm 40-pin QFN

### Collateral

- **Datasheet:** [CY39C831 Datasheet](#)
- **Development Kits:** [CY39C831 Evaluation Board](#)

### Availability

- **Production:** Now

---

1. The process of capturing and converting tiny amounts of energy (e.g., from light, vibration or heat) into electricity
2. Power Generation Device using heat
3. A sensor-based device that monitors conditions such as temperature, humidity and pressure and wirelessly transmits that data to a control unit, such as a PC or a mobile device
4. Current consumed at no load condition
5. Maximum Power Point Tracking maximizes the Energy Harvest by adjusting current drawn from a solar panel
6. Undervoltage lockout
7. Band Gap Reference
Cypress Roadmap: Automotive Products
## Cypress Automotive Roadmaps Slide Index

<table>
<thead>
<tr>
<th>Page</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>213</td>
<td>Automotive TrueTouch® &amp; PSoC®</td>
</tr>
<tr>
<td>199</td>
<td>Automotive Flash Memory</td>
</tr>
<tr>
<td>217</td>
<td>Automotive RAM</td>
</tr>
<tr>
<td>243</td>
<td>Automotive Power Management IC</td>
</tr>
<tr>
<td>249</td>
<td>Automotive Timing Solutions</td>
</tr>
<tr>
<td>254</td>
<td>Automotive Traveo™ MCU Family, Automotive Wireless Products, Automotive USB Products</td>
</tr>
</tbody>
</table>
Automotive TrueTouch® Roadmap
Automotive Portfolio: TrueTouch®

<table>
<thead>
<tr>
<th>Gen6</th>
<th>Gen7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gestures, AMS(^1) Thick Glove(^2) or Thick Overlay</td>
<td>In-Cell(^3), Gestures, AMS Thick Glove(^4) or Thick/Curved Overlay</td>
</tr>
<tr>
<td>Touchscreen, 10 Finger, AutoArmor™(^7), DualSense™(^8), H₂O(^9), Glove Touch(^10), Grades: A(^{11}) and S(^{12})</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CYAT8168X</th>
<th>CYAT8268X</th>
<th>CYAT817X</th>
</tr>
</thead>
<tbody>
<tr>
<td>88 I/O, 100-Hz RR(^13)</td>
<td>54 RX(^14), 100-Hz RR</td>
<td>103 I/O, 120-Hz RR</td>
</tr>
<tr>
<td>CYAT8168X</td>
<td>CYAT8268X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>77/71 I/O(^4), 120-Hz RR</td>
<td>46/39 RX, 120-Hz RR</td>
<td>88 I/O, 120-Hz RR</td>
</tr>
<tr>
<td>CYAT8168X</td>
<td>CYAT8268X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>61 I/O, 120-Hz RR</td>
<td>31 RX, 120-Hz RR</td>
<td>77/61 I/O, 120-Hz RR</td>
</tr>
<tr>
<td>CYAT8165X</td>
<td>CYAT8168X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>48 I/O, 100-Hz RR</td>
<td>CYAT8268X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>CYAT8268X</td>
<td>CYAT817X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>CYAT817X</td>
<td>54 RX(^14), 100-Hz RR</td>
<td>103 I/O, 120-Hz RR</td>
</tr>
<tr>
<td>CYAT817X</td>
<td>CYAT817X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>CYAT817X</td>
<td>CYAT817X</td>
<td>CYAT817X</td>
</tr>
<tr>
<td>CYAT817X</td>
<td>CYAT817X</td>
<td>CYAT817X</td>
</tr>
</tbody>
</table>

1 Automatic Mode Switching
2 1-mm to 5-mm glove thickness (ski gloves)
3 A type of sensor stack-up in which the RX sensor is inside the LCD module under the color-filter glass
4 Less than 1-mm glove thickness (normal leather gloves)
5 Low-power wake-up button
6 The ability of touchscreen to distinguish between different levels of force being applied on the touchscreen
7 Enables compliance with chip-level emission, immunity and system-level specifications
8 Self-Capacitance + Mutual-Capacitance
9 Waterproofing and wet-finger tracking
10 A feature that allows the detection of gloved fingers on a touch sensor
11 AEC-Q100: -40°C to +85°C
12 AEC-Q100: -40°C to +105°C
13 Refresh rate
14 Number of available I/Os depends on package selection
15 Receive Pins

<table>
<thead>
<tr>
<th>Concept</th>
<th>Development</th>
<th>Sampling</th>
<th>Production</th>
</tr>
</thead>
</table>

175 Cypress Roadmaps
## Automotive Portfolio: TrueTouch® Software

<table>
<thead>
<tr>
<th>Software</th>
<th>MPN</th>
<th>PSoC® Designer™</th>
<th>TrueTouch® Host Emulator</th>
<th>TrueTouch Driver for Android</th>
<th>Manufacturing Test Kit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Version</td>
<td></td>
<td>5.4 SP1</td>
<td>3.4.70</td>
<td>2.7</td>
<td>1.9.50</td>
</tr>
<tr>
<td>Gen 1</td>
<td>CY8CTMA120</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CY8CTMG120</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 3</td>
<td>CY8CTMA616</td>
<td>Production</td>
<td></td>
<td>TTDA 2.5.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CY8CTMA884</td>
<td>Production</td>
<td></td>
<td>Production</td>
<td></td>
</tr>
<tr>
<td>Gen 4</td>
<td>CY8CTMA460</td>
<td>Production</td>
<td></td>
<td>TTDA 2.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CY8CTMA461</td>
<td>Production</td>
<td></td>
<td>Production</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CY8CTMA768</td>
<td>Production</td>
<td></td>
<td>Production</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CY8CTMA1036</td>
<td>Production</td>
<td></td>
<td>Production</td>
<td></td>
</tr>
<tr>
<td>Gen 6</td>
<td>CYAT8165X-48</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-61</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-71</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-77</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-88</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gen 7</td>
<td>CYAT8X7XX</td>
<td>Production</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Contact Cypress Sales for the latest TrueTouch software, drivers and tools

1 PSoC Designer, TTHE and MTK releases are backward compatible. The latest version is recommended for new designs.
2 TrueTouch Host Emulator (TTHE) is a front-end tool used to configure, tune, debug and demonstrate TrueTouch devices
3 TrueTouch Driver for Android (TTDA) is the driver for Android that translates touch information into Linux/Android events
4 TrueTouch Manufacturing Test Kit (MTK) enables customers and ITO partners to test touch panels that use Cypress TrueTouch controllers through the manufacturing flow
### CYAT8268X

**Automotive TrueTouch® Gen6 Family**

#### Applications

- Large touchscreen human machine interface (HMI) systems

#### Features

- **Advanced User Interface**
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - 54 Receive channels to support ≥100-Hz refresh rates
  - DualSense\(^4\): Self\(^5\)- and mutual\(^5\)-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications
- **Sensor Design**
  - Supports Hybrid In-Cell\(^6\) sensors
- **System Solutions**
  - Manufacturing test kits for production testing
- **Package**
  - 100-pin TQFP

#### Collateral

**Datasheet and Design Guide:** [Contact Sales](mailto:contactsales@null.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

---

\(^1\) The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat

\(^2\) Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance

\(^3\) Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements

\(^4\) The capacitance of a row or column line in a touchscreen sensor

\(^5\) The capacitance between a row and a column in a touchscreen sensor

\(^6\) TX/VCOM share the same layer, receive ITO layer on/above the color filter

\(^7\) Interrupt

\(^8\) Display Driver Interface
CYAT8168X
Automotive TrueTouch® Gen6 Family

Applications
Large touchscreen human machine interface (HMI) systems

Features
▪ Advanced User Interface
  – Waterproofing\(^1\): Works with water droplets, condensation, sweat and wet-finger tracking
  – Tracking with up to 5-mm thick gloves or thick overlay
▪ Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)
  – True 5-V TX-Boost\(^4\) with Multi-Phase TX\(^4\)
  – 54 Receive Channels to support ≥100-Hz refresh rates
  – DualSense\(^5\): Self- and mutual-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  – AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications
▪ System Solutions
  – Manufacturing test kits for production testing
▪ Package
  – 128-pin TQFP, 100-pin TQFP

Collateral
Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability
Sampling: Now  Production: Now

\(^1\) The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
\(^2\) Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
\(^3\) Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
\(^4\) A scanning method used to drive multiple TX lines simultaneously
\(^5\) The capacitance of a row or column line in a touchscreen sensor
\(^6\) The capacitance between a row and a column in a touchscreen sensor
\(^7\) Interrupt
**CYAT8165X**

**Automotive TrueTouch® Gen6 Family**

### Applications

Small and medium touchscreen human machine interface (HMI) systems

### Features

- **Advanced User Interface**
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay

- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - True 5-V TX-Boost\(^4\) with Multi-Phase TX
  - 17 Receive Channels to support ≥100-Hz refresh rates
  - DualSense\(^5\): Self- and mutual-capacitance analog front end
  - (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications

- **System Solutions**
  - Manufacturing test kits for production testing

- **Package**
  - 100-pin TQFP and 64-pin TQFP

### Collateral

**Datasheet and Design Guide:** [Contact Sales](mailto:contact.sales@cybernetics.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

### Availability

**Sampling:** Now  
**Production:** Now

---

\(^1\) The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat

\(^2\) Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance

\(^3\) Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements

\(^4\) A scanning method used to drive multiple TX lines simultaneously

\(^5\) The capacitance of a row or column line in a touchscreen sensor

\(^6\) The capacitance between a row and a column in a touchscreen sensor

\(^7\) Interrupt
**CYAT7165X**

**Automotive TrueTouch® Gen6 Family**

### Applications
- Touchpad human machine interface (HMI) systems

### Features
- **Advanced User Interface**
  - Support with square, rectangular, round, and free-form shape
  - Waterproofing\(^1\): Works with water droplets, condensation, sweat, and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
  - Typical refresh rate of 120 Hz

- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - True 5-V TX-Boost\(^4\) with Multi-Phase TX\(^4\)
  - 17 Receive Channels to support typical refresh rate of 120 Hz
  - DualSense\(^5\): Self\(^5\)- and mutual\(^6\)-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), and system-level (CISPR 25) specifications

- **System Solutions**
  - Manufacturing test kits for production testing

- **Package**
  - 56-QFN wettable flank, 64-pin TQFP

### Collateral
- **Datasheet and Design Guide:** [Contact Sales](mailto:Contact.Sales@cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

### Availability
- **Sampling:** Q220
- **Production:** Q220

---

\(^1\) The ability of a touchpad sensor to work properly in the presence of water droplets, condensation or sweat

\(^2\) Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance

\(^3\) Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements

\(^4\) A scanning method used to drive multiple TX lines simultaneously

\(^5\) The capacitance of a row or column line in a touchscreen sensor

\(^6\) The capacitance between a row and a column in a touchscreen sensor

\(^7\) Interrupt
CYAT6165X
Automotive TrueTouch® Gen6 Family

Applications
Slider human machine interface (HMI) systems

Features

- **Advanced User Interface**
  - Waterproofing:\(^1\): Works with water droplets, condensation, sweat and wet-finger tracking
  - Tracking with up to 5-mm thick gloves or thick overlay
  - Typical refresh rate of 200 Hz
  - Low-power wake-up button: Typical power consumption of 50 µA

- **Proprietary Analog Front End\(^2\) with AutoArmor\(^3\)**
  - True 5-V TX-Boost\(^4\) with Multi-Phase TX\(^4\)
  - 17 Receive Channels to support ≥200-Hz refresh rates
  - DualSense\(^5\): Self\(^5\)- and mutual\(^6\)-capacitance analog front end (U.S. Patents 8,773,146; 8,358,142; 8,319,505; and 8,067,948)
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132) and system-level (CISPR 25) specifications

- **System Solutions**
  - Manufacturing test kits for production testing

- **Package**
  - 56-pin QFN wettable flank, 64-pin TQFP

Collateral

Datasheet and Design Guide: Contact Sales or automotive@cypress.com

Availability

Sampling: Now  Production: Now

---

1 The ability of a touchscreen sensor to work properly in the presence of water droplets, condensation or sweat
2 Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
3 Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
4 A scanning method used to drive multiple TX lines simultaneously
5 The capacitance of a row or column line in a touchscreen sensor
6 The capacitance between a row and a column in a touchscreen sensor
7 Interrupt
CYAT817X
Automotive TrueTouch® Gen7 Family

**Applications**
Integrated touchscreen human machine interface (HMI) systems with multimodal feedback

**Features**
- **Advanced User Interface**
  - 50-mm hover\(^1\) performance and force touch\(^2\) support
  - Supports low-power CapSense\(^3\) wake-up button
  - 4x timer/counter/pulse-width modulator (TCPWM) blocks for haptic feedback controls
  - 1x I\(^2\)S block for acoustic feedback
  - Parallel reporting of touch data via SCB\(^4\) or CAN blocks
  - Includes a Crypto block for optional data encryption
- **Proprietary Analog Front End\(^5\) with AutoArmor\(^6\)**
  - True 5-V TX-Boost\(^7\) with multi-phase TX
  - 64 receive channels to support ≥100-Hz refresh rates
  - Multi-phase self-capacitance methodology aids in meeting EMI/EMC requirements without performance degradation
  - AutoArmor enables compliance with chip-level emissions (IEC 61967), immunity (IEC 62132), ESD (IEC 62132), and system-level (CISPR 25) specifications
- **Packages**
  - 128-pin TQFP, 100-pin TQFP

**Collateral**
Datasheet and Design Guide: [Contact Sales](mailto:Contact.Sales@Cypress.com) or [automotive@cypress.com](mailto:automotive@cypress.com)

**Availability**
- **Sampling:** Now
- **Production:** Now

---

\(^1\) A feature allowing the detection of fingers hovering over the touchscreen sensor
\(^2\) The ability of a touchscreen sensor to distinguish between different levels of force being applied on the touchscreen
\(^3\) Cypress' touch-sensing user interface solution. The industry's No. 1 solution in sales by 4x over No. 2 due to superior performance
\(^4\) Serial communication block, configurable as SPI, I\(^2\)C or UART
\(^5\) Analog circuit in the touchscreen controller used to measure self- and mutual-capacitance
\(^6\) Cypress proprietary technology used to reduce emissions and improve EMI immunity to meet automotive EMC requirements
## Automotive TrueTouch Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Package</th>
<th>QFN</th>
<th>TQFP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pins</td>
<td>56</td>
<td>64</td>
</tr>
<tr>
<td>Body Size (mm)</td>
<td>8 x 8</td>
<td>10 x 10</td>
<td>14 x 14</td>
</tr>
<tr>
<td>Pitch (mm)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Gen 4</td>
<td>CY8CTMA460</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CY8CTMA461</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CY8CTMA768</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CY8CTMA1036</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Gen 6</td>
<td>CYAT6165X-41</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT7165X-41/48</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT6165X-48</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT8165X-48</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-61/71/77</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT8168X-88</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT8268X-XX</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Gen 7</td>
<td>CYAT817X-61/72</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>CYAT817X-77/88/103</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

1 Wettable flanks package to allow automated optical inspection (AOI)
Automotive PSoC® Roadmap
# Automotive PSoC and MCU Portfolio

<table>
<thead>
<tr>
<th>8-Bit</th>
<th>32-Bit Arm® Cortex®-M0/M0+</th>
<th>32-Bit Arm Cortex®-M3</th>
<th>32-Bit Arm Cortex®-M4</th>
<th>32-Bit Arm Cortex®-M7</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Analog Integration</td>
<td>Ultra-Low-Power 8-/16-Bit Replacement</td>
<td>Mid-Range Performance</td>
<td>High Performance</td>
<td>Next Generation</td>
</tr>
</tbody>
</table>

**Programmable System-on-Chip (PSoC)** is a brand of Cypress MCUs for the broad-base embedded market that delivers an Arm Cortex-M CPU (PSoC 4+) with unique software-defined peripherals and CapSense capacitive sensing.

**Flexible MCU (FM)** is a portfolio of high-performance Arm® Cortex®-M-based MCUs for industrial and consumer applications.

### PSoC 1
- **M8C CPU**
- 24 MHz, 32KB Flash
- 16 PAB, 16 PDB, 64 I/Os

### PSoC 3
- **8051 CPU**
- 67 MHz, 64KB Flash
- Up to 19 PAB, 30 PDB, 72 I/Os

### PSoC 4
- **Cortex®-M0/M0+**
- 48 MHz, 384KB Flash
- Up to 13 PAB, 20 PDB, 98 I/Os

### PSoC Analog Coprocessor CY8C4Ax
- 48 MHz, 32KB Flash
- Up to 12 PAB, 11 PDB, 38 I/Os

### FM0+ MCUs
- **Cortex®-M0+**
- 40 MHz, 512KB Flash, 102 I/Os

### PSoC 5LP
- **Cortex®-M3**
- 80 MHz, 256KB Flash
- 20 PAB, 30 PDB, 72 I/Os

### FM3 MCUs
- **Cortex®-M3**
- 144 MHz, 1.5MB Flash, 154 I/Os

### PSoC 6 HMI
- **Cortex®-M4 and Cortex®-M0+**
- NDA Required, Contact Sales

### PSoC 4
- **Cortex®-M0/M0+**
- 48 MHz, 384KB Flash
- Up to 13 PAB, 20 PDB, 98 I/Os

### PSoC 7
- **Cortex®-M7**
- NDA Required, Contact Sales

### FM4 MCUs
- **Cortex®-M4**
- 200 MHz, 2MB Flash, 190 I/Os

---

1 A programmable analog block that is configured using PSoC software to create analog front ends, signal conditioning circuits with opamps and filters.

2 A programmable digital block that is configured using PSoC software to implement custom digital peripherals and glue logic.
### Automotive Portfolio: PSoC® 1

#### M8C CPU | 24 MHz

<table>
<thead>
<tr>
<th>PSoC MCU</th>
<th>Programmable Digital</th>
<th>Intelligent Analog</th>
<th>Performance Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY8C21x23</td>
<td>4K/0.25K, 16 GPIOs</td>
<td>1x10-bit ADC</td>
<td></td>
</tr>
<tr>
<td>CY8C23x33</td>
<td>8K/0.25K, 26 GPIOs</td>
<td>CapSense, 1x 8-bit SAR ADC</td>
<td></td>
</tr>
<tr>
<td>CY8C24x93</td>
<td>32K/2K, 36 GPIOs</td>
<td>1x10-bit ADC</td>
<td></td>
</tr>
<tr>
<td>CY8C21x34</td>
<td>8K/0.5K, 28 GPIOs</td>
<td>CapSense, 2x10-bit ADC</td>
<td></td>
</tr>
</tbody>
</table>

| CY8C24894 | 16K/1K, 56 GPIOs | CapSense, 2x14-bit SAR ADC | Grade: A |
| CY8C24x23 | 4K/0.25K, 24 GPIOs | CapSense, 1x14-bit ΔΣ ADC | Grades: A and E |
| CY8C29x66 | 32K/2K, 44 GPIOs | 1x14-bit ΔΣ ADC | Grades: A¹ and E² |
| CY8C27x43 | 32K/2K, 44 GPIOs | CapSense, 4x14-bit ΔΣ ADC | |

---

1. Flash KB/SRAM KB
2. General-purpose input/output pins
3. Analog-to-digital converter: Includes incremental, successive approximation register (SAR) or Delta-Sigma (ΔΣ) ADCs
4. AEC-Q100: -40°C to +85°C
5. AEC-Q100: -40°C to +125°C

---

[Image of Cypress Roadmaps]
<table>
<thead>
<tr>
<th>Automotive Portfolio: PSoC® 4</th>
<th>Flexibility</th>
<th>CapSense®</th>
<th>Ease-of-Use</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PSoC MCU</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PSoC 4000</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Intelligent Analog PSoC 4100</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S = S-Series</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M = M-Series</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4045-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 32K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4024-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0+, 16K/2K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4014</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16-MHz M0, 16K/2K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, PC, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4124</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0+, 16K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4125</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0+, 32K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4126-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4126-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0+, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4127-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4127-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, S and E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4147-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, S and E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4147-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, S and E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4149-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 384K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4149-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 256K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x7-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4247-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UDB, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4247-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UDB, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4246-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UDB, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4246-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UDB, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4146-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, S and E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4146-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 64K/8K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, Opamp, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A, S and E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4149-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 384K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x8-HVT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 256K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x8-HVT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 256K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x7-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x7-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4245</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0, 32K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4148-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 32K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4148-M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 32K/4K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP, ADC, SCB, IDAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Smart I/O, CAN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grades: A and S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C4149-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 384K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x8-HVT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 256K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x8-HVT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 256K/32K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x7-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY8C41x7-HV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48-MHz M0+, 128K/16K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDA Contact Sales</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Flash KB/ SRAM KB
2 Comparator
3 Controller area network
4 AEC-Q100: -40°C to +105°C
5 Universal digital block
6 AEC-Q100: -40°C to +85°C
7 AEC-Q100: -40°C to +105°C

Industrial
Automotive
Availability

Concept Development
Sampling Production

\[187\] Cypress Roadmaps
Automotive Portfolio: PSoC® Software

<table>
<thead>
<tr>
<th>Software</th>
<th>PSoC Creator™²</th>
<th>PSoC Designer™³</th>
<th>PSoC Programmer⁴</th>
<th>EZ-Click ™⁵</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Version</td>
<td>4.3</td>
<td>5.4 SP1</td>
<td>3.28.6</td>
<td>2.0 SP2</td>
</tr>
<tr>
<td>PSoC 1</td>
<td></td>
<td>Production</td>
<td>Production</td>
<td></td>
</tr>
<tr>
<td>PSoC 4</td>
<td>Production</td>
<td>Production</td>
<td>Production</td>
<td></td>
</tr>
</tbody>
</table>

Download the latest PSoC software version [here](#).

---

1 All software and tool releases are backward compatible. The latest versions are recommended for new designs.

2 PSoC Creator is an Integrated Design Environment (IDE) that allows concurrent hardware and firmware design of PSoC 3 and PSoC 4 systems.

3 PSoC Designer is an IDE that enables firmware design using a library of precharacterized peripherals for PSoC 1 systems.

4 PSoC Programmer can be used with PSoC Designer and PSoC Creator to program and debug any design onto a PSoC device.

5 EZ-Click is a Windows® GUI-based tool that enables development of CapSense MBR solutions. It allows you to set up sensor configuration, apply global system properties, monitor real-time sensor output, and run production-line system diagnostics.
PSoC® 4000S-Series
PSoC MCU

Applications
User interface for infotainment systems, user interface for heating, ventilation, air conditioning

Features
- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 32KB Flash
  - 4KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 10-bit, 46.8-ksps single-slope analog-to-digital converter (ADC)\(^1\)
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Two serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave
- **Packages**
  - 24-pin QFN and 28-pin SSOP
- **I/O Subsystem**
  - Up to 24 GPIOs, including 16 Smart I/Os\(^2\)

Collateral

Datasheet: **PSoC 4000S**

---

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem

Availability

Sampling: Now  Production: Now
PSoC® 4100S-Series
Intelligent Analog

Applications
User interface for heating, ventilation, air conditioning, MCU and discrete analog replacement

Features
- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 64KB Flash
  - 8KB SRAM
  - Real-time clock (RTC) capability with a watch crystal oscillator (WCO)
- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksp single-slope ADC
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC
- **Programmable Digital Blocks**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Three serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave
- **Packages**
  - 28-pin SSOP and 40-pin QFN
- **I/O Subsystem**
  - Up to 34 GPIOs, including 16 Smart I/Os

Collateral
- **Datasheet**: PSoC 4100S

1 A simple ADC used to measure slow-moving signals
2 Embedded programmable digital logic in the I/O subsystem
**Applications**

User interface for HMI applications, Body Control and HVAC applications

**Features**

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller and real-time clock (RTC)
  - 128KB Flash and 16KB SRAM
  - External MHz oscillator (ECO) with PLL and 32KHz watch crystal oscillator (WCO)

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - One 10-bit, 46.8-ksp single-slope ADC\(^1\)
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - One CapSense® block that supports low-power operation with self- and mutual-capacitance sensing
  - Two 7-bit current-output digital-to-analog converters (IDAC) configurable as a single 8-bit IDAC

- **Programmable Digital Blocks**
  - Eight 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Five serial communication blocks (SCBs) that are configurable as I²C, SPI, UART or LIN Slave

- **One Controller Area Network (CAN) Controller**

- **Packages**
  - Up to 54 GPIOs, including 24 Smart I/Os\(^2\)

**Collateral**

Datasheet: [Contact Sales](#)

\(^1\) A simple ADC used to measure slow-moving signals  
\(^2\) Embedded programmable digital logic in the I/O subsystem  

---

**Availability**

**Sampling:** Now  
**Production:** Now
PSoC® 4100M-Series
Intelligent Analog

Applications
User interface for HMI applications, body Control and HVAC applications

Features
- **32-bit MCU Subsystem**
  - 24-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM
- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Msps successive approximation register (SAR) ADC
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)
- **Programmable Digital Blocks**
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART
- **Packages**
  - 48-pin LQFP and 64-pin TQFP
- **I/O Subsystem**
  - Up to 51 GPIOs

Collateral
Datasheet: [Contact Sales](#)

Availability
**Sampling:** Now  **Production:** Now

Datasheet:
[Contact Sales](#)
PSoC® 4200M-Series
Programmable Digital

**Applications**
User interface for HMI applications, body Control and HVAC applications

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU with a DMA controller and real-time clock (RTC)
  - Up to 128KB Flash and 16KB SRAM

- **Programmable Analog Blocks**
  - Two comparators (CMP)
  - Four opamps, programmed as PGAs, CMPs, filters, etc.
  - One 12-bit/1-Mspss successive approximation register (SAR) analog-to-digital converter (ADC)
  - One CapSense® block with self- and mutual-capacitance sensing
  - Four (2x 8-bit, 2x 7-bit) current-output digital-to-analog converters (IDACs)

- **Programmable Digital Blocks**
  - Four universal digital blocks (UDBs): custom digital peripherals
  - Eight programmable 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - Four serial communication blocks (SCBs) configurable as I²C master or slave, SPI master or slave, or UART

- **Two Controller Area Network (CAN) Controllers**

- **Packages**
  - 48-pin LQFP, 56-pin QFN and 64-pin TQFP

**Collateral**
Datasheet: Contact Sales

**Availability**
Sampling: Now  Production: Now

---

PSoC® 4 One-Chip Solution

MCU Subsystem
- arm Cortex®-M0 48 MHz

Programmable Analog Blocks
- Opamp x4
- SAR ADC
- CMP x2
- CSD

Programmable Digital Blocks
- Flash (64KB to 128KB)
- SRAM (8KB to 16KB)
- Serial Wire Debug
- CAN x2
- RTC
- DMA
- Advanced High-Performance Bus (AHB)

I/O Subsystem
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8
- GPIO x8

Programmable Interconnect and Routing
- UDB x4
- TCPWM x8
- SCB x4
- Segment LCD Drive
PSoC 4 HVPA | CY8C41x7-HV
Precision Analog

Applications
Intelligent battery monitoring and management systems

Features
- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller
  - 128KB Program Flash, 8KB SRAM and up to 4KB Data Flash EEPROM, with ECC
- **Precision Analog Channel Subsystem**
  - Two 16-bit Precision $\Delta\Sigma$ analog-to-digital converters (ADC)
  - Voltage Channel with High-Voltage input divider, Current Channel with automatic Gain
  - Temperature and diagnostic channels
  - Digital filtering, accumulators, and threshold comparisons on all channels
- **Programmable Digital Subsystem**
  - Four 16-bit timer-counter/pulse-width modulation (TCPWM) blocks
  - One independent Local Interconnect Network (LIN) block
  - One serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave
- **High Voltage Subsystem**
  - Operates directly off 12V battery (tolerant up to 42V), Integrated LIN Transceiver
- **ASIL-B Compliant**
- **Packages**
  - 32-pin Wetable Flank QFN
- **I/O Subsystem**
  - Precision Analog (up to 11), GPIOs (up to 8)

Collateral
Datasheet: [Contact Sales]

1 Optional Feature

Availablility
Sampling: Q320    Production: Q122
PSoC 4 HVPA | CY8C41x8-HV

Precision Analog

Applications
Intelligent battery monitoring and management systems

Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller
  - 192KB Program Flash, 16KB SRAM and up to 8KB Data Flash EEPROM, with ECC
- **Security**: Advanced cryptographic coprocessor (Crypto) for hardware encryption
- **Precision Analog Channel Subsystem**
  - Two 16-bit Precision ΔΣ analog-to-digital converters (ADC)
  - Voltage Channel with High-Voltage input divider, Current Channel with automatic Gain
  - Temperature and diagnostic channels
  - Digital filtering, accumulators, and threshold comparisons on all channels
- **Programmable Digital Subsystem**
  - Four 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - One independent Local Interconnect Network (LIN) block
  - One serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave
- **One Controller Area Network (CAN) Controller**
- **High Voltage Subsystem**
  - Operates directly off 12V battery (tolerant up to 42V), Integrated LIN Transceiver
- **ASIL-C Compliant**
- **Package**: 48-pin Wetable Flank QFN
- **I/O Subsystem**: Precision Analog (up to 11), GPIOs (up to 16)

Collateral

**Datasheet**: Contact Sales

1 Optional Feature

Availability

**Sampling**: TBD  **Production**: TBD
PSOC 4 HVMS | CY8C41x6-HVMS
High-Voltage, Mixed Signal

Applications
Multi-sensor hub (one-chip solution integrating MCU, Multi-Sense converter, LIN PHY and HVREG)

Features

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller
  - 64KB Program Flash, 8KB SRAM and up to 4KB Data Flash EEPROM, with ECC

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - Multi-Sense converter integrating 5th generation CapSense® (capacitive-sensing) and MagSense™ (inductive-sensing)

- **Programmable Digital Subsystem**
  - Five 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - One independent Local Interconnect Network (LIN) block
  - Two serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave

- **High Voltage Subsystem**
  - Operates directly off 12V battery (tolerant up to 42V), Integrated LIN Transceiver

- **ASIL-B Compliant**

- **Packages**
  - 32-pin Wetable Flank QFN, 48-pin Wetable Flank QFN

- **I/O Subsystem**
  - Up to 36 GPIOs

Collateral

- **Datasheet**: Contact Sales

1 Optional Feature

Availability

- **Sampling**: TBD
- **Production**: TBD
**Applications**

Multi-sensor hub (one-chip solution integrating MCU, Multi-Sense converter, LIN PHY and HVREG)

**Features**

- **32-Bit MCU Subsystem**
  - 48-MHz Arm® Cortex®-M0+ CPU with DMA controller
  - 128KB Program Flash, 16KB SRAM and up to 8KB Data Flash EEPROM, with ECC

- **Programmable Analog Blocks**
  - One 12-bit, 1-Msps successive approximation register (SAR) analog-to-digital converter (ADC)
  - Two opamps configurable as programmable gain amplifiers (PGA), comparators, etc.
  - Two low-power comparators (CMP)
  - Multi-Sense converter integrating 5th generation CapSense® and MagSense™

- **Programmable Digital Subsystem**
  - Eight 16-bit timer/counter/pulse-width modulation (TCPWM) blocks
  - One independent Local Interconnect Network (LIN) block
  - Four serial communication blocks (SCB) that are configurable as I²C, SPI, UART or LIN Slave
  - One CAN-FD (Controller Area Network with Flexible Data-rate) Controller

- **High Voltage Subsystem**
  - Operates directly off 12V battery (tolerant up to 42V), Integrated LIN Transceiver

- **ASIL-B Compliant**

- **Packages**
  - 32-pin Wetable Flank QFN, 48-pin Wetable Flank QFN, 64-pin TQFP

- **I/O Subsystem**
  - Up to 54 GPIOs

**Collateral**

Datasheet: [Contact Sales](#)

---

**Availability**

Sampling: TBD   Production: TBD
## Automotive PSoC Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Package</th>
<th>QFN</th>
<th>SOIC</th>
<th>SSOP</th>
<th>TQFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>24</td>
<td>40</td>
<td>56</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>Body Size (mm)</td>
<td>4 x 4</td>
<td>6 x 6</td>
<td>8 x 8</td>
<td>3.8 x 9.9</td>
<td>5.3 x 7.3</td>
</tr>
<tr>
<td>Pitch (mm)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>1.27</td>
<td>0.65</td>
</tr>
<tr>
<td>PSoC 1</td>
<td>21X34</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>24X23</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>24894</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>29X66</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PSoC 4</td>
<td>4000</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>41/42XX</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>40XXS</td>
<td>✓¹</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>41XXS</td>
<td>✓¹</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>41XXS Plus</td>
<td>✓¹</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>41/42XXM</td>
<td>✓¹</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

¹ Wettable flanks package to allow automated optical inspection (AOI)
Flash Memory Automotive Roadmaps
NOR Flash Memory Automotive Family Decoder

Technology:
- J = 110-nm Floating Gate (FG)
- K = 90-nm FG
- L = 65-nm FG
- M = 50-nm FG
- N = 110-nm MirrorBit® (MB)
- P = 90-nm MB
- S = 65-nm MB
- T = 45-nm MB

Density:
- 008 = 8Mb
- 016 = 16Mb
- 032 = 32Mb
- 064 = 64Mb
- 128 = 128Mb
- 256 = 256Mb
- 512 = 512Mb
- 01G = 1Gb
- 02G = 2Gb
- 04G = 4Gb

Voltage:
- D = 2.5 V
- L = 3.0 V
- S = 1.8 V

Family:
- A = Standard Address-Data Parallel (ADP)
- C = Burst Mode ADP
- F = Serial
- G = Page Mode
- H = High-Performance Serial
- J = Simultaneous Read/Write ADP
- K = HyperBus™
- P = Page Mode Simultaneous Read/Write ADP

Series:
- 25 = SPI
- 26 = HyperBus™
- 35 = SPI with Security
- 36 = HyperBus™ with Security
- 28 = Octal
- 38 = Octal with Security
- 29 = Parallel
- 70 = Stacked Die
- 79 = Dual Quad SPI

Prefix:
- S
### NOR Flash Memory Automotive Product Portfolio: New Products

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Sector Size</th>
<th>Series</th>
<th>Voltage</th>
<th>Densities</th>
<th>Lead</th>
<th>Tech</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semper™ Flash</td>
<td>Quad SPI</td>
<td>Hybrid</td>
<td>S25HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S25HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hybrid</td>
<td>S26HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hybrid</td>
<td>S28HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S28HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HyperBus</td>
<td>Hybrid</td>
<td>S26HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Octal</td>
<td>Hybrid</td>
<td>S25HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S25HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hybrid</td>
<td>S26HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hybrid</td>
<td>S28HS-T</td>
<td>1.8 V</td>
<td>128Mb-4Gb</td>
<td>512Mb</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S28HL-T</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>QSPI</td>
<td>Hybrid</td>
<td>S25FS-S</td>
<td>1.8 V</td>
<td>64Mb-1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S25FL-S</td>
<td>3.0 V</td>
<td>128Mb-1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Uniform 4kB</td>
<td>S25FL-L</td>
<td>3.0 V</td>
<td>64-256Mb</td>
<td>-</td>
<td>65-nm FG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>S79FS-S</td>
<td>1.8 V</td>
<td>256Mb-1Gb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S79FL-S</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HyperFlash</td>
<td>HyperBus™</td>
<td>S26KS-S</td>
<td>1.8 V</td>
<td>128-512Mb</td>
<td>-</td>
<td>65-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>S26KL-S</td>
<td>3.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel</td>
<td>Parallel</td>
<td>Hybrid</td>
<td>S29GL-T</td>
<td>3.0 V</td>
<td>512Mb-2Gb</td>
<td>-</td>
<td>45-nm MB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## x8 Serial NOR Flash Memory Automotive Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod(^1) [EOL])</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
</tr>
<tr>
<td>S28HS-T(^2) (1.8 V)</td>
<td>4Gb(^4)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S28HL-T(^2) (3.0 V)</td>
<td>2Gb(^4)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper™ Flash with Octal Interface 45-nm MB(^3)</td>
<td>1Gb</td>
<td>(Q2’21)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26HS-T(^2) (1.8 V)</td>
<td>4Gb(^4)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26HL-T(^2) (3.0 V)</td>
<td>2Gb(^4)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Semper Flash with HyperBus™ Interface 45-nm MB(^3)</td>
<td>1Gb</td>
<td>(Q2’21)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26KS-S (1.8 V)</td>
<td>512Mb</td>
<td>(EOL - LTB)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S26KL-S (3.0 V)</td>
<td>256Mb</td>
<td>(EOL - LTB)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperFlash 65-nm MB(^3)</td>
<td>128Mb</td>
<td>(EOL - LTB)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S79FS-S (1.8 V)</td>
<td>512Mb</td>
<td>(EOL - LTS)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S79FL-S (3.0 V)</td>
<td>256Mb</td>
<td>(EOL - LTS)</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 AEC-Q100  
2 JEDEC xSPI Compliant  
3 Hybrid Sector  
4 Stacked Die  
5 1.8 V only in production  
6 S79 Series (stacked die)

Products supported by Longevity Program unless noted:  
- Production  
- Concept  
- Samples  
- EOL - LTB  
- EOL - LTS

202 Cypress Roadmaps
# x8 Serial NOR Flash Memory Automotive Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>SDR Clock / DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dual Quad SPI</strong></td>
<td><strong>HyperFlash</strong></td>
<td><strong>Semper™ Flash</strong></td>
</tr>
<tr>
<td>S79FL-S^1</td>
<td>S26KL-S^1</td>
<td>S26HL-T^1</td>
</tr>
<tr>
<td>65-nm MB, 3.0 V</td>
<td>65-nm MB, 3.0 V</td>
<td>45-nm MB, 3.0 V</td>
</tr>
<tr>
<td><strong>S26FL-S</strong></td>
<td><strong>S79FL-S</strong></td>
<td><strong>S26HL-T</strong></td>
</tr>
<tr>
<td>133 MHz / 80 MHz</td>
<td>133 MHz / 80 MHz</td>
<td>166 MHz / 166 MHz</td>
</tr>
<tr>
<td><strong>A, B</strong></td>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
</tr>
<tr>
<td><strong>S26KL-S</strong></td>
<td><strong>S26HL-S</strong></td>
<td></td>
</tr>
<tr>
<td>100 MHz / 100 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-S</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-T</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-T</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-T</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-T</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
<tr>
<td><strong>S26HL-T</strong></td>
<td><strong>S26HL-T</strong></td>
<td></td>
</tr>
<tr>
<td>166 MHz / 166 MHz</td>
<td>166 MHz / 166 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>A, B, M</strong></td>
<td><strong>A, B, M</strong></td>
<td></td>
</tr>
</tbody>
</table>

1. Hybrid Sector
2. Stacked die
3. HyperBus Interface (xSPI Profile 2.0)
4. Octal Interface (xSPI Profile 1.0)
5. Contact Sales for higher speed offerings

---

**Notes:**
- **A** = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
- **B** = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- **M** = Automotive, AEC-Q100 Grade 1: -40°C to +125°C
# x4 Serial NOR Flash Memory Automotive Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod[^1]) (EOL)</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2Gb[^3]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>(Q2’21)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb[^8]</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S25FL-L (3.0 V) QSPI 65-nm FG[^4]</td>
<td>256Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb[^9]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[^1]: AEC-Q100  
[^2]: Hybrid Sector  
[^3]: VIO 1.8 V to 3.0 V  
[^4]: Uniform Sector  
[^5]: Stacked Die  
[^6]: 3.0 V only in production  
[^7]: S70 Series (stacked die)  
[^8]: S25FL127S and S25FL128S  
[^9]: FS-S only  
[^10]: S25FL128P and S25FL129P
# x4 Serial NOR Flash Memory Automotive Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>SDR Clock / DDR Clock</th>
<th>* Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S25FL256P5</td>
<td>104 MHz / --</td>
<td>* A</td>
</tr>
<tr>
<td>S25FL256L5</td>
<td>133 MHz / 66 MHz</td>
<td>* A, B, M</td>
</tr>
<tr>
<td>S25FL256S5</td>
<td>133 MHz / 66 MHz</td>
<td>* A, B, M</td>
</tr>
<tr>
<td>S25FL129P6</td>
<td>104 MHz / --</td>
<td>* A, B</td>
</tr>
<tr>
<td>S25FL128S6</td>
<td>133 MHz / 66 MHz</td>
<td>* A, B, M</td>
</tr>
<tr>
<td>S25FL064P6</td>
<td>104 MHz / --</td>
<td>* A, B</td>
</tr>
<tr>
<td>S25FL032P6</td>
<td>104 MHz / --</td>
<td>* A, B</td>
</tr>
</tbody>
</table>

1. Hybrid Sector
2. Uniform Sector
3. With QSPI
4. Contact Sales
5. Contact Sales for higher speed offerings
6. S25FL129P Quad SPI
7. S25FL128P Dual SPI
8. Stack die
9. S70 series (stacked die)

* A = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
* B = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
* M = Automotive, AEC-Q100 Grade 1: -40°C to +125°C

- **S25FL** Series: 90 nm, 3.0 V
- **S25FL** Series: 65 nm, 3.0 V
- **S25FS** Series: 65 nm, 1.8 V
- **S25HL** Series: 45 nm, 3.0 V
- **S25HS** Series: 45 nm, 1.8 V
- **S25HS04GT** Series: 133 MHz / 80 MHz
- **S25HS02GT** Series: 133 MHz / 80 MHz
- **S25FL04GT** Series: 133 MHz / 80 MHz
- **S25HL02GT** Series: 133 MHz / 80 MHz
- **S25HL01GT** Series: 166 MHz / 102 MHz
- **S25HL52GT** Series: 166 MHz / 102 MHz
- **S25HS01GT** Series: 166 MHz / 102 MHz
- **S25HL02GT** Series: 166 MHz / 102 MHz
- **S25FL064S** Series: 133 MHz / 80 MHz
- **S25FL128S** Series: 133 MHz / 80 MHz
- **S25FL127S** Series: 133 MHz / 80 MHz
- **S25FS064S** Series: 133 MHz / 80 MHz
- **S25HS128T** Series: 166 MHz / 102 MHz
- **S25HL128T** Series: 166 MHz / 102 MHz
- **S25FL129P** Series: 104 MHz / 54 MHz
- **S25HL04GT** Series: 133 MHz / 80 MHz
- **S25FL064S** Series: 133 MHz / 54 MHz
- **S25HL04GT** Series: 133 MHz / 80 MHz
- **S25HL01GT** Series: 166 MHz / 102 MHz
- **S25HL01GT** Series: 166 MHz / 102 MHz

- **Semper™ Flash**
- **QSPI**
- **S25FL**
- **S25FLS**
- **S25HL**
- **S25FS**
- **S25HS**

### Status and Availability

- **Concept**
- **Development**
- **Sampling**
- **Production**
- **EOL (Last-Time-Ship)**

### Engineering

- **AEC-Q100/ISO26262**
# Parallel and Burst Parallel NOR Flash Memory Automotive Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(Prod(^1)) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29GL-T(^2) (3.0 V) 45-nm MB</td>
<td>2Gb(^4) 1Gb 512Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29GL-S(^2) (3.0 V) 65-nm MB</td>
<td>2Gb(^4) 1Gb 512Mb 256Mb 128Mb 64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29GL-N(^2) (3.0 V) 110-nm MB</td>
<td>64Mb 32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29PL-J(^2,3) (3.0 V) 110-nm FG</td>
<td>128Mb 64Mb 32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29UL-J(^2) (3.0 V) 110-nm FG</td>
<td>64Mb 32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29AL-J (3.0 V) 110-nm FG</td>
<td>16Mb 8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29AS-J (1.8 V) 110-nm FG</td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29CD-J (2.5 V) Burst Parallel 110-nm FG</td>
<td>32Mb 16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S29CL-J (3.0 V) Burst Parallel 110-nm FG</td>
<td>32Mb 16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 AEC-Q100  
2 Supports Simultaneous Read/Write Operation  
3 Supports Page Mode  
4 S70 series (stacked die)  

Products supported by Longevity Program unless noted

- **EOL - LTB**  
- **EOL - LTS**
Parallel and Burst Parallel NOR Flash Memory

**Automotive Portfolio**

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial / Page Access</th>
<th>Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29AS-J</td>
<td>ADP Burst</td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29AL-J</td>
<td>ADP Burst</td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29AS016J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29AS016J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29AL016J</td>
<td></td>
<td>A, M</td>
</tr>
<tr>
<td>S29CL016J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CD016J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CD016J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29CL032J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CD032J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CL064J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL064J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL128J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL32S</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL08S</td>
<td></td>
<td>A, M</td>
</tr>
</tbody>
</table>

1. Address Data Parallel (ADP) Burst
2. Supports Simultaneous Read/Write Operation
3. Supports Page Mode

**S70 series (stacked die)**

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>Initial / Page Access</th>
<th>Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S29CL032J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CD032J</td>
<td></td>
<td>A, M, T</td>
</tr>
<tr>
<td>S29CL064J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL064J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL128J</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL32S</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>S29GL08S</td>
<td></td>
<td>A, M</td>
</tr>
</tbody>
</table>

**Status**

- Concept
- Development
- Engineering
- AEC-Q100/Sampling
- Production
- QQTY
- QQTY

**Availability**

- Concept
- Development
- EOL (Last-Time-Ship)

**EOL (Last-Time-Ship)**
Flash and RAM Memory Automotive MCP
### Flash and RAM Memory Automotive MCP Decoder

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Series</th>
<th>Family</th>
<th>Flash Technology</th>
<th>Flash Density</th>
<th>Voltage</th>
<th>RAM Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>76</td>
<td>76</td>
<td>HyperBus Interface (xSPI Profile 2.0)</td>
<td>512 = 512Mb</td>
<td>S</td>
<td>C = 64Mb</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NOR Flash + HyperRAM™</td>
<td></td>
<td></td>
<td>D = 128Mb</td>
</tr>
<tr>
<td></td>
<td>78</td>
<td>78</td>
<td>Octal Interface (xSPI Profile 1.0)</td>
<td>256 = 256Mb</td>
<td>S</td>
<td>E = 256Mb</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NOR Flash + HyperRAM™</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>71</td>
<td>71</td>
<td>NOR Flash + pSRAM</td>
<td>128 = 128Mb</td>
<td>L</td>
<td>A = 16Mb</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Flash Technology</th>
<th>Flash Density</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>S = 65-nm MirrorBit (MB)</td>
<td>128 = 128Mb</td>
<td>L = 3.0 V</td>
</tr>
<tr>
<td>T = 45-nm MB</td>
<td>256 = 256Mb</td>
<td>S = 1.8 V</td>
</tr>
<tr>
<td></td>
<td>512 = 512Mb</td>
<td></td>
</tr>
<tr>
<td></td>
<td>01G = 1Gb</td>
<td></td>
</tr>
</tbody>
</table>
Flash and RAM Memory Automotive MCP Roadmap

<table>
<thead>
<tr>
<th>Product Family Flash / RAM</th>
<th>Flash / RAM Density</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
</tr>
<tr>
<td>S78HS-T (1.8 V)¹</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb</td>
<td>(Q2'22)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb</td>
<td>(Q2'21)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S76HS-T (1.8 V)²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm Semper™ Flash / HyperRAM™</td>
<td>1Gb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71KS-S (1.8 V)³</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65-nm HyperFlash / HyperRAM</td>
<td>512Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S78HL-T (3.0 V)¹</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm Semper™ Flash / HyperRAM</td>
<td>1Gb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S76HL-T (3.0 V)²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45-nm Semper™ Flash / HyperRAM</td>
<td>1Gb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb/64Mb</td>
<td>(Q1'21)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/128Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb/64Mb</td>
<td>(Q2'22)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S71KL-S (3.0 V)³</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65-nm HyperFlash / HyperRAM</td>
<td>512Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb / 64Mb</td>
<td>(TBD)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ AEC-Q100
² Octal Interface (xSPI Profile 1.0)
³ HyperBus Interface (xSPI Profile 2.0)

Concept: Production Samples
EOL - LTB EOL - LTS

Products supported by Longevity Program unless noted.
## Flash and RAM Memory Automotive MCP Portfolio

<table>
<thead>
<tr>
<th>Product Family Number</th>
<th>RAM Density</th>
<th>Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>S71KL-S</td>
<td>64Mb</td>
<td>A, B</td>
</tr>
<tr>
<td>S76HL-T</td>
<td>128Mb</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td>S78HL-T</td>
<td>128Mb</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td>S71KS-S</td>
<td>64Mb</td>
<td>A, B</td>
</tr>
<tr>
<td>S76HS-T</td>
<td>128Mb</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td>S78HS-T</td>
<td>128Mb</td>
<td>I, A, V, B</td>
</tr>
</tbody>
</table>

### Flash Memory

- **HyperFlash**
- **HyperBus Interface (xSPI Profile 2.0)**
- **Octal Interface (xSPI Profile 1.0)**
- **HyperRAM™**

### Status

- **Concept**: Q320
- **Development**: Q121
- **Engineering Sampling**: QQYY
- **Production**: QQYY
- **EOL (Last-Time-Ship)**: QQYY

### Availability

- **Q121**: A
- **Q420**: A
- **Q221**: A

### Notes

- *A* = Automotive, AEC-Q100 Grade 3: -40°C to +85°C
- *B* = Automotive, AEC-Q100 Grade 2: -40°C to +105°C
- *V* = Industrial, AEC-Q100 Grade 1: -40°C to +85°C
- *I* = Industrial, AEC-Q100 Grade 1: -40°C to +105°C

---

**Legend**

- **S71KL-S**: 65-nm MB, 3.0 V
- **S76HL-T**: 45-nm MB, 3.0 V
- **S78HL-T**: 45-nm MB, 1.8 V
- **S71KS-S**: 65-nm MB, 1.8 V
- **S76HS-T**: 45-nm MB, 1.8 V
- **S78HS-T**: 45-nm MB, 1.8 V

---

**Notes**

- All parts supported by Longevity Program unless noted.
- EOL (Last-Time-Ship)
Package Offerings
# x8 NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>SOIC-16 300 mil</th>
<th>BGA24 8 x 8 mm 5 x 5 Ball</th>
<th>BGA24 8 x 6 mm 5 x 5 Ball</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semper™ Flash</td>
<td>HyperBus™</td>
<td>HS-T¹.²</td>
<td>256Mb</td>
<td>S26HS256T &amp; S28HS256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26HS512T &amp; S28HS512T</td>
<td></td>
<td>✓</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S26HS01GT &amp; S28HS01GT</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S26HS02GT &amp; S28HS02GT</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S26HS04GT &amp; S28HS04GT</td>
<td></td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperFlash</td>
<td></td>
<td>HL-T¹.²</td>
<td>256Mb</td>
<td>S26HL256T &amp; S28HL256T</td>
<td></td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26HL512T &amp; S28HL512T</td>
<td></td>
<td>✓</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S26HL01GT &amp; S28HL01GT</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2Gb</td>
<td>S26HL02GT &amp; S28HL02GT</td>
<td></td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4Gb</td>
<td>S26HL04GT &amp; S28HL04GT</td>
<td></td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>KS-S</td>
<td>128Mb</td>
<td>S26KS128S</td>
<td></td>
<td>✓</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>256Mb</td>
<td>S26KS256S</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26KS512S</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S70KS01GS</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>KL-S</td>
<td>128Mb</td>
<td>S26KL128S</td>
<td></td>
<td>✓</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>256Mb</td>
<td>S26KL256S</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S26KL512S</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>FS-S</td>
<td>256Mb</td>
<td>S79FS256S</td>
<td></td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S79FS512S</td>
<td></td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S79FS01GS</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Quad SPI</td>
<td>QSPI</td>
<td>FL-S</td>
<td>256Mb</td>
<td>S79FL256S</td>
<td>✓</td>
<td>CF</td>
<td>CF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>512Mb</td>
<td>S79FL512S</td>
<td>✓</td>
<td>CF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1Gb</td>
<td>S79FL01GS</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ S26 is HyperBus Interface (xSPI Profile 2.0)
² S28 is Octal Interface (xSPI Profile 1.0)
³ HyperBus Interface
⁴ S28HS02GT available

CF = Contact Factory
UD = Under Development

CF = Contact Factory
UD = Under Development
# x4 NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Interface</th>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>SOIC-8 208 mil</th>
<th>SOIC-16 300 mil</th>
<th>WSON 4 x 4 mm</th>
<th>WSON 6 x 5 mm</th>
<th>WSON 8 x 6 mm</th>
<th>BGA24 8 x 6 mm 5 x 5 Ball</th>
<th>BGA24 8 x 6 mm 4 x 6 Ball</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semper™ Flash</td>
<td>HS-T</td>
<td>256Mb</td>
<td>S25HS256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25HS512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S25HS01GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2Gb</td>
<td>S25HS02GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4Gb</td>
<td>S25HS04GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HL-T</td>
<td>256Mb</td>
<td>S25HL256T</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td>CF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25HL512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S25HL01GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2Gb</td>
<td>S25HL02GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4Gb</td>
<td>S25HL04GT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FL-S</td>
<td>128Mb</td>
<td>S25FL127S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL128S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FL256S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25FL512S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S70FL01GS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FS-S</td>
<td>64Mb</td>
<td>S25FS064S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FS128S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FS256S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>512Mb</td>
<td>S25FS512S</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1Gb</td>
<td>S70FS01GS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FL-P</td>
<td>32Mb</td>
<td>S25FL032P</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>64Mb</td>
<td>S25FL064P</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL128P</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL129P</td>
<td>EOL</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S70FL256P</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FL-L</td>
<td>64Mb</td>
<td>S25FL064L</td>
<td>✓</td>
<td>UD</td>
<td>UD</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>128Mb</td>
<td>S25FL128L</td>
<td>✓</td>
<td>UD</td>
<td>UD</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>256Mb</td>
<td>S25FL256L</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CF** = Contact Factory  
**UD** = Under Development
## Parallel and Burst Parallel NOR Flash Memory Packages

<table>
<thead>
<tr>
<th>Series</th>
<th>Density</th>
<th>Device</th>
<th>48-Ball FBGA (0.8-mm pitch)</th>
<th>48-Ball FBGA (0.5-mm pitch)</th>
<th>56-Ball BGA (0.8-mm pitch)</th>
<th>64-Ball BGA (0.8-mm pitch)</th>
<th>64-Ball Fortified BGA (1.0-mm pitch)</th>
<th>48-Pin TSOP</th>
<th>56-Pin TSOP</th>
<th>80-Ball FBGA (1.0-mm pitch)</th>
<th>80-Pin PQFP</th>
<th>KGD</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL-T</td>
<td>512Mb</td>
<td>S29GL512T</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>S29GL01GT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Gb</td>
<td>S70GL02GT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29GL064S</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29GL128S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29GL256S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>S29GL512S</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>S29GL01GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Gb</td>
<td>S70GL02GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GL-S</td>
<td>64Mb</td>
<td>S29GL064N</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29GL128S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>S29GL256S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>S29GL512S</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>S29GL01GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Gb</td>
<td>S70GL02GS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GL-N</td>
<td>32Mb</td>
<td>S29GL032N</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29GL064N</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29PL127J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PL-J</td>
<td>32Mb</td>
<td>S29PL032J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29PL064J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>S29PL127J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JL-J</td>
<td>32Mb</td>
<td>S29JL032J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>S29JL064J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AL-J</td>
<td>8Mb</td>
<td>S29AL008J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td>S29AL016J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AS-J</td>
<td>16Mb</td>
<td>S29AS016J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CD-J</td>
<td>16Mb</td>
<td>S29CD016J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td>S29CD032J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL-J</td>
<td>16Mb</td>
<td>S29CL016J</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td>S29CL032J</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Flash and RAM Memory MCP Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Flash Density</th>
<th>RAM Density</th>
<th>BGA24 8 x 6 mm, 1.0 mm pitch</th>
<th>BGA24 8 x 8 mm, 1.0 mm pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>S76HS-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td>S78HS-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td>S71KS-S</td>
<td>128Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td>S76HL-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td>S78HL-T</td>
<td>512Mb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>64Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>1Gb</td>
<td>128Mb</td>
<td>CF</td>
<td>CF</td>
</tr>
<tr>
<td>S71KL-S</td>
<td>128Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>256Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
<tr>
<td></td>
<td>512Mb</td>
<td>64Mb</td>
<td>✓</td>
<td>CF</td>
</tr>
</tbody>
</table>

CF = Contact Factory
RAM Automotive Roadmap
Nonvolatile RAM Roadmap

F-RAM™, nvSRAM
# Cypress Roadmaps

## LPC F-RAM

<table>
<thead>
<tr>
<th>F-RAM</th>
<th>Processor Companion</th>
<th>Parallel F-RAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>FM25V20A</td>
<td>2Mb; 2.0–3.6 V</td>
<td>40-MHz SPI; Ind</td>
</tr>
<tr>
<td>CY15B102Q</td>
<td>2Mb; 2.0–3.6 V</td>
<td>25-MHz SPI; Auto E</td>
</tr>
<tr>
<td>FM25V10/VN10</td>
<td>1Mb; 2.0–3.6 V</td>
<td>40-MHz SPI; Ind, Auto A</td>
</tr>
<tr>
<td>FM24V05</td>
<td>512Kb; 2.0–3.6 V</td>
<td>40-MHz SPI; Ind, Auto A</td>
</tr>
<tr>
<td>FM25V02A/W256</td>
<td>256Kb; V02A: 2.0–3.6 V</td>
<td>W256: 2.7–5.5 V</td>
</tr>
<tr>
<td>FM24V02A/W256</td>
<td>256Kb; V02A: 2.0–3.6 V</td>
<td>W256: 2.7–5.5 V</td>
</tr>
<tr>
<td>FM24V01A</td>
<td>128Kb; 2.0–3.6 V</td>
<td>40-MHz SPI; Ind, Auto A</td>
</tr>
<tr>
<td>FM25640B/CL64B</td>
<td>64Kb; 3.3, 5.0 V</td>
<td>20-MHz SPI; Ind, Auto E</td>
</tr>
<tr>
<td>FM25C160/L16</td>
<td>16Kb; 3.3, 5.0 V</td>
<td>20-MHz SPI; Ind, Auto E</td>
</tr>
<tr>
<td>FM25G40/L04</td>
<td>4Kb; 3.3, 5.0 V</td>
<td>20-MHz SPI; Ind, Auto E</td>
</tr>
<tr>
<td>Excelon F-RAM</td>
<td>Up to 16Mb</td>
<td>1.8 V, 108-MHz QSPI</td>
</tr>
<tr>
<td>FM24C64/CL64</td>
<td>64Kb; 3.3, 5.0 V</td>
<td>1-MHz PC; Ind, Auto E</td>
</tr>
<tr>
<td>FM24C16/CL16</td>
<td>16Kb; 3.3, 5.0 V</td>
<td>1-MHz PC; Ind, Auto E</td>
</tr>
<tr>
<td>FM24C04/CL04</td>
<td>4Kb; 3.3, 5.0 V</td>
<td>1-MHz PC; Ind, Auto E</td>
</tr>
<tr>
<td>FM33256</td>
<td>256Kb; 3.3 V; 16-MHz SPI</td>
<td>Ind; RTC; Power Fail; Watchdog; Counter</td>
</tr>
<tr>
<td>FM31256</td>
<td>256Kb; 3.3, 5.0 V</td>
<td>1-MHz PC; Ind; RTC; Power Fail; Watchdog; Counter</td>
</tr>
<tr>
<td>FM3164/31(L)32</td>
<td>64Kb; 3.3, 5.0 V</td>
<td>1-MHz PC; Ind; RTC; Power Fail; Watchdog; Counter</td>
</tr>
</tbody>
</table>

### Attributes

- **Low-pin-count**
- **Ultra-low-energy**
- **Quad serial peripheral interface**
- **AEC-Q001 -40 °C to +85 °C**
- **AEC-Q001 -40 °C to +125 °C**
- **Real-time clock**

###温度等级

- **Industrial grade**
  - 40 °C to +85 °C
- **Automotive**
  - 40 °C to +125 °C

## F-RAM Portfolio

- **Low Power**
- **High Endurance**

## Roadmap

- **Production**
- **Sampling**
- **Concept**
- **Development**
- **Industrial**
- **Automotive**

---

**1. Low-pin-count**

**2. Industrial grade -40 °C to +85 °C**

**3. Ultra-low-energy**

**4. Quad serial peripheral interface**

**5. AEC-Q001 -40 °C to +85 °C**

**6. AEC-Q001 -40 °C to +125 °C**

**7. Real-time clock**
## Excelon™ F-RAM Portfolio

**Ultra Low Power | High Speed | High Endurance**

<table>
<thead>
<tr>
<th>Excelon Auto</th>
<th>Excelon Ultra</th>
<th>Excelon LP</th>
</tr>
</thead>
</table>
| **CY15B116QSN**  
16Mb; 1.8–3.6 V  
24-ball FBGA  
108-MHz QSPI, Auto S | **CY15V116QSN**  
16Mb; 1.71–1.89 V  
24-ball FBGA  
108-MHz QSPI, Ind | **CY15B116QI/N**  
16Mb; 1.71–1.89 V  
24-ball FBGA  
20/40-MHz SPI, Comm, Ind |
| **CY15B116QN**  
16Mb; 1.8–3.6 V  
24-ball FBGA  
40-MHz SPI; Auto A | **CY15V116QN**  
16Mb; 1.71–1.89 V  
24-ball FBGA  
40-MHz SPI; Auto A | **CY15B116QI/N**  
16Mb; 1.71–1.89 V  
24-ball FBGA  
20/40-MHz SPI, Comm, Ind |
| **CY15B108QSN**  
8Mb; 1.8–3.6 V  
24-ball FBGA  
108-MHz QSPI; Auto S | **CY15V108QSN**  
8Mb; 1.71–1.89 V  
24-ball FBGA  
108-MHz QSPI, Ind | **CY15V108QI/N**  
8Mb; 1.71–1.89 V  
24-ball FBGA  
20/40-MHz SPI, Comm, Ind |
| **CY15B108QN**  
8Mb; 1.8–3.6 V  
8-pin SOIC  
50-MHz SPI; Auto E | **CY15V108QN**  
8Mb; 1.71–1.89 V  
8-pin SOIC  
50-MHz SPI; Auto E | **CY15V108QI/N**  
8Mb; 1.71–1.89 V  
8-pin QGQFN  
20/40-MHz SPI, Comm, Ind |
| **CY15B104QN**  
4Mb; 1.8–3.6 V  
8-pin SOIC  
50-MHz SPI; Auto E | **CY15V104QSN**  
4Mb; 1.71–1.89 V  
8-pin SOIC  
50-MHz QSPI, Auto E | **CY15B104QI/N**  
4Mb; 1.71–1.89 V  
8-pin SOIC  
20/50-MHz SPI, Comm, Ind |
| **CY15B104QN**  
4Mb; 1.8–3.6 V  
8-pin SOIC  
50-MHz SPI; Auto A | **CY15V104QN**  
4Mb; 1.71–1.89 V  
8-pin SOIC  
50-MHz SPI; Auto A | **CY15V104QI/N**  
4Mb; 1.71–1.89 V  
8-pin SOIC  
20/50-MHz SPI, Comm, Ind |
| **CY15B102QSN**  
2Mb; 1.8–3.6 V  
8-pin SOIC  
50-MHz SPI; Auto E | **CY15V102QSN**  
2Mb; 1.71–1.89 V  
8-pin SOIC  
108-MHz QSPI, Ind | **CY15B102QI/N**  
2Mb; 1.71–1.89 V  
8-pin SOIC  
50-MHz SPI, Ind |

1 Quad serial peripheral interface  
2 AEC-Q100 -40 °C to +105 °C  
3 Industrial grade -40 °C to +85 °C  
4 Commercial grade 0 °C to +70 °C  
5 AEC-Q100 -40 °C to +85 °C  
6 AEC-Q100 -40 °C to +125 °C

---

220 Cypress Roadmaps
## nvSRAM Portfolio

**High Density | High Speed**

<table>
<thead>
<tr>
<th>Parallel nvSRAM</th>
<th>LPC(^1) nvSRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY14B116R/S</td>
<td>CY14B116F/G</td>
</tr>
<tr>
<td>16Mb; 3.0 V</td>
<td>16Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC(^2)</td>
<td>30 ns; ONFI 1.0 x8, x16, Ind</td>
</tr>
<tr>
<td>CY14B104NA</td>
<td>CY14B108K/L</td>
</tr>
<tr>
<td>4Mb; 3.0 V</td>
<td>8Mb; 3.0 V</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; Ind RTC</td>
</tr>
<tr>
<td>CY14B104K/LA</td>
<td>CY14V104F/G</td>
</tr>
<tr>
<td>1Mb; 3.0 V</td>
<td>1Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; x16, Ind</td>
</tr>
<tr>
<td>CY14B101K/MA</td>
<td>CY14V101MA/NA</td>
</tr>
<tr>
<td>1Mb; 3.0 V</td>
<td>1Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; Ind RTC</td>
</tr>
<tr>
<td>CY14V101LA</td>
<td>CY14V101MA/NA</td>
</tr>
<tr>
<td>1Mb; 3.0 V</td>
<td>1Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; Ind RTC</td>
</tr>
<tr>
<td>CY14V101NA</td>
<td>CY14V101MA/NA</td>
</tr>
<tr>
<td>1Mb; 3.0 V</td>
<td>1Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; Ind RTC</td>
</tr>
<tr>
<td>CY14V101PS</td>
<td>CY14V101PS</td>
</tr>
<tr>
<td>1Mb; 3.0 V</td>
<td>1Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>108-MHz QSPI; Ind Ext. Ind; RTC</td>
</tr>
<tr>
<td>CY14B108M/N</td>
<td>CY14B108M/N</td>
</tr>
<tr>
<td>16Mb; 3.0 V</td>
<td>8Mb; 3.0 V</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; Ind RTC</td>
</tr>
<tr>
<td>CY14B104M/NA</td>
<td>CY14V104F/G</td>
</tr>
<tr>
<td>4Mb; 3.0 V</td>
<td>4Mb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>25, 45 ns; x8; x16, Ind</td>
</tr>
<tr>
<td>CY14B256K/MA</td>
<td>CY14B256K/MA</td>
</tr>
<tr>
<td>512Kb; 3.0 V</td>
<td>256Kb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>35 ns; x8; Ind</td>
</tr>
<tr>
<td>CY14B256F/G</td>
<td>CY14B256F/G</td>
</tr>
<tr>
<td>256Kb; 3.0 V</td>
<td>256Kb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>35 ns; x8; x16, Ind</td>
</tr>
<tr>
<td>CY14B256PA</td>
<td>CY14B256PA</td>
</tr>
<tr>
<td>256Kb; 3.0 V</td>
<td>256Kb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>40-MHz SPI; Ind RTC</td>
</tr>
<tr>
<td>CY14B064PA</td>
<td>CY14B064PA</td>
</tr>
<tr>
<td>64Kb; 3.0 V</td>
<td>64Kb; 3.0, 1.8 V I/O</td>
</tr>
<tr>
<td>25, 45 ns; x8; IndRTC</td>
<td>40-MHz SPI; Ind RTC</td>
</tr>
</tbody>
</table>

\(^1\) Low-pin-count
\(^2\) Industrial grade -40 °C to +85 °C
\(^3\) Real-time clock
\(^4\) Open NAND flash interface
\(^5\) Error-correcting code
\(^6\) Quad serial peripheral interface
\(^7\) Extended Industrial grade -40 °C to +105 °C

- **Industrial**
- **Automotive**
- **Military**
- **Sampling**
- **Development**
- **Production**

221 Cypress Roadmaps
# Nonvolatile RAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>(ES) [EOL]</th>
<th>2020 Q1</th>
<th>2020 Q2</th>
<th>2020 Q3</th>
<th>2020 Q4</th>
<th>2021 Q1</th>
<th>2021 Q2</th>
<th>2021 Q3</th>
<th>2021 Q4</th>
<th>2022 Q1</th>
<th>2022 Q2</th>
<th>2022 Q3</th>
<th>2022 Q4</th>
<th>2023 Q1</th>
<th>2023 Q2</th>
<th>2023 Q3</th>
<th>2023 Q4</th>
<th>2024 Q1</th>
<th>2024 Q2</th>
<th>2024 Q3</th>
<th>2024 Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Excelon F-RAM</td>
<td>Ultra</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Auto</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial F-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPI, I²C</td>
<td>4Kb–4Mb</td>
<td>3.3/5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processor Companion</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I²C</td>
<td>64Kb, 256Kb</td>
<td>3.3/5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel F-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>x8, x16</td>
<td>64Kb–4Mb</td>
<td>3.3/5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel nvSRAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>x8, x16</td>
<td>256Kb–16Mb</td>
<td>3 V, 5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial nvSRAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I²C, SPI, QSPI</td>
<td>64Kb–1Mb</td>
<td>3 V, 5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: CONCEPT [ ], SAMPLES [ ], PRODUCTION [ ], EOL [ ]
2Mb-to-16Mb Excelon™ F-RAM Family

**Applications**
- Medical devices, wearables, industrial control and automation, and automotive

**Features**
- **Excelon Ultra**
  - 2Mb to 16Mb
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - Industrial temperature range grade “I”: -40 °C to +85 °C
- **Excelon Auto**
  - 4Mb to 16Mb Auto “A”, 8Mb to 16Mb Auto “S”, 2Mb to 8Mb Auto “E”
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - 40/50-MHz Serial Peripheral Interface (SPI)
  - Automotive temperature range grade “A”: -40 °C to +85 °C
  - Automotive temperature range grade “S”: -40 °C to +105 °C
  - Automotive temperature range grade “E”: -40 °C to +125 °C
- **Excelon LP**
  - 2Mb to 16Mb
  - 20-MHz SPI (Commercial/Industrial), 40/50-MHz SPI (Industrial)
  - Ultra low (0.75 µA) deep power down current
  - Ultra low (0.1 µA) hibernate current
  - Commercial temperature range grade “C”: 0 °C to +70 °C
  - Industrial temperature range grade “I”: -40 °C to +85 °C
- **Common features for Excelon Ultra/Auto/LP**
  - Operating voltage ranges: 1.71 V to 1.89 V, 1.80 V to 3.60 V
  - 100-trillion read/write cycle endurance
  - 100-year data retention

**Datasheets**: 4Mb Excelon Ultra; 2Mb Excelon Auto; 8Mb Excelon LP

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>Standby Current (Typ.)</th>
<th>Active Current (Typ.)</th>
<th>Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Mb</td>
<td>2.3 µA</td>
<td>2.4 mA</td>
<td>SOIC (8), TDFN (8)</td>
</tr>
<tr>
<td>4Mb</td>
<td>2.3 µA</td>
<td>2.4 mA</td>
<td>SOIC (8), GQFN (8)</td>
</tr>
<tr>
<td>8Mb</td>
<td>3.5 µA</td>
<td>2.6 mA</td>
<td>SOIC (8), GQFN (8)</td>
</tr>
<tr>
<td>16Mb</td>
<td>7.3 µA</td>
<td>3.0 mA</td>
<td>FBGA (24)</td>
</tr>
</tbody>
</table>

**Availabilty**

**Sampling**: Now (2Mb Ind), Q420 (8Mb Auto S, 16Mb)
**Production**: Now (2Mb Auto E, 4Mb Auto A/Ultra/LP & 8Mb LP), Q220 (2Mb Ind), Q221 (16Mb, 8Mb Auto S)

1 Quad SPI has 4 I/Os
# F-RAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>8-pin SOIC</th>
<th>8-pin DFN</th>
<th>8-pin GQFN</th>
<th>8-pin EIAJ</th>
<th>14-pin SOIC</th>
<th>28-pin SOIC</th>
<th>28-pin TSOP I</th>
<th>32-pin TSOP I</th>
<th>44-pin TSOP II</th>
<th>24-ball FBGA</th>
<th>48-ball FBGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI 4Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC 4Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>512Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processor</td>
<td>64Kb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Companion</td>
<td>256Kb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel 64Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2Mb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4Mb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# nvSRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>8-pin SOIC</th>
<th>8-pin DFN</th>
<th>16-pin SOIC</th>
<th>28-pin SOIC</th>
<th>28-pad CDIP</th>
<th>28-pad LCC</th>
<th>32-pin SOIC</th>
<th>44-pin TSOP II</th>
<th>48-ball FBGA</th>
<th>48-pin SSOP</th>
<th>48-pin TSOP I</th>
<th>54-pin TSOP II</th>
<th>60-ball FBGA</th>
<th>165-ball FBGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SPI</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PC</td>
<td>64Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>256Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Parallel Asynchronous SRAM Roadmap

Low-Power (MoBL®), Fast, PowerSnooze™
# Parallel Asynchronous SRAM Portfolio

## High Density | Wide Voltage Range | Automotive A¹, E² | On-Chip ECC

<table>
<thead>
<tr>
<th>Density</th>
<th>Fast SRAM</th>
<th>Low-Power SRAM (MoBL®³)</th>
<th>PowerSnooze™⁴</th>
</tr>
</thead>
<tbody>
<tr>
<td>64Kb–1Mb</td>
<td>CY7C102x</td>
<td>CY6218x 64Mb: 1.8, 3.0 V 55 ns; x16 Ind</td>
<td>CY6216x 64Mb: 3.0 V 55 ns; x16 Ind</td>
</tr>
<tr>
<td></td>
<td>CY62256</td>
<td>CY6218x 64Mb: 1.8, 3.0 V 55 ns; x16 Ind</td>
<td>CY6216x 64Mb: 1.8-5.0 V 55 ns; x16 Ind</td>
</tr>
<tr>
<td>2Mb–16Mb</td>
<td>CY7C1010/11</td>
<td>CY6216x 16Mb: 1.8, 3.0, 5.0 V 45 ns; x8, x16, x32 Ind, Auto A, E</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td></td>
<td>CY7C1019/21/100x</td>
<td>CY6216x 16Mb: 1.8, 3.0, 5.0 V 45 ns; x8, x16, x32 Ind, Auto A, E</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td>32Mb–64Mb</td>
<td>CY7C100x</td>
<td>CY6216x 16Mb: 1.8, 3.0, 5.0 V 45 ns; x8, x16, x32 Ind, Auto A, E</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td></td>
<td>CY7C106x</td>
<td>CY6216x 16Mb: 1.8-5.0 V 55 ns; x16 Ind</td>
<td>CY6216x 16Mb: 3.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td></td>
<td>CY7100x</td>
<td>CY6216x 16Mb: 1.8, 3.0, 5.0 V 45 ns; x8, x16, x32 Ind, Auto A, E</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td></td>
<td>CY7C107x</td>
<td>CY6216x 16Mb: 1.8-5.0 V 55 ns; x16 Ind</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
<tr>
<td></td>
<td>CY7C109x</td>
<td>CY6216x 16Mb: 1.8, 3.0, 5.0 V 45 ns; x8, x16, x32 Ind, Auto A, E</td>
<td>CY6216x 16Mb: 1.8-5.0 V 45 ns; x8, x16, x32 Ind</td>
</tr>
</tbody>
</table>

1 AEC-Q100 -40 °C to +85 °C 2 AEC-Q100 -40 °C to +125 °C 3 More Battery Life 4 A Fast SRAM with a deep-sleep mode in addition to the conventional standby 5 Ultra-Low-Power
# Parallel Asynchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td>MoBL SRAM ULP</td>
<td>65 nm, ECC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel Asynchronous</td>
<td>8Mb,</td>
<td>Q1, Q2, Q3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb, 32Mb, 64Mb</td>
<td>Q4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MoBL SRAM</td>
<td>65 nm, ECC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel Asynchronous</td>
<td>4Mb, 8Mb, 16Mb</td>
<td>Q1, Q2, Q3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MoBL SRAM ≥ 90 nm</td>
<td>Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PowerSnooze SRAM</td>
<td>65 nm, ECC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel Asynchronous</td>
<td>4Mb, 16Mb</td>
<td>Q1, Q2, Q3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fast SRAM</td>
<td>65 nm, ECC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel Asynchronous</td>
<td>2Mb, 4Mb, 8Mb, 16Mb</td>
<td>Q1, Q2, Q3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fast SRAM ≥ 90 nm</td>
<td>Parallel Asynchronous</td>
<td>64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Low-Power SRAM Family with ECC

Applications
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers, and automotive

Features
- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16, and x32
- **Low Power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC\(^1\) logic to detect and correct single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS\(^2\)-Compliant Packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

Collateral
Datasheet: Asynchronous SRAM with ECC

SRAM with ECC

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Standby Current (Maximum at 85 °C)</th>
<th>Standby Current (Typical at 25 °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY6214x</td>
<td>8.7 µA</td>
<td>3.5 µA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY6215x</td>
<td>16.0 µA</td>
<td>5.5 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY6216x</td>
<td>16.0 µA</td>
<td>5.5 µA</td>
</tr>
</tbody>
</table>

Availability
Production: Now

Notes:
1. Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2. Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
Ultra Low-Power MoBL®1 SRAM Family with ECC²

Applications
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, automotive, and computation servers

Features
- **Speed**
  - Access time: 45/55 ns
  - Bus-width configurations: x8 and x16
- **Low Power**
  - Standby current: 8.0 µA max for 16Mb
- **Operating Voltage Range**
  - 2.2 V to 3.6 V, 1.65V to 2.25V (8Mb)
- **Features**
  - ECC² logic to detect and correct single-bit errors
- **Temperature Grades**
  - 8Mb, 16Mb, 32Mb, 64Mb; Industrial grade: -40 °C to +85 °C
  - 8Mb; Automotive A grade: -40 °C to +85 °C
  - 8Mb; Automotive E grade: -40 °C to +125 °C
- **RoHS³-compliant Packages**
  - All existing MoBL packages supported

Collateral
Datasheet: 64Mb contact sales; 32Mb contact sales
16Mb ULP SRAM; 8Mb contact sales

SRAM with ECC

Family Table
<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Standby Current (Maximum at 85 C)</th>
<th>Standby Current (Typical at 25 C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Mb</td>
<td>CY6215x</td>
<td>6.5 µA</td>
<td>1.4 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY6216x</td>
<td>8.0 µA</td>
<td>1.5 µA</td>
</tr>
<tr>
<td>32Mb</td>
<td>CY6217x</td>
<td>19.0 µA</td>
<td>3.0 µA</td>
</tr>
<tr>
<td>64Mb</td>
<td>CY6218x</td>
<td>38.0 µA</td>
<td>6.0 µA</td>
</tr>
</tbody>
</table>

Availability
Production: Now

---
1 MoBL: More Battery Life
2 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
3 Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components
Fast SRAM Family with PowerSnooze™

**Applications**
Programmable logic controllers, handheld devices, multifunction printers, computation servers, and automotive

**Features**

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16, and x32

- **Low Power**
  - Deep-sleep current: 15 µA for 4Mb

- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors

- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades

- **RoHS-compliant Packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

**Collateral**

- Datasheet: Asynchronous SRAM with ECC

---

1 A Fast SRAM with a deep sleep mode in addition to a conventional standby mode
2 Error-correcting code
3 Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

---

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (Maximum at 85 °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>10 ns</td>
<td>15 µA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>10 ns</td>
<td>22 µA</td>
</tr>
</tbody>
</table>

**Availability**

- **Production:** Now
Fast SRAM Family with ECC

**Applications**
- Switches and routers, IP phones, test equipment, computation servers, automotive, military, and aerospace systems

**Features**
- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16, and x32
- **Features**
  - ECC logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Multiple Operating Temperatures**
  - Industrial and automotive temperature grades
- **RoHS²-compliant Packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

**Collateral**
- Datasheet: [Asynchronous SRAM with ECC](#)

---

1 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2 Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

---

**SRAM with ECC**

**Family Table**

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Operating Current (Maximum at 85 °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7C104x</td>
<td>10 ns</td>
<td>45 mA</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY7C105x</td>
<td>10 ns</td>
<td>110 mA</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7C106x</td>
<td>10 ns</td>
<td>110 mA</td>
</tr>
</tbody>
</table>

**Availability**

Production: Now
## Parallel Asynchronous SRAM Packages

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast</td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>512Kb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-Power</td>
<td>256Kb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>16Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
HyperRAM Roadmap

High-performance Pseudo-static RAM
## HyperRAM™ Portfolio

<table>
<thead>
<tr>
<th>Density</th>
<th>Initial Access</th>
<th>DDR Clock</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64Mb</td>
<td>36 ns/100 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>36 ns/166 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td></td>
<td>128Mb</td>
<td>35 ns/166 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td></td>
<td>64Mb</td>
<td>35 ns/200 MHz</td>
<td>I, A, V, B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>35 ns/200 MHz</td>
<td>I, A, V, B</td>
</tr>
</tbody>
</table>

|          | 128Mb 1       | 35 ns/200 MHz | I, A, V, B        |
|          |                |              |                   |

|          | 64Mb           | 35 ns/200 MHz | I, A, V, B        |
|          |                |              |                   |

|          | 128Mb 1       | 35 ns/200 MHz | I, A, V, B        |
|          |                |              |                   |

### Notes:
- Industrial: -40 °C to +85 °C
- Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C
- Industrial-plus: -40 °C to +105 °C
- Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C

1 Stacked die

---

235 Cypress Roadmaps
## HyperRAM™ Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>S27KS-1 (1.8 V)</td>
<td>128Mb^1</td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KL-1 (3.0 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperRAM 1.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63-nm PS-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KS-2/3 (1.8 V)</td>
<td>128Mb^1</td>
<td>64Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S27KL-2/3 (3.0 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HyperRAM 2.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>38-nm PS-RAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

^1 Stacked die

Products supported by Longevity Program unless noted

- **Concept**
- **Production**
- **Samples**
- **EOL - LTB**
- **EOL - LTS**
Synchronous SRAM Roadmap

Std Sync, NoBL®, QDR-II, DDR-II, QDR-IV
Synchronous SRAM Portfolio

High Random Transaction Rate (RTR) | Low Latency | High Bandwidth

<table>
<thead>
<tr>
<th>Standard Sync and NoBL (Ref.)</th>
<th>Standard Sync and NoBL with ECC (Ref.)</th>
<th>QDR®-II/DDR-II</th>
<th>QDR-II+/DDR-II+</th>
<th>QDR-II+X/DDR-II+X</th>
<th>QDR-IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes</td>
<td>RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes</td>
<td>RTR: 666 MT/s (max.) BW: 47.8 Gbps (max.) Latency: 1.5 Cycles CIO® and SIO®</td>
<td>RTR: 666 MT/s (max.) BW: 79.2 Gbps (max.) Latency: 2 or 2.5 Cycles CIO and SIO, ODT®</td>
<td>RTR: 900 MT/s (max.) BW: 91.1 Gbps (max.) Latency: 2.5 Cycles SIO, ODT</td>
<td>RTR: 2.1 GT/s (max.) BW: 153.5 Gbps (max.) Latency: 5 or 8 Cycles Dual-Port Bidirectional ODT</td>
</tr>
<tr>
<td>CY7C147/8xB 72Mb; 133–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C144/6xK 36Mb; 133–250 MHz 2.5, 3.3 V; x36, x72</td>
<td>CY7C1611/2xKV18 144Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C1511/2xKV18 72Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C156/7xKV18 72Mb; 366–633 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C411xKV13 144Mb; 667–1,066 MHz 1.3 V; x18, x36 Burst 2</td>
</tr>
<tr>
<td>CY7C144/6xKVE 36Mb; 133–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C1411/2xKV18 36Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C141/2xKV18 36Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C54/5/6/7xKV18 72Mb; 250–550 MHz 1.8 V; x18, x36 RHA; Burst 2, 4</td>
<td>CY7C54/5/6/7xKV18 36Mb; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4</td>
<td>CY7C40xKV13 72Mb; 667–1,066 MHz 1.3 V; x18, x36 Burst 2</td>
</tr>
<tr>
<td>CY7C137/8xD/K 18Mb; 100–250 MHz 3.3 V; x18, x32, x36</td>
<td>CY7C137/8xKVE 18Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C131/2/9xKV18 18Mb; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C19111xKV18 18Mb; 250–333 MHz 1.8 V; x9 Burst 2, 4</td>
<td>CY7C126/7x 36Mb; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4</td>
<td>CY7C126/7xKV18 36Mb; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4</td>
</tr>
<tr>
<td>CY7C135/6xC 9Mb; 100–250 MHz 3.3 V; x18, x32, x36 Auto E®</td>
<td>CY7C135/6xKVE 9Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C135/6xKVE 9Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C135/6xKVE 9Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C124/5/6/7xKV18 18Mb; 400–550 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C135/6xKV13 144Mb; 667–1,066 MHz 1.3 V; x18, x36 Burst 2</td>
</tr>
<tr>
<td>CY7C134/2xG 2–4Mb; 100–250 MHz 3.3 V; x18, x32, x36</td>
<td>CY7C134/2xGVE 2–4Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C134/2xGVE 2–4Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C134/2xGVE 2–4Mb; 100–250 MHz 2.5, 3.3 V; x18, x36</td>
<td>CY7C124/5/6/7xKV18 18Mb; 400–550 MHz 1.8 V; x9, x18, x36 Burst 2, 4</td>
<td>CY7C134/2xG 2–4Mb; 100–250 MHz 3.3 V; x18, x32, x36</td>
</tr>
</tbody>
</table>

1 Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
2 Error-correcting code
3 Common I/O
4 Separate I/O
5 On-die termination
6 Radiation hardened, military grade
7 AEC-Q100: -40 °C to +125 °C

CY7C147/8xB
72Mb; 133–250 MHz 2.5, 3.3 V; x18, x36

CY7C144/6xK
36Mb; 133–250 MHz 2.5, 3.3 V; x36, x72

CY7C137/8xD/K
18Mb; 100–250 MHz 3.3 V; x18, x32, x36

CY7C135/6xC
9Mb; 100–250 MHz 3.3 V; x18, x32, x36 Auto E®

CY7C134/2xG
2–4Mb; 100–250 MHz 3.3 V; x18, x32, x36

Random Transaction Rate

Cypress Roadmaps

238 Cypress Roadmaps
## Synchronous SRAM Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Density (Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
</tr>
<tr>
<td>QDR®-IV SRAM 65 nm, ECC 2.1 GT/s, 153.5 Gbps</td>
<td>72Mb, 144Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-II+X SRAM 65 nm, ECC 900 MT/s, 91.1 Gbps</td>
<td>36Mb, 72Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-II+ SRAM 65 nm, ECC 666 MT/s, 79.2 Gbps</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>QDR-II SRAM 65 nm 666 MT/s, 47.9 Gbps</td>
<td>18Mb, 36Mb, 72Mb, 144Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync and NoBL® SRAM 65 nm, ECC 250 MT/s, 18 Gbps</td>
<td>18Mb, 36Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync and NoBL SRAM 65 nm/90 nm 250 MT/s, 18 Gbps</td>
<td>2Mb, 4Mb, 9Mb, 18Mb, 36Mb, 72Mb</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Radiation hardened, military grade
2 AEC-Q100 -40 °C to +125 °C
3 65-nm

QDR® and NoBL® are trademarks of Cypress Semiconductor Corporation.
Standard Synchronous SRAM With On-Chip ECC¹

Applications
Switches and routers, radar and signal processing, test equipment, automotive, military, and aerospace systems

Features
- **Speed**
  - Available in two modes²: Pipeline and Flow-Through
  - Bus widths: x18 and x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options³
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral
Datasheets: 36M Sync SRAM, 18M Sync SRAM

Synchronous SRAM

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with On-Chip ECC Pipeline</td>
<td>18Mb</td>
<td>CY7C1370/2K</td>
<td>250 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>36Mb</td>
<td>CY7C1440/2K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync with On-Chip ECC Flow-Through</td>
<td>18Mb</td>
<td>CY7C1371/3K</td>
<td>133 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>36Mb</td>
<td>CY7C1441/3K</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Availability
Production: Now

¹ Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
² Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
³ Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
⁴ The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data
NoBL® SRAM With On-Chip ECC

Applications
Switches and routers, radar and signal processing, test equipment, automotive, military, and aerospace systems

Features
- **Speed**
  - Available in two modes: Pipeline and Flow-Through
  - No Bus Latency™ (NoBL) architecture for balanced read and write
  - Bus widths: x18 and x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral
Datasheets: 36M NoBL SRAM, 18M NoBL SRAM

Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb*</th>
</tr>
</thead>
<tbody>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
<td>CY7C1380/2K</td>
<td>250 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Pipeline</td>
<td>36Mb</td>
<td>CY7C1460/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NoBL with On-Chip ECC</td>
<td>18Mb</td>
<td>CY7C1381/3K</td>
<td>133 MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Flow-Through</td>
<td>36Mb</td>
<td>CY7C1461/3K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
2 Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
3 Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
4 The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

Availability
Production: Now
## Synchronous SRAM Packages

<table>
<thead>
<tr>
<th>Family</th>
<th>Density</th>
<th>100-pin TQFP</th>
<th>119-ball BGA</th>
<th>165-ball BGA</th>
<th>209-ball BGA</th>
<th>361-ball BGA</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Std Sync</td>
<td>18Mb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NoBL</td>
<td>2Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4Mb</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>9Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>QDR</td>
<td>9Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>72Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>144Mb</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
PMIC Automotive Roadmap
Automotive PMIC Family Portfolio

<table>
<thead>
<tr>
<th>Single-channel PMIC</th>
<th>Multi-Channel PMIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S6BP203A</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{out}$: 3.3V 2.4A, 2-MHz Buck-Boost, 16-Pin TSSOP</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP202A</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{out}$: 5.0V (2.4A), 2-MHz Buck-Boost, PG, 16-Pin TSSOP</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP201A</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{out}$: 5.0V (1.0A), 2-MHz Buck-Boost, PG, 16-Pin TSSOP</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP502A</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{out}$: 5.0V / 3.3 / 1.1V (2.0A), 400-kHz Buck, 2-MHz Buck, 2-MHz Boost, PG, SSCG, HOT, 32-Pin wettable QFN</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP501A</strong></td>
<td></td>
</tr>
<tr>
<td>$V_{out}$: 5.0V / 3.3 / 1.1V (1.4A), 400-kHz Buck, 2-MHz Buck, 2-MHz Boost, PG, SSCG, HOT, 32-Pin wettable QFN</td>
<td></td>
</tr>
<tr>
<td><strong>S6BP401A</strong></td>
<td></td>
</tr>
<tr>
<td>5V → six output rails, 2-MHz Buck x4, LDO x2, PG, WDT, 40-Pin QFN</td>
<td></td>
</tr>
</tbody>
</table>

1. Lead-acid battery whose typical voltage is 12V.
2. Topology to supply stable output regardless of input variation.
3. Power-Good signal output.
4. Step-down voltage regulator.
5. Step-up voltage regulator.
6. Spread-spectrum clock generator which deliberately varies the internal clock signal frequency to lower the electromagnetic radiation.
7. Hard pin output that indicates the die is getting hot.
8. QFN packages whose pin is processed so that the solder fillet would form between the pin and pad.
S6BP20xA
One-Channel Buck-Boost Automotive PMIC

Applications
Instrument clusters, body electronics and ADAS

Features
- **1-Channel PMIC**: Synchronous buck-boost converter
- **Wide Input Voltage Range**: 2.5–42 V
- **Low Quiescent Current**: 20 μA
- **Programmable Switching Frequency**: 0.2–2.1 MHz
  - Synchronization with external clock from 200 kHz to 400 kHz
  - Autonomous PFM/PWM\(^1\) switching
- **BOM Integration**: Built-in switching transistors
- **System Safety Function\(^2\) Support**:
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with power good\(^3\) pin
- **Operating Temperature Range**: -40°C to +125°C
- **Package**: 16-pin thermally enhanced TSSOP (5-mm x 6.4-mm)
- **Qualification**: AEC-Q100 Grade-1

Collateral
- **Datasheet**: S6BP201A, S6BP202A and S6BP203A
- **Evaluation Kit**: S6BP201A, S6BP202A and S6BP203A

Family Table

<table>
<thead>
<tr>
<th>Output Voltage(^*)</th>
<th>Max. Output Current</th>
<th>MPN</th>
<th>UVP/OVP Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0–5.2 V</td>
<td>1.0 A</td>
<td>S6BP201A</td>
<td>±4.5%</td>
</tr>
<tr>
<td>5.0–5.2 V</td>
<td>2.4 A</td>
<td>S6BP202A</td>
<td>±4.5%, ±8.0%</td>
</tr>
<tr>
<td>3.3 V</td>
<td>2.4 A</td>
<td>S6BP203A</td>
<td>±8.0%</td>
</tr>
</tbody>
</table>

\(^1\) Pulse-frequency modulation / pulse-width modulation
\(^2\) A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
\(^3\) An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
\(^*\) S6BP201A and S6BP202A have factory-selectable options of output voltage, power-on-reset time, UVP/OVP threshold, and SYNC Function

Availability
- **Sampling**: Now
- **Production**: Now
S6BP50xA
Three-Channel Automotive PMIC

Applications
Low-end to mid-range hybrid automotive cluster systems

Features
- **3-Channels**: Buck controller with load switch, boost converter, buck converter
- **Wide Range Input**: 2.5–42 V
- **Low Quiescent Current**: 15 µA
- **High Switching Frequency**:
  - Boost converter and buck converter: 2.1 MHz
  - Built-in spread-spectrum clock generator (SSCG)
  - Synchronization with external clock from 1.8–2.4 MHz
- **System Safety Function**¹ Support:
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Thermal warning
  - Window-monitoring voltage supervisors with independent power good² pins
- **Operating Temperature Range**: -40°C to +105°C
- **Package**: 32-pin thermally enhanced side-wettable³ QFN (5-mm x 5-mm)
- **Qualification**: AEC-Q100 Grade-2

Collateral
- Preliminary Datasheet: S6BP501A/S6BP502A
- Evaluation Kit: S6SBP501A00VA1001/S6SBP502A00VA1001

¹ A set of system functions that protect ECU’s from damage and/or from generating erroneous results during abnormal power supply conditions
² An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
³ QFN packages whose pin is processed so that the solder fillet would form between the pin and pad

Family Table

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1.15 V, 1.4 A</td>
<td>S6BP501A</td>
<td>3.3 V, 1.6 A</td>
<td>5.0 V, 1.3 A</td>
</tr>
<tr>
<td>1.2 V, 2.0 A</td>
<td>S6BP502A</td>
<td>3.3 V, 1.9 A</td>
<td>5.0 V, 1.3 A</td>
</tr>
</tbody>
</table>

Availability
- **Sampling**: Now
- **Production**: Now
S6BP401A
Six-Channel Automotive PMIC

Applications
Advanced driver assistance systems (ADAS), security camera systems

Features
- **6-Channel PMIC**: 4-channel buck converters, 2-channel LDOs
- **Input Voltage Range**: 4.5–5.5 V
  - Input voltage for LDO: 1.62–5.5 V
- **High Switching Frequency**: 2.1 MHz
  - Synchronization with external clock from 1.8–2.4 MHz
- **BOM Integration**:
  - Switching transistors, voltage setting resistors, and compensation circuitry
- **System Safety Function**
  - Overvoltage protection (OVP), overcurrent protection (OCP), undervoltage lock-out (UVLO), thermal shutdown (TSD)
  - Window-monitoring voltage supervisors with independent power good pins
  - Built-in windowed watchdog timer (WDT)
  - Independent enable pins
- **Operating Temperature Range**: -40°C to +125°C
- **Package and Qualification**: 40-pin QFN (6-mm x 6-mm), AEC-Q100 Grade-1

Datasheet: S6BP401A
Evaluation Kit: S6SBP401AJ0SA1001, S6SBP401AM2SA1001

1 A set of system functions that protect ECUs from damage and/or from generating erroneous results during abnormal power supply conditions
2 An output signal that PMICs provide to signify that the supplied power by PMICs is proper and ready
3 S6BP401A has factory-selectable options of output voltage for each channel

Availability
Sampling: Now  Production: Now

DC/DC Converter: 4.5-5.5 V
LDO: 2.97-5.5 V

Enable for 6-Channel
1.8 V, Enable
Oscillator, External Sync
External Clock for Synchronization
Trigger Input
Windowed Watchdog Timer
Power Good
Power Good for 5-ch (Except LDO1)

Buck Converter 2.1 MHz (DC/DC 1)
Buck Converter 2.1 MHz (DC/DC 2)
Buck Converter 2.1 MHz (DC/DC 3)
Buck Converter 2.1 MHz (DC/DC 4)
LDO 1
LDO 2
Protection Function

S6BP401A: Six-Channel Automotive PMIC
## Compatibility with Traveo™ MCU

<table>
<thead>
<tr>
<th>Traveo MCU for Instrument Cluster</th>
<th>S6J3120</th>
<th>✔</th>
<th>✔</th>
<th>✔</th>
<th>✔</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S6J3300</td>
<td>✔</td>
<td>✔</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>S6J3300</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>S6J3200</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Traveo MCU for Body Control</th>
<th>S6J3110</th>
<th>✔</th>
<th>✔</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S6J3400</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>S6J3500</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td></td>
<td>S6J3350</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>
Timing Solutions Automotive Roadmap
## Clock Synthesizer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27430</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 Outputs; Diff &amp; SE; PCIe 3.0;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCXO2; EMI; 0.7-ps RMS Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.8 V/2.5 V/3.3 V; Ind; 48-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY27410</td>
<td>4-PLL; Maximum Frequency: 700 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8 Outputs; Diff &amp; SE; PCIe 3.0;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCXO; EMI; 0.7-ps RMS Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.8 V/2.5 V/3.3 V; Auto A S; 48-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCY254x/CY251x</td>
<td>1-4 PLL; Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3-9 Outputs; I2C; EMI; Low Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100-ps CCJ/Ind: 1.8 V/2.5 V/3.0 V/3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8-SOIC; 8/16/20-TSSOP; 48-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Maximum Frequency: 166 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3-8 Outputs; CMOS; Low Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>200-ps PPJ; VCXO; Ind: 3.3 V/5 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8/16/20-SOIC; 16-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2429x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-5 Outputs; HCSL, CMOS; EMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>75-ps CCJ; PCIe 1.1; Ind; Auto A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3 V; 16-TSSOP; 32-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2239x</td>
<td>3-4 PLL; Maximum Frequency: 400 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5-8 Outputs; LVPECL, CMOS; I2C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>400-ps PPJ; VCXO; 3.3 V Ind; Auto A E1; 16-TSSOP; 32-QFN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-3 Outputs; CMOS; EMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY22050/150</td>
<td>1-PLL; Maximum Frequency: 200 MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6 Outputs; CMOS; I2C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>250-ps PPJ; Ind 2.5 V/3.3 V; 16-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Differential and single-ended outputs
2 Voltage Controlled Crystal Oscillation
3 Electromagnetic interference reduction using Lexmark profile
4 Integrated phase noise across 12-kHz to 20-MHz offset
5 Industrial grade: -40°C to +85°C
6 AEC-Q100: -40°C to +85°C
7 AEC-Q100: -40°C to +105°C
8 Power Management options
9 Cycle-to-cycle Jitter
10 Peak-to-peak period Jitter
11 AEC-Q100: -40°C to +125°C

Products supported by Longevity Program unless noted
- Concept
- Production
- EOL - LTB
- EOL - LTS

250 Cypress Roadmaps
# Clock Buffer Roadmap

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2DPx/CPx</td>
<td>Maximum Frequency: 1.5 GHz 2–10 Outputs; LVPECL; 2.5 V/3.3 V 0.11-ps Additive Jitter(^1); Ind(^2) 820-TSSOP; 8-SOIC; 32-TQFP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY2DMx/DLx</td>
<td>Maximum Frequency: 1.5 GHz 2–10 Outputs; LVDS, CML; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 820-TSSOP; 32-TQFP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY230x/EP0x (Zero Delay)</td>
<td>Maximum Frequency: 220 MHz 2–9 Outputs; LVCMOS; 2.5 V/3.3 V/5 V 22-ps CCJ; Ind; Auto A(^4) 8/16-SOIC; 16-TSSOP; WAFER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY230xNZ/2994x (Non-Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4–18 Outputs; LVCMOS 100-ps Cjit-Op Skew; Ind 2.5 V/3.3 V; 8-TSSOP, 16-SOIC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY23FS04/08/FP12 (Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4–12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5 V/3.3 V 16/28-SSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY23S0x (Zero Delay)</td>
<td>Maximum Frequency: 133 MHz 5–9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind; 2.5 V/3.3 V; 8/16-SOIC; 16-TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CY7B99x (RoboClock™)</td>
<td>Maximum Frequency: 200 MHz; 8–13 Outputs Configurable Skew; 2.5 V/3.3 V/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) Additive RMS Phase Jitter  
\(^2\) Industrial grade: -40°C to +85°C  
\(^3\) Cycle-to-cycle Jitter  
\(^4\) AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted
### Timing Solutions Portfolio

#### Programmable | High-Performance | EMI Reduction | Automotive

#### Clock Synthesizers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY27410</td>
<td>4-PLL; Max Freq: 700 MHz 12 Outputs; Dif&amp;SE; PCIe 3.0 VXCO; EMI: 0.7-ps RMS Jitter; &lt;200 ppm phase noise</td>
</tr>
<tr>
<td>CY24940</td>
<td>1-PLL; Max Freq: 2.1 GHz 1 Output; Dif &amp; SE; 40/100 GbE VXCO; 0.11-ps RMS Jitter; Ind</td>
</tr>
<tr>
<td>CY254xs/CY251x</td>
<td>1-4 PLL; Max Freq: 200 MHz 3-9 Outputs; PC; EMI; Low Power; 100-ps CCJ; Ind</td>
</tr>
<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Max Freq: 166 MHz 3-8 Outputs; CMOS; Low Power 200-ps PJ; VXCO; 3.3 V; Ind; Auto A 3.3 V; 16-TSSOP; 16-QFN</td>
</tr>
<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Max Freq: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VXCO; Ind 3.3 V; 8-SOIC; 8-TSSOP</td>
</tr>
<tr>
<td>CY22050/150</td>
<td>1-PLL; Max Freq: 200 MHz 6 Outputs; CMOS; PC 250-ps PJ; 2.5/3.3 V; 16-TSSOP</td>
</tr>
</tbody>
</table>

#### Oscillators

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2941x/2x</td>
<td>1-PLL; Max Freq: 2.1 GHz 1 Output; Dif &amp; SE; 40/100 GbE VXCO; 0.11-ps RMS Jitter; Ind 1.8 V/2.5 V/3.3 V; Auto A 5°; 48-QFN</td>
</tr>
<tr>
<td>CY51x7</td>
<td>1-PLL; Max Freq: 2.1 GHz 1 Output; Dif &amp; SE; 40/100 GbE VXCO; 0.11-ps RMS Jitter; Ind 1.8 V/2.5 V/3.3 V; WAFA/DIE</td>
</tr>
<tr>
<td>CY229x (FlexO™)</td>
<td>1 PLL; Max Freq: 690 MHz 1 Output; LVCMOS, LVDS, LVPECL 0.6-ps RMS Jitter; Ind 5 Outputs; LVCMOS; 2.5/3.3 V</td>
</tr>
<tr>
<td>CY25701</td>
<td>1-PLL; Max Freq: 166 MHz 1 Output; CMOS; EMI 85-ps CCJ; Ind 3.3 V; 3.3 V; 40/100 GbE 3.3 V; 40-180 ps CCJ; 8/16-TSSOP; 16-TSSOP</td>
</tr>
<tr>
<td>CY5077</td>
<td>1-PLL Max Freq: 166 MHz 1 Output; CMOS 75-ps CCJ; Ind 1.8/2.5/3.0/3.3 V; WAFA</td>
</tr>
<tr>
<td>CY5057</td>
<td>1-PLL Max Freq: 170 MHz 1 Output; CMOS; EMI &lt;200-ps CCJ; Ind 3.3/5.0 V; WAFA</td>
</tr>
<tr>
<td>CY2350x (Zero Delay)</td>
<td>Max Freq: 200 MHz 5-9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind 2.5/3.3 V; 8/16-SOIC; 16-TSSOP</td>
</tr>
</tbody>
</table>

#### Clock Buffers

<table>
<thead>
<tr>
<th>Model</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2Dpx/CpX</td>
<td>Max Freq: 1.5 GHz 2-10 Outputs; LVPECL; 2.5/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 8-SOIC; 32-TQFP</td>
</tr>
<tr>
<td>CY2DMx/DCx</td>
<td>Max Freq: 1.5 GHz 2-10 Outputs; LVDS, CM; 2.5/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP</td>
</tr>
</tbody>
</table>

### Notes
1. Differential and single-ended outputs
2. Voltage Controlled Crystal Oscillation
3. Electromagnetic interference reduction using Lexmark profile
4. Integrated phase noise across 12-kHz to 20-MHz offset
5. Industrial grade: -40°C to +85°C
6. AEQ-C100: -40°C to +85°C
7. AEQ-C100: -40°C to +105°C
8. Additive RMS phase jitter
9. Power Management options
10. Cycle-to-cycle jitter
11. Peak-to-peak period jitter
12. AEQ-C100: -40°C to +125°C

### Status Availability
- Concept
- Development
- Sampling
- Production
- EOL
# CY27430: High-Performance 4-PLL Clock Generator

## Applications
- Car infotainment and navigation systems

## Features
- **Eight Outputs**
  - Four configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0, and 10 GbE
  - AEC Q-100 qualified (-40°C to +105°C)
- **Additional Features**
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency select
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-Compliant Package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

## Collateral
- Preliminary Datasheet: [Contact Sales](mailto:sales@cypress.com)

## Availability
- Production: Now

---

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eight Outputs</td>
<td>Four configurable (differential or single-ended), Four single-ended</td>
</tr>
<tr>
<td>Specifications</td>
<td>High frequency: 700-MHz differential, 250-MHz single-ended, RMS phase jitter &lt;0.7 ps (typical), Reference clock support for PCIe 3.0, SATA 2.0, and 10 GbE, AEC Q-100 qualified (-40°C to +105°C)</td>
</tr>
<tr>
<td>Additional Features</td>
<td>Pin select and I²C programming, Configurable as zero or non-zero delay buffer, Glitch-free frequency switching, Frequency select, Early/late clocks, PLL cascading, Voltage-controlled frequency synthesis (VCFS)</td>
</tr>
<tr>
<td>RoHS-Compliant Package</td>
<td>Available in a 7 mm x 7 mm 48-pin QFN package</td>
</tr>
</tbody>
</table>

---

1 Crystal input  
2 Crystal output  
3 Reference clock inputs  
4 Serial port  
5 Voltage input pin for VCFS  
6 Frequency select inputs
Traveo™ MCU Family Automotive Roadmaps
Wireless Product Automotive Roadmaps
USB Product Automotive Roadmaps

Please Contact Your Cypress Local Sales Office For Details