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EMC Countermeasure Techniques in Hardware

Abstract
This white paper presents the techniques for EMC countermeasure in the hardware of Cypress Automotive MCUs.

Introduction
Electronic Control Units (ECUs) are used for vehicle control. These days, ECUs have more functionality and better integration due to the Microcontroller Unit (MCU) that is loaded with the ECU.

When the MCU performs a switching operation, it releases an electric current including a harmonic content. This switching electric current may interfere with the operation of other electronic equipment. This interference is called Electro Magnetic Interference (EMI). Conversely, MCU has to endure interference from outside. This is called Electromagnetic Susceptibility (EMS). Together, these are called Electro Magnetic Compatibility (EMC) and the countermeasure is very important.

This white paper presents the technique for EMC countermeasure in the hardware of Cypress Automotive MCUs. The list of the contents is as follows.

- Bypass capacitors
- GND patterns
- Power supply and GND wiring
- Pattern around oscillators
- Countermeasures of MODE and Reset pin
- Signal wiring
- Global pins
- Others


**EMC Countermeasure in Hardware**

**Bypass Capacitors**

- Example (1)

![Figure 1. Bypass Capacitors Connection with MCU (1)](image)

Connecting the bypass capacitors with the MCU power and GND terminal results in the following:

- It prevents noise invasion into the MCU from the power line, which is measured as EMS.
  - EMC is the sum of EMS and EMI.
- It does not betray the noise that occurs in the power terminal of the MCU to the power line, which is the measure of EMI.

To get the effect, locate the bypass capacitors as close as possible to the power supply and GND pins of the MCU.

- Example (2)

![Figure 2. Bypass Capacitors Connection with MCU (2)](image)

It is important for power supply (VDD, VSS) patterns to pass through both ends of the bypass capacitor with the least noise. In the bad example of Figure 2, because there is a branch in the VDD line between the MCU and the bypass capacitor, the line passes through a point with a large amount of noise. This needs to be changed by shifting the VDD line into the following sequence: **MCU > bypass capacitor > branch point**, as shown in the good example of Figure 2.

- Example (3)

![Figure 3. Bypass Capacitors Connection with MCU (3)](image)

In the bad example of Figure 3, because the line does not form the sequence **MCU > bypass capacitor > branch point**, it passes through a point with a large noise. Change this to the following sequence: **MCU > bypass capacitor > branch point**, as shown in the good example of Figure 3.
If a bypass capacitor is located on the opposite surface (reverse side) of the PCB from the MCU mounting surface, the lines will be connected through a via and the effectiveness of the bypass capacitor will be degraded due to the inductance component of the via. It is, therefore, best to locate bypass capacitors on the MCU mounting surface.

If bypass capacitors with different capacitances are mounted in parallel, the resonance point can be shifted to a higher frequency and the radiative noise at higher frequencies can be reduced by placing the bypass capacitor with the lowest capacitance closer to the MCU power supply and GND pins. Therefore, in the examples of Figure 5, it is best to arrange the 100-pF capacitor closest to the power supply and GND pins.

**GND Patterns**

The area directly under the MCU (on the MCU mounting surface) is the best location for reducing EMI. This needs to be converted to a solid GND to reduce radiative noise. **Note:** Radiative noise can be reduced by stabilizing the GND level.
• Example (7)

![Figure 7. GND Pattern for PCB](image)

The wiring closest to the perimeter of the PCB has the least coupling with the ground wiring and can easily radiate large amounts of noise. It is best to place the GND pattern around the perimeter and not run the power supply (VDD) or signal lines.

• Example (8)

![Figure 8. Free Areas on PCB](image)

Because the radiative noise can be reduced by increasing the area of the GND pattern on the board, free areas should be converted to GND.

**Note:** Radiative noise can be reduced by stabilizing the GND level.

• Example (9)

![Figure 9. Closed loop of GND Pattern](image)

Avoid creating open loops in the GND pattern of the board.
- Create broad ground areas using closed loops.
- Make loops as small as possible.
**Power Supply and GND Wiring**

- Example (10)

![Figure 10. Power supply / GND Pattern (1)](image)

If a power supply or GND pattern forms a loop shape, the radiated noise will be proportional to the area of the loop. Therefore, avoid making loops in the wiring.

- Example (11)

![Figure 11. Power supply / GND Pattern (2)](image)

- Power supply current loops can be made smaller and radiative noise reduced by running power supply patterns beside and parallel to the GND pattern.
- Use star-connected tracks to reduce the high-current carrying GND with the GND return path for delicate components, such as analog sensors.

- Example (12)

![Figure 12. Power supply / GND Pattern (3)](image)

Radiative noise is strong at sharp, 90-degree corners. It is, therefore, best if the power supply and GND pattern corners are 45 degrees or curved. This applies to both inner and outer layers.
Pattern around Oscillators

- Example (13)

![Figure 13. Oscillators Connection with MCU](image)

Make the wiring as short as possible because high-frequency noise at integral multiples of the oscillator frequency are radiated from the oscillator wiring.

- Example (14)

![Figure 14. Surrounding Oscillator Wiring with a GND Pattern](image)

Radiative noise is reduced by surrounding oscillator wiring with a GND pattern instead of running the wiring next to other signal wires or power supply (VDD) lines.

- Example (15)

![Figure 15. Separate the Oscillator GND and PCB GND](image)

Since there is a lot of noise on the GND connected to the load capacitance of the oscillator, fluctuations in the PCB GND can be suppressed and radiative noise reduced by creating a gap separating the PCB GND. However, some amount of area needs to be allocated to the separated GND. Caution is required because this gap also needs to be created in other layers so that there are no solid connections with GND planes in other layers through the vias.
Example (16)

![Diagram of good and bad power supply wiring]

Figure 16. Do not cross the Power Supply (VCC) or Signal Wiring

Ensure that the GND and the oscillator up and down lines do not cross the power supply (VCC) or signal wiring. If these lines cross, the oscillator may affect the power supply or signal wire, or the power supply or signal wire may affect the oscillator.

Example (17)

![Diagram of good and bad long pattern wiring]

Figure 17. Long Pattern around Oscillators

When a long pattern is arranged near the oscillator pattern, the long pattern will be an antenna and a strong noise occurs in the long pattern created by the radio wave. Sometimes, the oscillation is suspended. When the width of the GND pattern is insufficient, insert a 0-Ω dumping resistor in the long pattern. If the influence of noise is weak at the surface or at the back, mount the MCU and an oscillator on its side and wire.

Countermeasures of MODE and Reset Pin

Example (18)

![Diagram of average, good, and excellent mode pin termination]

Figure 18. Termination of the Mode Pins (1)

In principle, the MODE pins should be connected directly to the power supply or GND.
Example (19)

Cypress recommends that you switch the MODE pins mechanically, not logically, when performing on-board reprogramming of Flash products.

Example (20)

To prevent the reset pin from entering a HI-Z state, it should be pulled up using a resistance of approximately 1 kΩ.

Signal Wiring

Example (21)

The wiring of high-speed signals strongly radiate noise at sharp 90-degree corners, which is the same as power supply and GND patterns. Therefore, the patterns of high-speed signals should also be curved at 45 degrees. This applies to both inner and outer layers.
- Example (22)

- Run high-speed signal wiring, paired with GND wiring, in the same manner as you do for power supply (VDD) wiring.
- If you cannot fit many lines, GND wires can also be arranged for groups of several signal lines.
- The electrical length of a high-speed signal must be less than lambda/4, where lambda is the wavelength of the highest frequency component of the signal. This is usually dependent on the rise time of the signal.
- To reduce timing violations, match the electrical lengths of all signals, which are sampled by the same clock.

Note: High-speed signal lines are signal lines on the PCB that change at high frequencies (clocks, buses, and so on) or signals that are low frequency but have steep rising or falling edges.

- Example (23)

If there is some margin in the timing and drive capacity of an output pin that changes periodically, fit pads (lands) in advance so that a damping resistor can be added. When you need to filter out high frequencies, adjust by increasing the value of the damping resistor (if deemed unnecessary under testing, apply a zero-ohm short). Place the damping resistor close to the output pin.
- Example (24)

![Diagram of wiring the multi-layer board](image1)

**Figure 24. Wiring the multi-layer board (1)**

- In the case of multi-layer boards, the high-speed signal layer must have a neighboring GND layer (L1 or L3 in Figure 24).
- For high-speed boards, the PCB must be fabricated with a controlled impedance between the signal track and the neighboring GND layer, so that reflection losses are minimized.

- Example (25)

![Diagram of high-speed signal pattern](image2)

**Figure 25. High-Speed Signal Pattern (2)**

In the case of multi-layer boards, the wiring in the L3 and L4 layers shown in Figure 25 should be offset so that they are not stacked vertically (this is to ensure opposing GND).

- **Global Pins**

  - Example (26)

![Diagram of inserting protective components](image3)

**Figure 26. Insert the Protective Components**

Global pins (MCU pins that are connected directly to a harness and cable), including power supply (VDD, AVcc, AVRH, AVRL), apply surges and ESD directly to the MCU pins. This causes damage to the MCU due to overvoltage, overcurrent, and latch-up, and induces MCU malfunctions due to applying noise. Protective components suitable for the type of noise, therefore, need to be inserted.
Others

- Example (27)

![Figure 27. Insert the Ferrite](image)

Radiative noise due to MCU power supply current variations is often a problem. Equip the power supply pins (VDD) with pads (lands) in advance so that ferrite (beads) can be added. When you need to reduce radiative noise due to power supply current variations, adjust using the ferrite value.

**Note:** If deemed unnecessary under testing, apply a zero-ohm short.

- Example (28)

![Figure 28. Metal Case of the Crystal Oscillator](image)

The metal case of the crystal oscillator floats electrically, and will form an antenna that radiates noise if used as-is. The case, therefore, needs to be forced to GND.

**Note:** Pin floating islands (floating wiring and metal cases) to GND.

- Example (29)

![Figure 29. Use Smaller Components](image)

Use smaller components and strengthen the GND.
Example (30)

- Figure 30. Pull-up / Pull-down

If the fixed level of fixed-input pins can be either H or L, give priority to pull-down over pull-up. This is because pull-up requires power supply (VDD) wiring for that purpose and reduces the GND area compared to pull-down.

Example (31)

- Figure 31. TEST Pad

Since the wiring becomes crowded and the GND area is also reduced when TEST pads are fitted, pads should be limited to the bare minimum and avoided where possible.

References
