AN216999

Migrating from S25FL032P/S25FL064P Serial NOR Flash Products to S25FL064L Serial NOR Flash Products

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Associated Part Family: S25FL-P, S25FL-L

AN216999 provides guidelines for migration from Cypress' S25FL032P/S25FL064P Serial NOR Flash family of products to Cypress' S25FL064L Serial NOR Flash Family of products. The application note describes the similarities and differences in specifications to facilitate this conversion

Contents

1 Introduction

This document provides guidelines for migrating from Cypress' S25FL032P/S25FL064P Serial NOR Flash family of products to S25FL064L Serial NOR Flash family of products. It discusses the known issues that may be encountered when facilitating this conversion.

S25FL032P/S25FL064P is a 3.0 V, single-supply Flash memory device based on 90-nm MirrorBit® process technology. S25FL064L is also a 3.0 V, single-supply Flash memory device but based on an advanced 65-nm Floating Gate process technology. S25FL064L family of Flash devices represent the effort committed by Cypress to continually improve its product line. Among the advances are higher bandwidth through double-data rate instructions (DDR), the uniform 4 KB sector option, enhanced data protection schemes, and higher temperature grades. See the S25FL064L datasheet for full description of all new features and functions specified in the S25FL064L device.

2 Feature Comparison

S25FL064L supports a superset of the S25FL032P/S25FL064P feature set. Table 1 summarizes the feature similarities and differences. The Commands Set Comparison section discusses these differences in more detail.

Table 1. Feature Comparison

Feature/Parameter	S25FL064L	S25FL032P/S25FL064P
Technology Node	65-nm NOR Flash	90-nm NOR Flash
Architecture	Floating Gate	MirrorBit®
Density	64 Mb	32 Mb/64 Mb
Bus Width	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7V – 3.6V	2.7V – 3.6V
Normal Read Speed (SIO)	6.25 MB/s (50 MHz)	5MB/s (40MHz)
Fast Read Speed (SIO)	13.5 MB/s (108 MHz)	13MB/s (104MHz)
Dual Read Speed (DIO)	27 MB/s (108 MHz)	20MB/s (80MHz)
Quad Read Speed (QIO)	52 MB/s (108 MHz)	40MB/s (80MHz)
Quad Read Speed (QIO - DDR)	54 MB/s (54 MHz)	–
Program Buffer Size	256B	256B
Erase Sector Size	4 KB / 32 KB / 64 KB	64 KB
Parameter Sector Size	–	4 KB
Security Region / OTP	1024B	506B
Data Protection	Legacy Block	Legacy Block
	Individual Block Lock	
	Pointer Region	
Suspend / Resume	Erase / Program	–
Addressing	3 / 4 Byte + Bank	3 Byte
Hardware Reset	Yes	No
Operating Temperature	–40°C to +85°C	–40°C to +85°C
	–40°C to +105°C	–40°C to +105°C
	–40°C to +125°C	–
Deep Power Down	Yes – 2 µA (typical)	Yes – 3 µA (typical)
ID and Common Flash Interface	–	Yes
ID and Serial Flash Discovery Parameter	Yes	–
Packages	8-lead SOIC (208 mils) 16-pin SOIC (300 mils)	8-lead SOIC (208 mils) (32Mb only) 16-pin SOIC (300 mils)
	USON (4 × 4 mm) 8-Contact WSON (5 x 6 mm)	USON (5 x 6 mm) (32Mb only) 8-Contact WSON (6 × 8 mm)
	24-Ball FBGA (6 × 8 mm) (5 x 5 pin) 24-Ball FBGA (6 × 8 mm) (6 x 4 pin)	24-Ball FBGA (6 × 8 mm) (5 x 5 pin) 24-Ball FBGA (6 × 8 mm) (6 x 4 pin)

3 Conversion Highlights

This section shows the values that you may pay attention to while migrating from S25FL032P/S25FL064P to S25FL064L devices. Some register definitions are different between these two device families. See the highlighted text Table 2 and Table 3.

Table 2. S25FL032P/S25FL064P to S25FL064L Conversion Highlights

Feature	S25FL032P/S25FL064P				FL064L			
Commands								
Legacy Device Identification	Read_ID = 90h				N/A			
JEDEC Device Identification	RDID = 9Fh				RDID = 9Fh			
JEDEC Serial Flash Discoverable Parameters (SFDP)	N/A				RSFDP = 5Ah			
4KB Erase	P4E = 20h				SE = 20h			
8KB Erase	P8E = 40h				N/A			
32KB Erase	N/A				HBE = 52h			
64KB Erase	SE = D8h				BE = D8h			
OTP Program	OTPP = 42h				SECRP = 42h			
OTP Read	OTPR = 4Bh				SECR = 48h			
Device Identification								
RDID (9Fh) command output	*Identification*				*Identification*			
	Byte 0 Manu ID	Byte 1 Device ID	Byte 2 Device ID	Byte 3 # CFI Bytes	Byte 0 Manu ID	Byte 1 Device ID	Byte 2 Device ID	Byte 3 RFU
	01h	02h	15h/16h	4Dh	01h	60h	17h	Undefined
CFI tables	Yes				N/A			
Deep Power Down Release (ABh) while not in DPD Mode	Read 8bit electronic signature				Read Device ID			
Multiplexed IO2 & IO3 (Quad IO off/on)	(W# or ACC)/IO2 HOLD#/IO3				WP#/IO2 RESET#/IO3			
OTP/Secure Region	OTP: 2x8B ESN; 30x16B; 1x10B				Non-Volatile: 2x256B			
OTP/Secure Region Lock Protection	Yes, via OTP Lock Bits for each region				No for Regions 0 & 1; Yes for Regions 2 & 3			

Table 3. S25FL032P/S25FL064P to S25FL064L Conversion Highlights

S25FL032P/S25FL064P			FL064L	
RDSR = 05h			RDSR = 05h or RDSR2 = 07h	
Status Register			**Register[bit] & Command**	
Bit	**Name**	**Function**	**Bit**	**Command**
7	SRWD	Status Register Write Disable	SR1V[7]	RDSR1 = 05h
6	P_ERR	Programming Error	SR2V[6]	RDSR2 = 07h
5	E_ERR	Erase Error	SR2V[5]	RDSR2 = 07h
4	BP2	Block Protect	SR1V[4:2]	RDSR1 = 05h
3	BP1			
2	BP0			
1	WEL	Write Enable Latch	SR1V[1]	RDSR1 = 05h
0	WIP	Write In Progress	SR1V[0]	RDSR1 = 05h
RCR = 35h			RDCR1 = 35h or RDSR = 05h	
Configuration Register			**Register[bit] & Command**	
Bit	**Name**	**Function**	**Bit**	**Command**
7	N/A	N/A	N/A	N/A
6	N/A	N/A	N/A	N/A
5	TBPROT	Configures Start of Block Protection	SR1V[5]	RDSR = 05h
4	N/A	N/A	N/A	N/A
3	BPNV	Configures BP[2:0] Bits in Status Register	N/A	N/A
2	TBPARM	Configures the Parameter Sectors	N/A	N/A
1	QUAD	Quad I/O Mode	CR1V[1]	RDCR1 = 35h
0	FREEZE	Locks BP[2:0] Bits in Status Register	CR1V[0]	RDCR1 = 35h

4 Commands Set Comparison

Table 4 summarizes the supported commands for each device. Pertinent differences will be discussed in subsequent sections.

Table 4. Command Set Comparison

Function	Command	Description	S25FL064L	S25FL032P/ S25FL064P
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Fh	9Fh
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	–
	RDQID	Read Quad ID	AFh	–
	RUID	Read Unique ID	4Bh	–

Function	Command	Description	S25FL064L	S25FL032P/ S25FL064P
	READ_ID	Read Manufacturer and Device Identification	–	90h
Register Access	RDSR1	Read Status Register 1	05h	05h
	RDSR2	Read Status Register 2	07h	–
	RDCR1	Read Configuration Register 1	35h	35h
	RDCR2	Read Configuration Register 2	15h	–
	RDCR3	Read Configuration Register 3	33h	–
	RDAR	Read Any Register	65h	–
	WRR	Write Register (Status-1 and Configuration-1,2,3)	01h	01h
	WRDI	Write Disable	04h	04h
	WREN	Write Enable for Non-volatile data change	06h	06h
	WRENV	Write Enable for Volatile Status and Configuration Registers	50h	–
	WRAR	Write Any Register	71h	–
	CLSR	Clear Status Register	30h	30h
	4BEN	Enter 4 Byte Address Mode	B7h	–
	4BEX	Exit 4 Byte Address Mode	E9h	–
	SBL	Set Burst Length	77h	–
	QPIEN	Enter QPI	38h	–
	QPIEX	Exit QPI	F5h	–
	DLPRD	Data Learning Pattern Read	41h	–
	PDLRNV	Program NV Data Learning Register	43h	–
	WDLRV	Write Volatile Data Learning Register	4Ah	–
Read Flash Array	READ	Read	03h	03h
	4READ	Read (4-Byte Address)	13h	–
	FAST_READ	Fast Read	0Bh	0Bh
	4FAST_READ	Fast Read (4-Byte Address)	0Ch	–
	DOR	Dual Output Read	3Bh	3Bh
	4DOR	Dual Output Read (4-Byte Address)	3Ch	–
	QOR	Quad Output Read	6Bh	6Bh
	4QOR	Quad Output Read (4-Byte Address)	6Ch	–
	DIOR	Dual I/O Read	BBh	BBh
	4DIOR	Dual I/O Read (4-Byte Address)	BCh	–
	QIOR	Quad I/O Read	EBh	EBh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh	–
	DDRQIOR	DDR Quad I/O Read	EDh	–
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh	–
Program Flash Array	PP	Page Program	02h	02h
	4PP	Page Program (4-Byte Address)	12h	–
	QPP	Quad Page Program	32h	32h

Function	Command	Description	S25FL064L	S25FL032P/ S25FL064P
	4QPP	Quad Page Program (4-Byte Address)	34h	–
Erase Flash Array	SE	Sector Erase	20h	–
	4SE	Sector Erase (4-Byte Address)	21h	–
	P4E	4 KB Parameter Sector Erase	–	20h
	P8E	8 KB (two 4 KB) Parameter Sector Erase	–	40h
	HBE	Half Block Erase	52h	–
	4HBE	Half Block Erase (4-Byte Address)	53h	–
	BE	Block Erase	D8h	–
	4BE	Block Erase (4-Byte Address)	DCh	–
	SE	64 KB Sector Erase	–	D8h
	CE	Chip Erase / Bulk Erase	60h	60h
	CE	Chip Erase / Bulk Erase (alternate instruction)	C7h	C7h
Erase / Program Suspend / Resume	EPS	Erase / Program Suspend	75h	–
	EPR	Erase / Program Resume	7Ah	–
Security Region Array	SECRE	Security Region Erase	44h	–
	SECRP	Security Region Program	42h	–
	SECRR	Security Region Read	48h	–
	OTPP	Programs one byte of data in OTP memory space	–	42h
	OTPR	Read data in the OTP memory space	–	4Bh
Array Protection	IBLRD	IBL Read	3Dh	–
	4IBLRD	IBL Read (4-Byte Address)	E0h	–
	IBL	IBL Lock	36h	–
	4IBL	IBL Lock (4-Byte Address)	E1h	–
	IBUL	IBL Unlock	39h	–
	4IBUL	IBL Unlock (4-Byte Address)	E2h	–
	GBL	Global IBL Lock	7Eh	–
	GBUL	Global IBL Unlock	98h	–
	SPRP	Set Pointer Region Protection	FBh	–
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h	–
Individual and Region Protection	IRPRD	IRP Register Read	2Bh	–
	IRPP	IRP Register Program	2Fh	–
	PRRD	Protection Register Read	A7h	–
	PRL	Protection Register Lock (NVLOCK Bit Write)	A6h	–
	PASSRD	Password Read	E7h	–
	PASSP	Password Program	E8h	–
	PASSU	Password Unlock	EAh	–
Reset	RSTEN	Software Reset Enable	66h	–
	RST	Software Reset	99h	–

Function	Command	Description	S25FL064L	S25FL032P/ S25FL064P
	MBR	Mode Bit Reset	FFh	–
Deep Power Down	DPD	Deep Power Down	B9h	B9h
	RES	Release from Deep Power Down / Device Id	ABh	ABh

The primary areas of concern for migration from S25FL032P/S25FL064P to S25FL064L are device identification, extended 4-byte addressing, array protection feature reduction, AC/DC specification differences, and package/pin out differences.

4.1 Device Identification

In S25FL032P/S25FL064P, the RDID command outputs 1-byte of manufacturer's identification, followed by 2-bytes of device identification, and 64-bytes of Common Flash Interface (CFI) tables. CFI is a JEDEC defined (JEDEC-137B) query structure for host system interrogative handshake. Table 5 provides the byte sequence showing Device ID and CFI values after the host system provides the Device Identification (RDID) command. For details on the CFI byte contents, see the S25FL032P/S25FL064P datasheet.

Table 5. S25FL032P/S25FL064P Device Identification Command Byte Sequence

	Identification				Common Flash Interface					
Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	–	Byte 15	Byte 16	–	Byte 80
S25FL032P	01h	02h	15h	4Dh	Undefined	–	Undefined	51h	–	00h
S25FL064P			16h							

S25FL064L also provides a RDID command which outputs 1-byte of manufacturer's identification, followed by 2-bytes of device identification. Table 6 provides the byte sequence showing ID values.

Table 6. S25FL064L Device Identification Command Byte Sequence

	Identification			
Device	Byte 0	Byte 1	Byte 2	Byte 3
S25FL064L	01h	60h	17h	Undefined

S25FL064L does not have Common Flash Interface (CFI) tables. Instead, Serial Flash Discoverable Parameters (SFDP) are provided. SFDP is defined by JEDEC (JEDEC-216B) and consists of a header table, which identifies the SFDP parameters. SFDP is address based and Table 7 provides the SFDP address/byte sequences. For details on the SFDP byte contents, refer to the S25FL064L datasheet.

Table 7. S25FL064L SFDP Header and Parameter Address Map

	SFDP Header			SFDP Parameters			
Device	**Address 00h**	**–**	**Address 17h**	**Address 0300h**	**Address 0301h**	**–**	**Address 033Fh**
S25FL064L	53h	–	FFh	E5h	20h	–	A1h

4.2 Unique Identification

S25FL064L provides a 64-bit unique number for each device. S25F064P does not support unique identification.

Table 8 shows the address map for unique identification for S25FL064L.

Table 8. S25FL064L Unique ID Address Map

	UID			Additional UID Bytes			Reserved			OEM Name		
Device	**Address 00h**	**–**	**Address 07h**	**Address 08h**	**–**	**Address 0Fh**	**Address 10h**	**–**	**Address 1Fh**	**Address 20h**	**–**	**Address 37h**
S25FL064L	UID_Byte0	–	UID_Byte7	UID_Byte8	–	UID_Byte15	UID_Byte16	–	UID_Byte23	UID_Byte24	–	UID_Byte55

4.3 Extended Addressing

S25FL032P/S25FL064P utilizes a 3-byte (24-bits) address within commands to access the memory array (16 MB). Since 64 Mb translates to 8 MB, 3-byte addressing scheme is sufficient. However, to accommodate addressing the above 24-bits on multi-chip packages, S25FL064L supports additional addressing options, listed in Table 9. This enables use of higher density devices with greater performance in existing systems.

4.3.1 Extended Addressing with Legacy Instructions

S25FL064L provides a configuration bit that, when enabled, changes all 3-byte address commands to expect a 4-byte address. Most 3-byte address commands are legacy SPI commands. Table 9 lists all the commands requiring 4-byte addressing when the address configuration bit (ADP – CR2NV[1]) is set.

Table 9. Legacy Commands Requiring 4-Byte Addressing when ADP - CR2NV[1] is Set

Function	Command	Description	S25FL064L
Read Device ID	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah
Register Access	RDAR	Read Any Register	65h
	WRAR	Write Any Register	71h
Read Flash Array	READ	Read	03h
	FAST_READ	Fast Read	0Bh
	DOR	Dual Output Read	3Bh
	QOR	Quad Output Read	6Bh
	DIOR	Dual I/O Read	BBh
	QIOR	Quad I/O Read	EBh
	DDRQIOR	DDR Quad I/O Read	EDh
Program Flash Array	PP	Page Program	02h
	QPP	Quad Page Program	32h
Erase Flash Array	SE	Sector Erase	20h
	HBE	Half Block Erase	52h
	BE	Block Erase	D8h
Security Region Array	SECRE	Security Region Erase	44h
	SECRP	Security Region Program	42h
	SECRR	Security Region Read	48h
Array Protection	IBLRD	IBL Read	3Dh
	IBL	IBL Lock	36h
	IBUL	IBL Unlock	39h

4.3.2 Extended Addressing with New 4-Byte Instructions

S25FL064L has new instructions which require 4-byte addresses. lists all 4-byte commands supported by the S25FL064L.

Table 10. New Commands Requiring 4-Byte Addressing

Function	Command	Description	S25FL064L
Read Device ID	4READ	Read (4-Byte Address)	13h
	4FAST_READ	Fast Read (4-Byte Address)	0Ch
	4DOR	Dual Output Read (4-Byte Address)	3Ch
	4QOR	Quad Output Read (4-Byte Address)	6Ch
	4DIOR	Dual I/O Read (4-Byte Address)	BCh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh
Program Flash Array	4PP	Page Program (4-Byte Address)	12h
	4QPP	Quad Page Program (4-Byte Address)	34h
Erase Flash Array	4SE	Sector Erase (4-Byte Address)	21h
	4HBE	Half Block Erase (4-Byte Address)	53h
	4BE	Block Erase (4-Byte Address)	DCh
Array Protection	4IBLRD	IBL Read (4-Byte Address)	E0h
	4IBL	IBL Lock (4-Byte Address)	E1h
	4IBUL	IBL Unlock (4-Byte Address)	E2h
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h

4.4 Status and Configuration Registers

The working condition of S25FL064LP and S25FL064L devices is set by internal configuration registers. Status registers, on the other hand, provide the device status during embedded algorithmic operations.

Table 11 summarizes the supported registers for each device.

Table 11. Register Set Comparison

Register Type	S25FL064L	S25FL032P/ S25FL064P
Status Register 1	Yes	Yes
Status Register 2	Yes	–
Configuration Register 1	Yes	Yes
Configuration Register 2	Yes	–
Configuration Register 3	Yes	–
Individual and Region Protection Register	Yes	–
Password Register	Yes	–
Individual Block Lock Access Register	Yes	–
Pointer Region Protection Register	Yes	–
DDR Data Learning Registers	Yes	–

For the type and functionality of each configuration/status bit, see the device specific datasheet.

4.5 Deep Power Down Mode

S25FL032P/S25FL064P and S25FL064L both support low power Deep Power-down modes. However, S25FL032P/S25FL064P allows for reading the 8-bit electronic signature using the Release from Deep Power-down command. This feature is not supported in S25FL064L.

4.6 High Voltage Accelerated Programming

S25FL032P/S25FL064P supports V_{HH} (nominally 9 V) on the W#/ACC input pin to accelerate programming. S25FL064L does not support high voltage accelerated programming and does not allow application of V_{HH} (nominally 9V) on the WP# input.

4.7 OTP/Secure Regions

S25FL032P/S25FL064P and S25FL064L both support addressable space which is separate from the main Flash memory array. Table 12 shows the regions for both devices.

Table 12. OTP/Secure Region Definitions

Device Type	One-Time Programmable	Region Type 1: Two 8-byte (ESN) Thirty 16-byte One 10-byte	Non-Volatile	Region Type 2: Four 256-byte
S25FL032P/ S25FL064P	Yes	Yes	–	–
S25FL064L	–	–	Yes	Yes

4.8 Double Data Rate (DDR) Read Commands

S25FL064L supports the DDR Quad I/O Read command which improves bandwidth in the four I/O modes. This command is supported up to 54 MHz. A 4-byte address version of this command is also available. S25FL032P/S25FL064P does not support any DDR Read commands.

4.9 Data Protection

S25FL032P/S25FL064P and S25FL064L Flash devices implement data protection schemes which shield program and erase operations. Table 13 shows the data protection schemes supported in each device. For more details on the protection schemes, see the respective device datasheets.

Table 13. Data Protection Schemes Supported

Device Type	Block Protection	Individual Block Lock Protection	Pointer Protection	OTP Region Lock Protection	Individual and Region Protection
S25FL032P/ S25FL064P	Yes	–	–	Yes	–
S25FL064L	Yes	Yes	Yes	–	Yes

4.10 Erase and Program Suspend/Resume Operations

S25FL064L supports program and erase suspend and resume commands which allow program and erase operations to be individually suspended (EPS:75h) and resumed (EPR: 7Ah) to access data in blocks which are not being modified. Status Register 2 has been added to allow host software to determine if a particular operation is in suspension. Read Status Register 2 (RDSR2:07h) command has been added to access this new register. Erase/Program suspend/resume operations are not supported in S25FL032P/S25FL064P.

5 Hardware Comparison

Pertinent hardware differences will be discussed in subsequent sections.

5.1 HOLD Functionality

S25FL032P/S25FL064P supports serial communications hold (stop) through HOLD# pin. HOLD# is a multiplexed pin and is used during Quad communication as IO3. S25FL064L does not support hold functionality. Instead, HOLD# is replaced by RESET# and acts like a hardware reset when CS# is high. RESET# is again multiplexed with IO3 for Quad mode.

5.2 Software Reset

S25FL064L supports a new Software Rest command (RSTEN:66h, RESET:99h) which restores the device to its initial power-up state except for FREEZE and PPB Lock bits in device configuration and PPB Lock registers.

5.3 DC Parameters

Table 14 provides comparisons of DC parameters for S25FL032P/S25FL064P and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that the user carefully review all the parameter differences for any potential impact.

Table 14. DC Parameters Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL032P/S25FL064P			Unit
		Min	Typical	Max	Min	Typical	Max	
VDD	Supply Voltage	2.7	3	3.6	2.7	3	3.6	V
VHH	ACC Program Acceleration Voltage	–	–	–	**8.5**	–	**9.5**	**V**
VDD (min)	VDD (minimum operation voltage)	2.7	–	–	2.7	–	–	V
VDD (cut-off)	VDD (Cut 0ff where re-initialization is needed)	2.4	–	–	2.4	–	–	V
VDD (low)	VDD (low voltage for initialization to occur)	1	–	–	2.3	–	–	V
VIL	Input Low Voltage	–0.5	–	0.3 x VDD	–0.3	–	0.3 x VDD	V
VIH	Input High Voltage	0.7 x VDD	–	VDD + 0.4	0.7 x VDD	–	VDD +0.5	V

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL032P/S25FL064P			Unit
		Min	Typical	Max	Min	Typical	Max	
VOL	Output Low Voltage	–	–	0.2		–	0.4	V
VOH	Output High Voltage	VDD – 0.2	–		VDD-0.6	–		V
ILI	Input Leakage Current	–	–	±4	–	–	±2	µA
ILO	Output Leakage Current	–	–	±4	–	–	±2	µA
ICC1	Active Power Supply Current (READ) - Serial SDR	–	25	35	–	–	38	mA
	Active Power Supply Current (READ) - Serial DDR	–	30	35	–	–		mA
ICC2	Active Power Supply Current (Page Program)	–	40	50	–	–	26	mA
ICC3	Active Power Supply Current (WRR or WRAR)	–	40	50	–	–	15	mA
ICC4	Active Power Supply Current (SE)	–	40	50	–	–	26	mA
ICC5	Active Power Supply Current (HBE, BE)	–	40	50	–	–	26	mA
ISB	Standby Current	–	60	100	–	80	200	µA
IDPD	Deep Power Down Current	–	2	20	–	3	10	µA
IPOR	Power On Reset Current	–	15	20	–	–	–	mA

5.4 SDR AC Parameters

Table 15 provides comparisons of AC parameters for S25FL032P/S25FL064P and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all parameter differences for any potential impact.

Table 15. SDR AC Parameter Comparison

Symbol	Parameter Operating Temperature Range –40 °C to +105 °C	S25FL064L			S25FL032P/S25FL064P			Unit
		Min	Typical	Max	Min	Typical	Max	
FSCK - 1	SCK Clock Frequency for dual and quad commands	–	–	108	–	–	80	MHz
FSCK - 2	SCK Clock Frequency for READ and 4READ instructions	–	–	50	–	–	40	MHz
PSCK	SCK Clock Period	1/ FSCK	–	–	1/ FSCK	–	–	
tWH, tCH	Clock High Time	50% PSCK -5%	–	–	4.5	–	–	ns
tWL, tCL	Clock Low Time	50% PSCK -5%	–	–	4.5	–	–	ns
tCRT, tCLCH	Clock Rise Time (slew rate)	0.1	–	–	0.1	–	–	V/ns
tCFT, tCHCL	Clock Fall Time (slew rate)	0.1	–	–	0.1	–	–	V/ns
tCS	CS# High Time (Any Read Instructions)	20	–	–	10	–	–	ns
	CS# High Time (All other Non-Read instructions)	50	–	–	50	–	–	ns
tCSS	CS# Active Setup Time (relative to SCK)	3	–	–	3	–	–	ns
tCSH	CS# Active Hold Time (relative to SCK)	5	–	–	3	–	–	ns

Symbol	Parameter Operating Temperature Range –40 °C to +105 °C	S25FL064L			S25FL032P/S25FL064P			Unit
		Min	Typical	Max	Min	Typical	Max	
tSU	Data in Setup Time	3	–	–	3	–	–	ns
tHD	Data in Hold Time	2	–	–	2	–	–	ns
tV	Clock Low to Output Valid	–	–	8	–	–	9.5	ns
tHO	Output Hold Time	1	–	–	2	–	–	ns
tDIS	Output Disable Time	–	–	8	–	–	8	ns
tWPS	WP# Setup Time	20	–	–	20	–	–	ns
tWPH	WP# Hold Time	100	–	–	100	–	–	ns
tDP	CS# High to Deep Power Down Mode	–	–	3	–	–	10	µs
tRES	CS# High to Release from Deep Power Down Mode	–	–	5	–	–	30	µs
tQEN	QIO or QPI Enter mode, time needed to issue next command	–	–	1.5	–	–	–	µs
tQEXN	QIO or QPI Exit mode, time needed to issue next command	–	–	1	–	–	–	µs

5.5 Embedded Algorithms Performance

Table 16 provides comparisons of Embedded Algorithms performance parameters for S25FL032P/S25FL064P and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all parameter differences for any potential impact.

Table 16. Embedded Algorithm Performance Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL032P/S25FL064P			Unit
		Min	Typical	Max	Min	Typical	Max	
tW	Non-volatile Register Write Time	–	220	1200	–	–	100	ms
tPP	Page Programming (256 Bytes)	–	450	1350	–	1500	3000	µs
tBP1	Byte Programming (First Byte)	–	75	90	–	–	–	µs
tBP2	Additional Byte Programming (After First Byte)	–	10	30	–	–	–	µs
tSE	Sector Erase Time (4KB physical sectors)	–	65	270	–	200	800	ms
tHBE	Half Block Erase Time (32KB physical sectors)	–	300	600	–	–	–	ms
tBE	Block Erase Time (64KB physical sectors)	–	450	1150	–	500	2000	ms
tCE	Chip Erase Time	–	55	150	–	64	128	s

6 Conclusion

Migration from S25FL032P/S25FL064P to S25FL064L is straight forward and requires minimal accommodation regarding either system software or hardware. Once accommodations are made, if required, S25FL064L Flash can enable use of higher density devices with greater performance in existing systems.

7 Related Documents

Table 17. Cypress NOR Flash Product Specific Datasheets

Product Family	Spec Number	Document Title
FL-P Family	002-00650	S25FL032P, 32-Mbit 3.0 V SPI Flash Memory
FL-P Family	002-00649	S25FL064P, 64-Mbit 3.0 V SPI Flash Memory
FL-L Family	002-12878	S25FL064L, 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5500327	SZZX	11/11/2016	New application note.
*A	5810225	AESATP12	07/11/2017	Updated logo and copyright.
*B	6182738	ZHFE	05/03/2018	Included FL032P Added conversion highlight table

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