AN216200

Cypress Non-Burst-Mode Parallel NOR Flash Memory – Layout Guide for PCBs

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Associated Part Families: S29AS-J, S29AL-J, S29JL-J, S29PL-J, S29GL-N, S29GL-P, S29GL-S, and S29GL-T

Related Application Notes: AN98508, AN201383, and AN211622

AN216200 discusses printed circuit board (PCB) layout recommendations to improve signal integrity and system performance when using Cypress non-burst-mode parallel NOR Flash memory.

1 Introduction

This document provides general design recommendations for a PCB utilizing Cypress non-burst-mode parallel NOR Flash Memory products. These guidelines include recommendations for both signal routing and power delivery to the device.

In general, to achieve the best performance, the PCB design should provide an impedance- and loss-controlled environment, support a low-impedance power delivery system, and control electromagnetic interference (EMI).

This document serves as an initial reference for PCB designs using Cypress non-burst-mode parallel NOR Flash products. It does not eliminate the need to perform signal integrity and power delivery simulations. Use Cypress-provided IBIS models as well as IBIS models from controller vendors for signal timing and crosstalk simulations. You should verify actual signal characteristics empirically on prototype and validation build units.

If a design cannot meet the recommendations provided herein, perform detailed simulations to determine whether deviations from the recommendations would affect bus performance.

2 Non-Burst-Mode Parallel NOR Flash Signal Description

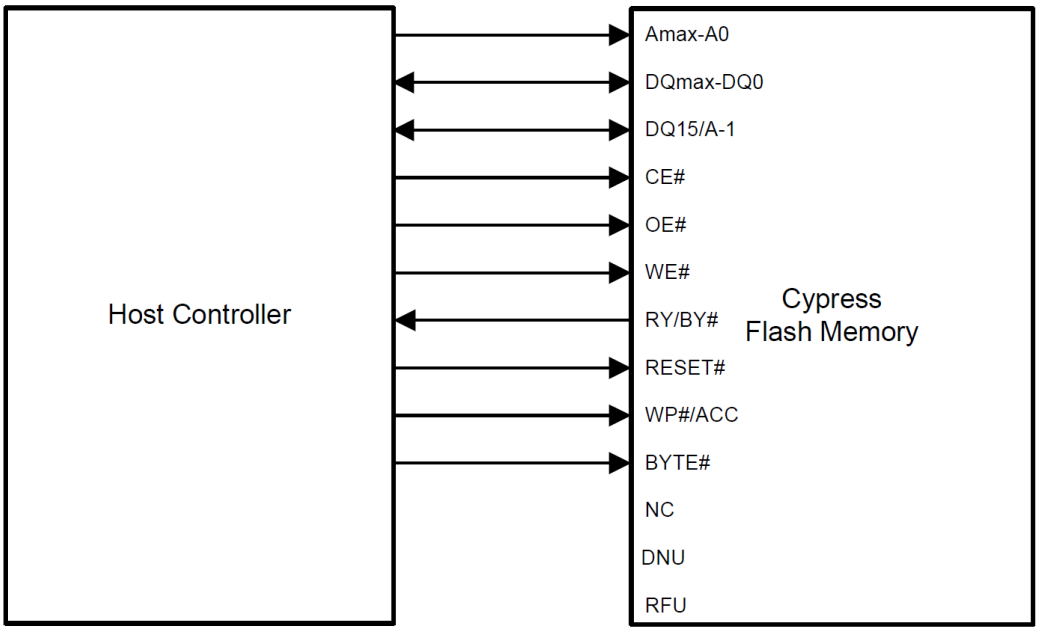
Cypress non-burst-mode parallel NOR Flash products are available in single-die-per-package and dual-die-per-package options. In both options, a single chip enable control input (CE#) enables all die within the package. Table 1 provides a summary with descriptions of all I/Os on the Cypress non-burst-mode parallel NOR Flash memory device. Figure 1 presents a simplified signal connection diagram between the Cypress Flash Memory and the host controller. Note that Table 1 and Table 2 summarize the I/Os found on all Cypress non-burst-mode parallel NOR Flash devices and may not reflect an individual device. See product-specific datasheets, listed in Section 7, to determine the I/Os for a particular device and for additional information regarding their function and operation.

Table 1. I/O Descriptions and PCB Connection Recommendations

Symbol	Type	Description
RESET#	Input	Hardware Reset. At V_{IL} (Input Low Voltage), causes the device to reset control logic to its standby state, ready for reading array data.
CE#	Input	Chip Enable. At V_{IL}, selects the device for data transfer with the host controller.
OE#	Input	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH} (Input High Voltage), causes outputs to be high impedance (HI-Z).
WE#	Input	Write Enable. At V_{IL}, indicates data transfer from host to device. At V_{IH}, indicates data transfer is from device to host.
Amax-A0	Input	Address inputs.
DQmax-DQ0	Input/Output	Data inputs and outputs.

Symbol	Type	Description
DQ15/A-1	Input/Output	DQ15: Data inputs and outputs. A-1: Least significant bit of the address input in byte mode.
WP#/ACC	Input	Write Protect. At V_{IL}, disables program and erase functions in a sector of the device. At V_{IH}, the sector is not protected. At V_{HH} (Voltage for ACC Program Acceleration), automatically places device in unlock bypass mode and supports accelerated programming on devices that support it. WP# has an internal pull up; when unconnected WP# is at V_{IH}.
RY/BY#	Output – open drain	Ready/Busy. Indicates whether the execution of an embedded algorithm is in progress.
BYTE#	Input	Selects data bus width.
V_{CC}	Power Supply	Core power supply.
V_{IO}	Power Supply	Input/Output power supply.
V_{SS}	Power Supply	Power supplied ground.
NC	No Connect	Not connected internally, the pin/ball location may be used in the PCB as part of a routing channel.
RFU	No Connect	Reserved for future use. Not currently connected internally; however, the pin/ball location should be left unconnected and unused as a PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.
DNU	Reserved	Do not use; reserved by Cypress.

Figure 1. Host to Non-Burst-Mode Parallel NOR Flash Simplified Interface Connections



The signals listed in Table 1 form five distinct signal groups: data, address, read/write control, other controls, and power/ground. During signal routing, you should give priority to the signal groups to ensure they maintain a high quality signal. Table 2 ranks the signal integrity priority of the five signal groups, where one represents the highest priority and four represents the lowest.

Table 2. Signal Integrity Priority of Signal Groups

Signal Group	Pin Names	Signal Integrity Priority
Data	DQmax-DQ0	1
Address	Amax-A0, A-1	2
Read/Write Control	CE#, OE#, WE#	3
Other Controls	RESET#, WP#/ACC, RY/BY#	4
Power/Ground	V_{CC}, V_{IO}, V_{SS}	See Section 5

The signal integrity priority denotes the importance of treating that particular signal group as a high-speed signal. Note that the signal integrity priority does not necessarily dictate the order of signal routing.

3 Signal Breakout, Routing Strategy, and Impedance Control

Cypress recommends the following actions to improve signal integrity and impedance control.

- Break out all signals on the top PCB layer, assuming that the second layer is a ground plane. This will allow better impedance control and smaller impedance mismatch between the breakout traces and traces outside the breakout area.
- Connect V_{CC} and V_{IO} to the nearest power plane through vias that are located as close to the target power ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Connect V_{SS} to the nearest ground plane through vias that are located as close to the target ground ball/pin as possible. Traces from the land pad to the vias should be as thick as possible.
- Use a smaller trace width (between 4-mil and 6-mil) and space adjacent traces approximately three trace widths apart to achieve a 50-ohm impedance. The impedance of data traces depends on the PCB stack-up and the trace width. Use either Microstrip or Stripline interconnects so long as the continuous trace impedance is 50 ohms (±10 percent) throughout the routing path.
- Use buried vias and as few vias as possible to reduce impedance discontinuities due to additional capacitive loading arising from through-hole vias. Any via attached to a trace will alter the signal delay of that trace.
- Route all signal groups on the same signal layer and in the same signal configuration, either all microstrip or all stripline.

4 General Signal Routing Guidelines

The following guidelines define the recommended trace width and trace spacing, total length limitation, and length-matching requirements to achieve optimal signal integrity and timing margins. These recommendations assume point-to-point routing between the host controller and the Cypress non-burst-mode parallel NOR Flash memory for simplicity. If this is not the case, you should first select the topology type to follow (star, T, or daisy chain). Cypress recommends star or T topology with the appropriate termination resistors determined from IBIS simulations. Consider performing signal integrity simulations using Cypress-provided IBIS models to determine guidelines tailored to your specific application.

- Determine the exact values of signals trace width and trace spacing based on the trace impedance requirement.
- Make the V_{SS} plane serve as a primary reference, or return path, for all signals. The power layer should only serve as a secondary signals reference option where a solid, continuous ground reference is present.
- Avoid gaps or voids in reference planes to minimize or eliminate return current discontinuity.
- Avoid routing traces at the edge of the reference plane.
- When routing data signals, route the longest signals first. This allows adjustment for signals with shorter lengths.

- Isolate the ground return path of analog signals from digital noise whenever possible.
- Keep all recommended signal routing lengths equal to the distance from package pin (source) to package pin (destination) by considering package length compensation.
- Use signal integrity tools to estimate actual trace velocities and path delays to validate the electrical properties depending on the dielectric material. Cypress determines electrical properties of signal routing by assuming the dielectric material is FR4. With this assumption, 1-inch equals approximately166-ps.

4.1 Signal Routing Geometry Constraints

4.1.1 Maximum Total Length

- The total load capacitance, which directly affects signal integrity, defines the absolute maximum length of signals with respect to their reference plane.
  - The total load capacitance should remain below 30 pF.
  - Total load capacitance includes the following:
    - Total trace length capacitance (~3.3 pF/inch with FR4 assumption),
    - Maximum pin capacitance associated with any parasitic capacitance of connected devices such as connectors and series resistors
    - Maximum pin capacitance of the controller package.
- The Read/Write operation timing requirements bound the total length of address, control, and data signal routing lines, as stated in the product datasheet. Perform a channel timing simulation to ensure the system meets these critical timing requirements. For example, address and data maximum lengths should ensure the required t_{ACC} and t_{RC} parameters for back-to-back read operations.
- Best practice is to begin with the AC timing equations for key timing parameters provided on the Cypress non-burst-mode parallel NOR Flash and controller datasheets for the Flash interface.

4.1.2 Length Matching

- Length matching refers to the trace lengths from the memory package pin to the signal pin of the controller. Length matching must include the effective electrical length of any vias.
- Cypress recommends routing WE# first. WE# will determine the length mismatch requirements with CE# through t_{CH}, with address through t_{ALS}/t_{ALH}, and with data through t_{DS}/t_{DH}.
- Table 3 provides signal skew recommendations for the various signal groups. It is important to note the signal polarities (rising edge and falling edge triggers) as well as the lead and lag timing to determine whether a specific control signal should always lead or lag compared to another signal or Data bus.

Table 3. Length Match Recommendations for Signal Groups

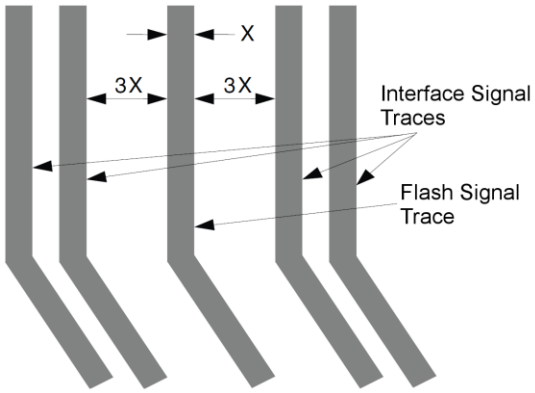
Signal Group	Length Match Recommendation
Data	± 500 mils
Address	± 500 mils
Data to Read/Write Control	± 500 mils
Address to Read/Write Control	± 500 mils

- The length of WP#, RY/BY#, and RESET# should be as small as possible. Avoid routing these signals adjacent to higher-frequency signals to minimize noise from crosstalk.

4.1.3 Signal Spacing Constraints

- The center-to-center trace spacing should be greater than three times 'H' within a signal group is, where H is the dielectric height between the signal and ground reference layer.
- The center-to-center trace spacing between signal groups should be greater than three times the trace width. In addition, the center-to-center trace spacing between Flash signals and other interface signals should be greater than three times the trace width as well. Figure 2 provides a visualization of the recommended signal trace spacing.

Figure 2. Recommended Signal Trace Spacing on the PCB



4.1.4 Termination

- You should review the drive strength/impedance of the controller I/O as well as transmission line routing to determine whether series termination is required on these lines. Drive strength for all three pressure, volume, and temperature (PVT) (typical, minimum, and maximum corners) can be determined by reviewing the IBIS IV/VT curves.
- Refer to the appropriate Cypress product datasheet, listed in Section 7, for the RY/BY# pull-up resistor value.

5 Power Delivery Guidelines

The following power delivery guidelines will help ensure that there are no power issues within the system.

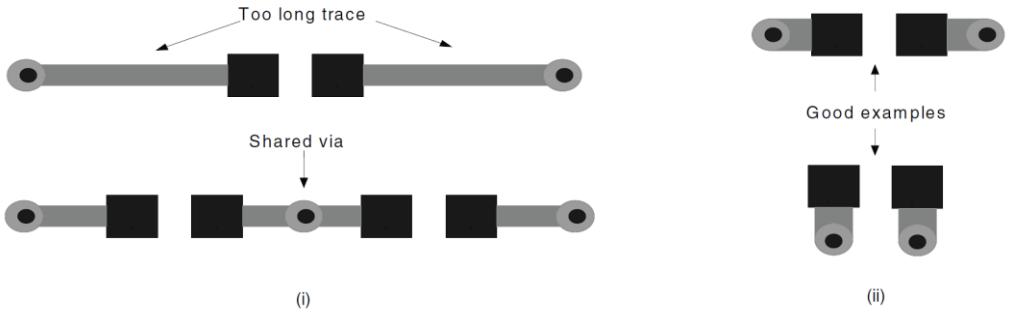
- Connect each V_{SS} pin/ball to a solid ground plane with its own unique via to improve IR drop.
- Connect V_{CC} pins/balls to a supply plane with its own unique via to improve IR drop.
- Connect V_{IO} pins/balls to a separate V_{IO} plane through more than one via from the breakout layer.
- At no point should V_{IO} be greater than V_{CC} +200-mV; therefore, you must keep these supply planes as noise-free as possible. In addition, the regulator set points and tolerances should be selected with this restriction in mind as there could be varying DC drops from the regulator pin to the V_{CC} and V_{IO} supply near the memory device.
- Gaps between power planes should be at least 20 mil, where possible. A gap of at least 80 mil should exist between power islands on the same layer, if possible. The air gap between power islands must be greater than 40 mil, preferably as much as 100 mil.
- Power islands, such as V_{CC} and V_{IO} islands, should be at least 250-mil wide at the narrowest point to avoid bottlenecks.
- Maintain a minimum trace width of 20 mil for all supply traces, except at the package breakout area where vias tie the supply to the nearest supply plane. Route the supply and ground traces (or planes) close to each other to avoid large inductive loops.
- Cypress recommends keeping the supply trace lengths less than or equal to 400-mil and keeping the trace widths greater than or equal to 20 mil.
- Utilize trace widths greater than 20 mil to maintain low impedance from the voltage regulator to the Flash voltage supply pins/balls as well as from the voltage regulator to the controller Flash I/F supply pins/balls.
- It is possible that voltage regulator will not be on the same PCB as the Flash package when using a module configuration. In this case, you should maintain the lowest possible impedance on traces to V_{CC}, V_{IO}, and V_{SS}. Wider traces can help to ensure a lower impedance.

- If there is a connector between the Host Controller and the Cypress non-burst-mode parallel NOR Flash, Cypress recommends the use of a G: S/P: G type connector configuration where 'S' refers to signal, 'G' refers to GND, and 'P' refers to V_{CC}.
- It is best to add V_{CC}, V_{IO}, and GND test points as close as possible to each Flash package and next to the voltage regulator. These test points will allow the measurement of V_{CC}-GND and V_{IO}-GND waveforms at both VRM and the package.

5.1 Decoupling Capacitor Recommendations

- Place the PCB decoupling capacitors as close to the package as possible.
- Select decoupling capacitors that have low equivalent series inductance (ESL) and equivalent series resistance (ESR).
- V_{CC} and GND trace routing from the capacitor should be as wide as possible to avoid inductive and resistive effects.
- A minimum two 1-uF 0402 ceramic capacitors should be placed between V_{CC} and GND near each side of the package.
- In additional to these decoupling capacitors; two 0.1-uF 0402 ceramic capacitors should be placed, as close to the package as possible, between V_{CC} and GND and another two, as close as possible, between V_{IO} and GND.
- Cypress recommends using X7R or X5R capacitors with a rated voltage greater than or equal to at least two times V_{CC} max.
- The decoupling capacitor trace length should remain short and should have a unique via, not shared with another decoupling capacitor. Figure 3 presents good and poor examples of decoupling capacitor routing techniques.

Figure 3. Decoupling Capacitor Routing Techniques: (i) Poor Routing Examples, (ii) Good Routing Examples



6 Test Points and Oscilloscope Measurements

You should perform signal quality, timing, and power delivery characterization using industry-standard digital signal evaluation techniques. The statements below outline a number of those techniques.

- Test points should be as close as possible to the controller and Cypress non-burst-mode parallel NOR Flash memory package pins for DQmax-DQ0 and RY/BY# signals. In addition, the test points should be located as close as possible to the non-burst-mode parallel NOR Flash memory package pin for the remaining the signals.
- Measure meaningful signals as close to the Flash memory as possible when the controller is driving. When the Flash memory device is driving, the opposite is true.
- While creating test pad, the stub (extra inductance and capacitance) resulting from the test pad should be minimized. It is better to probe at the breakout via rather than creating test pad stubs. In addition, in the case of 4-layer PCBs with through-hole vias, probe signals at the bottom of the PCB on the through-hole vias if possible.

- While performing scope measurements, use a 3-GHz or greater bandwidth scope and low-impedance probes. This will provide a more accurate representation of the waveform transition (such as the rising and the falling portion of the waveform).
- Always measure V_{CC}-V_{SS} and V_{IO}-V_{SS} at the controller, the voltage regulator, next to the connector (either side), and at the Flash memory. This needs to be performed prior to making any signal measurements to ensure that the supply is not noisy, which will affect the signal timing. In addition, these measurements establish the IR drop from regulator to controller or the regulator to the Flash device.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals, such as WE#.

7 Related Documents

Table 4. Cypress Non-Burst-Mode Parallel NOR Flash Product Specific Datasheets.

Product Family	Spec. Number	Title
GL Family	001-98285	3.0V GL-S Flash Memory Family, S29GL01GS 1 Gbit, S29GL512S 512 Mbit, S29GL256S 256 Mbit, S29GL128S 128 Mbit Datasheet
	001-98286	3.0V GL-S Flash Memory, S29GL064S 64 Mbit Datasheet
	001-98296	S70GL02GS 2 Gbit (256 Mbyte) 3.0V Flash Memory Datasheet
	001-98525	S29GL064N, S29GL032N 64 Mbit, 32 Mbit 3 V Page Mode MirrorBit Flash Datasheet
	002-00247	S29GL01GT 1 Gbit and S29GL512T 512 Mbit Parallel NOR Flash Datasheet
	002-00886	S29GL01GP, S29GL512P, S29GL256P, S29GL128P 1 Gbit, 512, 256, 128 Mbit, 3 V, Page Flash with 90 nm MirrorBit Process Technology Datasheet
	002-01338	S70GL02GP, 2 Gbit, 3.0 Volt-only Page Mode, S70GL-P MirrorBit® Flash Memory Datasheet
	002-01522	S29GL512N, S29GL256N, S29GL128N 512, 256, 128 Mbit, 3 V, Page Flash Featuring 110 nm MirrorBit Datasheet
PL Family	002-00615	S29PL-J 128/128/64/32 Mbit (8/8/4/2M x 16-Bit) V, Flash with Enhanced VersatileIO™ Datasheet
JL Family	002-00856	S29JL064J 64 Mbit (8M x 8-Bit/4M x 16-Bit), 3 V, Simultaneous Read/Write Flash Datasheet
AL Family	002-00777	S29AL016J 16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 3 V, Boot Sector Flash Datasheet
AS Family	002-01122	S29AS016J 16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 1.8 V Boot Sector Flash Datasheet

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