Military Memory

Q4 2019

Cypress Roadmap
<table>
<thead>
<tr>
<th>Fast Async SRAM</th>
<th>Sync SRAM</th>
<th>Nonvolatile SRAM</th>
<th>F-RAM™</th>
<th>NOR Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC1</td>
<td>NoBL®2, ECC</td>
<td>QDR®3 II+/IV</td>
<td>Serial/Parallel I/O</td>
<td>Serial I/O, ECC</td>
</tr>
<tr>
<td>CYT41xKV13</td>
<td>144Mb, 1.8 V, 250 MHz, x18/x36, Burst 2/4, M</td>
<td>S70/79FL-S</td>
<td>1Gb; 3.0 V, 133-MHz QSPI, Auto E, M</td>
<td></td>
</tr>
<tr>
<td>CYT26xKV18</td>
<td>144Mb, 1.8 V, 250 MHz, x18/x36, Burst 2/4, M</td>
<td>S25FL-S</td>
<td>128Mb/256Mb; 3.0 V, 133-MHz QSPI, Auto E, M</td>
<td></td>
</tr>
<tr>
<td>CYPT154xAV18</td>
<td>72Mb, 1.8 V, 250 MHz, x18/x36; Burst 2/4, M</td>
<td>Q419</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Error-correcting code  
2 No Bus Latency  
3 Quad Data Rate  
4 Real-time clock  
5 Qualified Manufacturers  
6 Military Temperature: −55°C to +125°C  
7 Qualified Manufacturers List Level Q, per MIL-PRF-38535  
8 AEC-Q100 −40°C to +125°C  
9 Qualified Manufacturers List Level Q, per MIL-PRF-38535  
10 Military Temperature: −55°C to +125°C
256Kb/1Mb Military nvSRAM

**Applications**
Military communication and real-time controls, avionics real-time controls and high-reliability data logging

**Features**
- Fast Nonvolatile Memory
  - Access time 35 ns
  - Available in parallel interface for 256Kb and 1Mb densities
  - Unlimited read/write endurance
  - One million store cycles on power fail
- Specifications
  - 100 years data retention at +85°C
  - Qualified Manufacturers List Level Q (QML-Q certified) per MIL-PRF-38535
  - Military temperature grade: -55°C to +125°C
- Packages: Ceramic 32-pin DIP

**Collateral**
Datasheet: [Contact Sales](#) (Available Now)

**Availability**
Production: Now
72Mb QDR®²-II+ SRAM

Applications
Payload processing and reconfigurable computing platforms

Features
- High Performance Memory
  - Maximum frequency of operation/throughput: 250 MHz/36 Gbps
  - Two independent unidirectional data ports for read and write enable concurrent transactions
  - Maximum throughput with double data rate (DDR) data ports
  - Output impedance matching input (ZQ): Matches the device outputs to system data bus impedance
  - Bit-interleaving to eliminate multi-bit errors
  - I/O signaling standards: 1.5–1.8 V (HSTL)
- Specifications
  - Burst sizes: 2 or 4
  - Bus-width configurations: x18 or x36
  - Military temperature grade: -55°C to +125°C
- Controllers available for Altera/Xilinx/Microsemi FPGAs
- Package: 165-pin CCGA²

Collateral
Datasheets: CYPT1542AV18/CYPT1544AV18
CYPT1543AV18/CYPT1545AV18

Availability
Production: Now

1 Quad Data Rate: Four data transfers per clock cycle
2 Ceramic column grid array package
QDR®-IV SRAM

Applications
Switches and routers, high-performance computing, test equipment, military and aerospace systems

Features
- **Highest Performance Memory**
  - Available in two options: High Performance (RTR 1334 MT/s) and Extreme Performance (RTR 2132 MT/s)
  - Two independent, bidirectional double data rate (DDR)\(^1\) data ports
  - Error-correcting code (ECC) to detect and correct single-bit errors (<0.01 FIT/Mb\(^2\))
  - On-die termination (ODT) to reduce board complexity
  - De-skew training\(^3\) to improve signal-capture timing
- **Specifications**
  - I/O Levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD\(^4\))
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **RoHS\(^5\)-Compliant Package**
- **Package:** 361-ball flip-chip ball grid array (FCBGA)

Collateral
- **Datasheets:** CY7C4121KV13/CY7C4141KV13

Family Table

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>Maximum Frequency</th>
<th>RTR</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDR-IV HP</td>
<td>72Mb 144Mb</td>
<td>CY7C40x1KV13</td>
<td>667 MHz</td>
<td>1,334 MT/s</td>
</tr>
<tr>
<td>QDR-IV XP</td>
<td>72Mb 144Mb</td>
<td>CY7C40x2KV13</td>
<td>1,066 MHz</td>
<td>2,132 MT/s</td>
</tr>
</tbody>
</table>

QDR-IV

<table>
<thead>
<tr>
<th>Control Logic</th>
<th>Test Engine</th>
<th>Address Interface</th>
<th>Data Port A (HSTL/SSTL or POD)</th>
<th>Data Port B (HSTL/SSTL or POD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Inversion</td>
<td>x2</td>
<td>Address Parity</td>
<td>Data Valid</td>
<td>Data Valid</td>
</tr>
<tr>
<td>Address Control Clock</td>
<td>x2</td>
<td>ECC</td>
<td>Data Clocks</td>
<td>Data Clocks</td>
</tr>
<tr>
<td>JTAG Interface</td>
<td>x4</td>
<td>Parity Error</td>
<td>x2</td>
<td>x2</td>
</tr>
</tbody>
</table>

Collateral
- **Production:** Now

1. Two data transfers per clock cycle
2. The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
3. An iterative algorithm for assessing and eliminating the skew (differences in arrival times) between data signals
4. Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up

CYPRESS EMBEDDED IN TOMORROW

Product Overview
Synchronous SRAM with On-Chip ECC

**Applications**
Switches and routers, radar and signal processing, test equipment, automotive, military and aerospace systems

**Features**
- **New Features**
  - Available in two modes: Pipeline and Flow-Through
  - SCD and DCD deselect options
  - Error-correcting code (ECC) to detect and correct single-bit errors
- **Specifications**
  - Voltage options: 2.5 V and 3.3 V
  - Bus-width configurations: x18 and x36
  - Industrial and commercial temperature grades
  - Military temperature grade: -55°C to +125°C
- **Packages**: 165-ball BGA (w/ and w/o leaded balls) and 100-pin TQFP

**Collateral**
Datasheets: CY7C135XKV33/CY7C136XKV33
CY7C137XKV33/CY7C138XKV33
CY7C144XKV33/CY7C146XKV33

**Family Table**

<table>
<thead>
<tr>
<th>Option</th>
<th>Density</th>
<th>MPN</th>
<th>RTR</th>
<th>FIT/Mb³</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Sync with ECC Pipeline</td>
<td>9Mb</td>
<td>CY7C1360/2K</td>
<td>250MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td>CY7C1370/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>CY7C1440/2K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Sync with ECC Flow-Through</td>
<td>9Mb</td>
<td>CY7C1361/3K</td>
<td>133MT/s</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>18Mb</td>
<td>CY7C1371/3K</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>36Mb</td>
<td>CY7C1441/3K</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Availability**
Production: Now

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1 Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
2 Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
3 The projected failure rate of a device. One FIT/Mb equals one failure per billion device hours per megabit of data
Fast SRAM Family with PowerSnooze

Applications
Programmable logic controller, handheld devices, multifunction printers, computation servers and automotive

Features
- Error Detection and Correction
  - Error-correcting code (ECC) logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- Specifications
  - Access time: 10 ns
  - Deep-sleep current: 15 µA for 4Mb
  - Bus-width configurations: x8, x16, and x32
  - Industrial and automotive temperature grades
  - Military temperature grade: -55°C to +125°C
- Packages: 48-ball BGA (w/ and w/o leaded balls)

Collateral
Datasheets: CY7S1049G/CY7C1049G
CY7S1051H/CY7C1051H
CY7S1061G/CY7C1061G

Family Table

<table>
<thead>
<tr>
<th>Density</th>
<th>MPN</th>
<th>Access Time</th>
<th>Deep Sleep Current (maximum at 85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4Mb</td>
<td>CY7S104x</td>
<td>x8</td>
<td>10 ns</td>
</tr>
<tr>
<td>8Mb</td>
<td>CY7S105x</td>
<td>x16</td>
<td>10 ns</td>
</tr>
<tr>
<td>16Mb</td>
<td>CY7S106x</td>
<td>x32</td>
<td>10 ns</td>
</tr>
</tbody>
</table>

Fast SRAM with PowerSnooze

Collateral
Datasheets: CY7S1049G/CY7C1049G
CY7S1051H/CY7C1051H
CY7S1061G/CY7C1061G

Availability
Production: Now

1 A Fast SRAM with a deep-sleep mode in addition to a conventional standby mode.
16Mb Parallel nvSRAM

**Applications**
Industrial automation, programmable logic controllers, gaming machines, industrial data logging, telecom equipment, networking and storage

**Features**
- **Fast Nonvolatile Memory**
  - Access time (25 ns)
  - Optional real-time clock (RTC) functionality
  - Available in parallel and open NAND Flash Interface (ONFI) Version 1.0 interfaces
  - Unlimited read/write endurance
  - One million store cycles on power fail
- **Specifications**
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- **Packages**: 44-pin TSOP, 54-pin TSOP, 165-ball BGA (w/ and w/o leaded balls)

**Collateral**
Datasheet: CY14X116L/CY14X116N/CY14X116S

**Availability**
Sampling: Now
Production: Contact Sales

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1. Crystal connection input
2. Crystal connection output
3. Interrupt output/calibration/square wave
4. External capacitor connection
5. Hardware STORE busy
2Mb / 1Mb Military SPI F-RAM

Applications
Multifunction printers, industrial controls and automation, medical wearables, test and measurement equipment, smart meters, aerospace and defense applications, missiles and launchers

Features
- Ultra-Low Power Memory
  - 40-MHz SPI interface
  - 100-trillion read/write cycle endurance
- Specifications
  - Operating voltage range: 2.0–3.6 V
  - Low (20-µA) sleep current at +125°C
  - 100 years data retention at +85°C
  - Military temperature grade: -55°C to +125°C
- Packages: 8-pin TDFN and 8-pin SOIC

Collateral
Datasheet: CY15B102Q

Availability
Sampling: Now (1Mb)
Production: Now (2Mb) / Q4’19 (1Mb)
64Mb/128Mb/256Mb/512Mb/1Gb/2Gb Parallel NOR Flash

Applications
- Military systems boot memory
- Avionics boot memory

Features
- High-Reliability Boot Flash Memory
  - 100 program1/sector erase2 endurance cycles3 at +125°C
  - >10 years data retention at +125°C
- Specifications
  - Operating voltage range: 2.7–3.6 V
  - Initial access time: 120 ns
  - Page access time: 15 ns
  - Program time (512B): 0.4 ms (typical)
  - Sector erase time (128KB): 410 ms (typical)
  - Military temperature grade: -55°C to +125°C
- Packages: 64-ball fortified4 BGA (9 x 9 mm and 13 x 11 mm, w/ and w/o leaded balls)

Collateral
Datasheet: S29GLXXXS (128M/256M/512M/1G)

Availability
Samples: Now (1Gb, 2Gb, 64Mb)
Production: Now (128Mb/256Mb/512Mb) / Q4’19 (1Gb) / Q4’19 (2Gb) / Q4’19 (64Mb)

1 The operation required to change a NOR Flash memory cell state from “1” to “0”
2 The operation in which all the bytes in a sector of NOR Flash memory are erased simultaneously prior to programming
3 The number of times a NOR Flash memory sector can be programmed or erased before it wears out
4 Fortified BGA supports a 1-mm ball pitch
5 Write protect input
6 Ready/busy output
128Mb/256Mb/512Mb/1Gb SPI NOR Flash

Applications
Military systems boot memory
Avionics boot memory

Features
- High-Reliability Boot Flash Memory
  - 100 program\(^1\)/sector erase\(^2\) endurance cycles\(^3\) at +125°C
  - >10 years data retention at +125°C
- Specifications
  - Operating voltage range: 2.7–3.6 V
  - Single data rate (SDR)\(^4\) clock rate: 104-MHz quad input/output (QIO)\(^5\)
  - Double data rate (DDR)\(^6\) clock rate: 80-MHz QIO
  - Program time (512B): 0.340 ms (typical)
  - Sector erase time (256KB): 520 ms (typical)
  - Military temperature grade: -55°C to +125°C
- Packages: 24-ball BGA (6 x 8 mm, w/ and w/o leaded balls)

Collateral
Datasheets: S25FL512S (512Mb)
S25FL128/256S (128Mb/256Mb)

Availability
Sampling: Now (1Gb)
Production: Now (128/256/512Mb) / Q4'19 (1Gb)

Notes:
1 The operation required to change a NOR Flash memory cell state from "1" to "0"
2 The operation in which all the bytes in a sector of NOR flash memory are erased simultaneously
3 The number of times a NOR Flash memory sector can be programmed/erased before it wears out
4 A mode of data transfer in which data is transferred once per clock cycle
5 An interface that transfers addresses or data on four I/O’s simultaneously
6 A mode of data transfer in which data is transferred twice per clock cycle
7 Signals used for standard Quad (x4) SPI interface. Refer to the S25FL512S datasheet for signal definitions in the x1 and x2 mode.
8 RESET# is an optional signal available on 16-pin-SOC and BGA packages