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AN214925

CYW4329: Power Topologies

Associated Part Family: CYW4329

This application note documents the regulator resources provided by the CYW4329 and provide details on the various power topologies available to optimally match these resources with the requirements of the target host system. The application note addresses the production version of the CYW4329.

Contents

1 About This Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4329	CYW4329

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Introduction

The CYW4329 has been designed to meet the varied and demanding requirements of embedded systems such as cellular and smart phones, music players, game devices, and other mobile systems. These systems require a WLAN/Bluetooth® solution that has low power consumption, low cost, and a small foot print. The systems can also vary widely in the power supply rails they have available to the WLAN/Bluetooth subsystem.

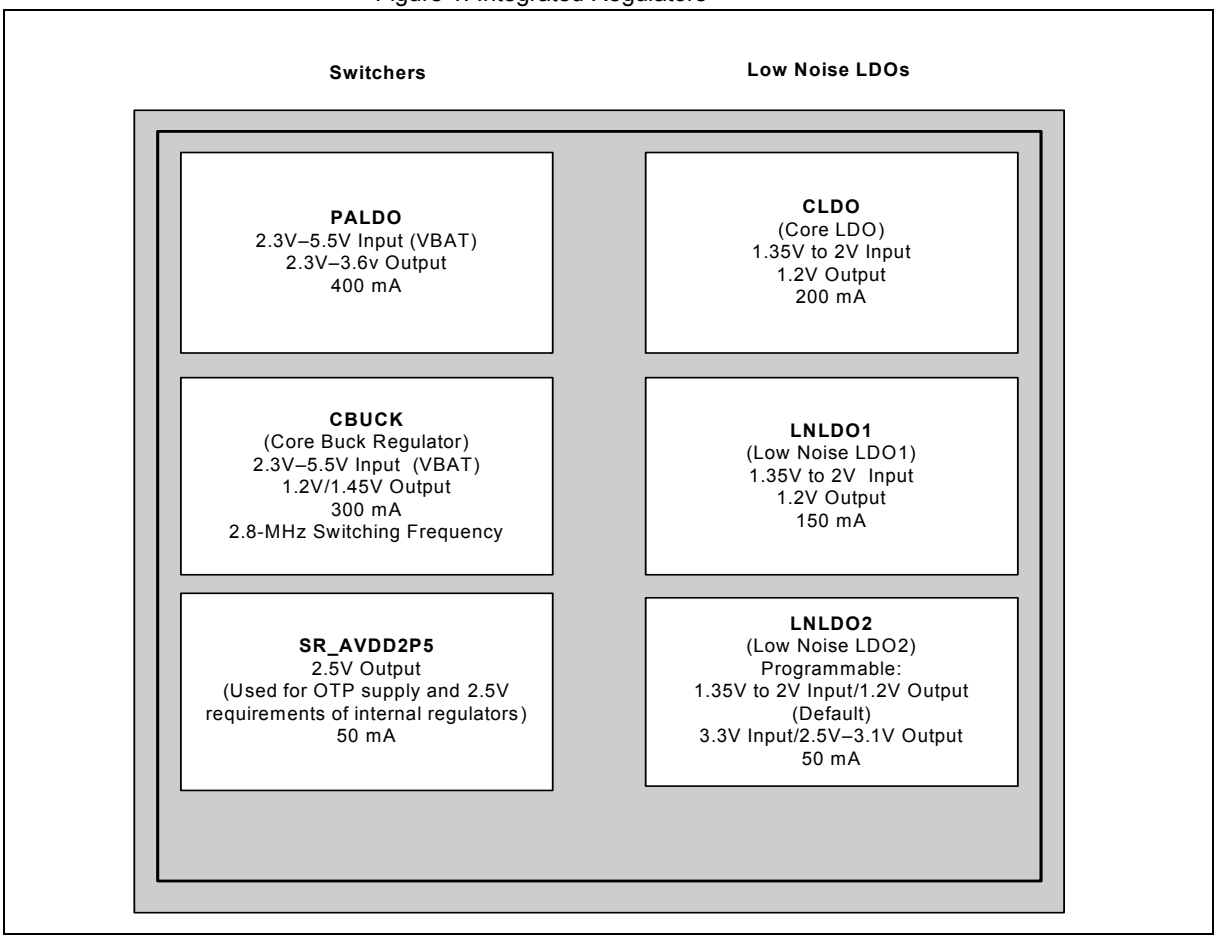
The CYW4329 addresses these requirements by providing a comprehensive set of integrated switching and linear regulators. All of the regulators are independent and have their inputs and outputs brought out to pins on the CYW4329. This functionality enables each regulator to be used or bypassed to optimally match the resources and needs of the target system.

For example, if a system has only VBAT (battery voltage, 2.3V to 5.5V) available for the CYW4329, a combination of integrated CYW4329 regulators can be used to provide all of the voltages needed by the WLAN/Bluetooth subsystem, all of which are derived from VBAT. Conversely, if a system already has a 3.3V and 1.2V rail available to the CYW4329, then most of the CYW4329 regulators can be bypassed and the host-supplied rails can be used directly. This technique allows the number of external components in the CYW4329 circuit to be reduced.

4 CYW4329 Integrated Regulators

Figure 1 illustrates the CYW4329 integrated regulators. Integrated regulators include the CBUCK switcher and the following linear regulators: CLDO, LNLDO1, LNLDO2, and PALDO. There is also an additional 2.5V LDO (SR_AVDD2P5) that is used primarily to supply 2.5V to the internal regulators and for the CYW4329 OTP block. The inputs and outputs of the regulators are both brought out to CYW4329 pins, allowing the designer to use or bypass the regulators as is appropriate for the target platform. If LNLDO1 or LNLDO2 are not used, their input pins should be grounded and their outputs left floating. If CLDO is not used, *and* CBUCK is still being used, the CLDO input pin should still be connected to the CBUCK LC node output. This requirement is because the CLDO input pin is used internally as a voltage feedback sense for CBUCK. If PALDO is not used, its input pin (VDDBAT3) should still be connected to VBAT, and its output can be left floating. If CBUCK is not used, its inputs (VDDBAT1,2) should be connected to VBAT/3.3V. Its outputs should be left floating. Also note that if CBUCK is not used, then there needs to be a 4.7 µF input capacitor near the inputs of CLDO and LNLDO1. The external power supply trace that feeds these regulators should have an ESR of less than 50 mohms. The PALDO regulator is used to supply the WLAN PA and the Bluetooth PA. Its output is nominally 3.3V. When its input drops below 3.3V, the PALDO output will follow the input down. Note that the PALDO is off when the CYW4329 is initially powered on. It must be turned on by software after bootup.

Figure 1. Integrated Regulators



5 CYW4329 Power Supply Requirements

The CYW4329 requires the following voltages to operate: 3.3V, 2.5V, 1.2V, 1.8V, and VDDIO (I/O power supply).

5.1 3.3V Supply

The 3.3V rail is used primarily for the integrated WLAN power amplifier. It is also used for the VDDIO_RF pins, which are explained later in more detail. This supply could also be used for the generic VDDIO and VDDIO_SD supplies if the host uses 3.3V signaling. Finally, it is also used to supply the Bluetooth PA for Class 1 designs. If 3.3V is supplied externally (PALDO not used), the supply should be capable of supporting 260 mA loads (with 450 mA peaks with durations of several milliseconds).

5.2 2.5V Supply

The CYW4329 requires a 2.5V supply for its OTP (One-Time Programmable memory) block. This 2.5V supply is generally derived using the CYW4329 on-chip SR_AVDD2P5 regulator, so an external 2.5V supply is not required. Note that the SR_AVDD2P5 regulator is used for OTP and the CYW4329 switching regulators.

5.3 1.8V Supply

An external, clean 1.8V supply capable of 5 mA is used for the FM Tx block in the CYW4329.

5.4 1.2V Supplies

Two types of 1.2V supplies are required. The first is a basic 1.2V supply, which is used to provide power to the digital logic portions of the CYW4329. It also provides power to the noise-insensitive blocks in the CYW4329 radio blocks. The second 1.2V supply must be a clean filtered supply, as it provides power to the noise-sensitive blocks (in the CYW4329) such as the radios, AFEs, LNAs, and clock circuits. If FM is required by the system, then an

additional filtered 1.2V rail is required for the FM Rx circuitry. If 1.2V is provided externally (CLDO, LNLDO1, and so on, are not used), the external supply should be capable of 250 mA loads.

5.5 VDDIO Supplies

There are three types of VDDIO (I/O power supplies) in the CYW4329. The first, which is generally labeled VDDIO, is for the generic digital I/Os in the chip. This covers most of the I/Os including the GPIOs, reset lines, Bluetooth I/O supplies, and so on. The second I/O supply is the VDDIO_SD supply. This supply provides power just to the SDIO/SPI interfaces I/O pads. Finally, the VDDIO_RF supply provides power to the I/Os that control external RF components such as the SP3T RF switch used to select which RF function (Bluetooth transmit, WLAN transmit, BT/WLAN receive) is connected to the antenna. These three separate I/O supplies give the CYW4329 additional flexibility in adapting to a given system. For example, generic I/Os could use 1.8V signaling, whereas the SDIO interface could function at 3.3V. The most common configuration is likely to be 1.8V signaling for the generic I/Os and SDIO interface (VDDIO and VDDIO_SD), with 3.3V signaling for the VDDIO_RF I/Os. This configuration is the most common because most RF switches do not support control voltages as low as 1.8V. Total I/O currents are less than 10 mA.

Note: The currents listed above are conservative values that are intended for sizing power supplies. They are not appropriate for battery life estimation as they do not represent the lower typical currents seen in normal or low-power operation. Contact your Cypress representative for the latest current consumption numbers appropriate for battery life estimation.

6 FM Supplies

If FM is required in a target design, the FM Rx circuitry needs a dedicated filtered 1.2V supply for optimal performance. Cypress recommends using LNLDO2 (configured by software for 1.2V output) for this purpose. An external, clean 1.8V supply is used for the FM Tx block.

If FM is not required in a design, the FM pins should be configured as follows:

- No bypass capacitors are required if FM is not used.
- All FM ground pins should be connected to ground.
- All FM supply pins should be connected to 1.2V. This supply does *not* need to be a dedicated filtered 1.2V supply because the FM will not be functional. Consequently, LNLDO2 can be left for other uses, and an already existing shared 1.2V can be used for the FM supply pins, including the FM Tx supply.
- All other FM pins will be left floating (NO_CONNECT).

7 Initializing the LNLDO2 Regulator

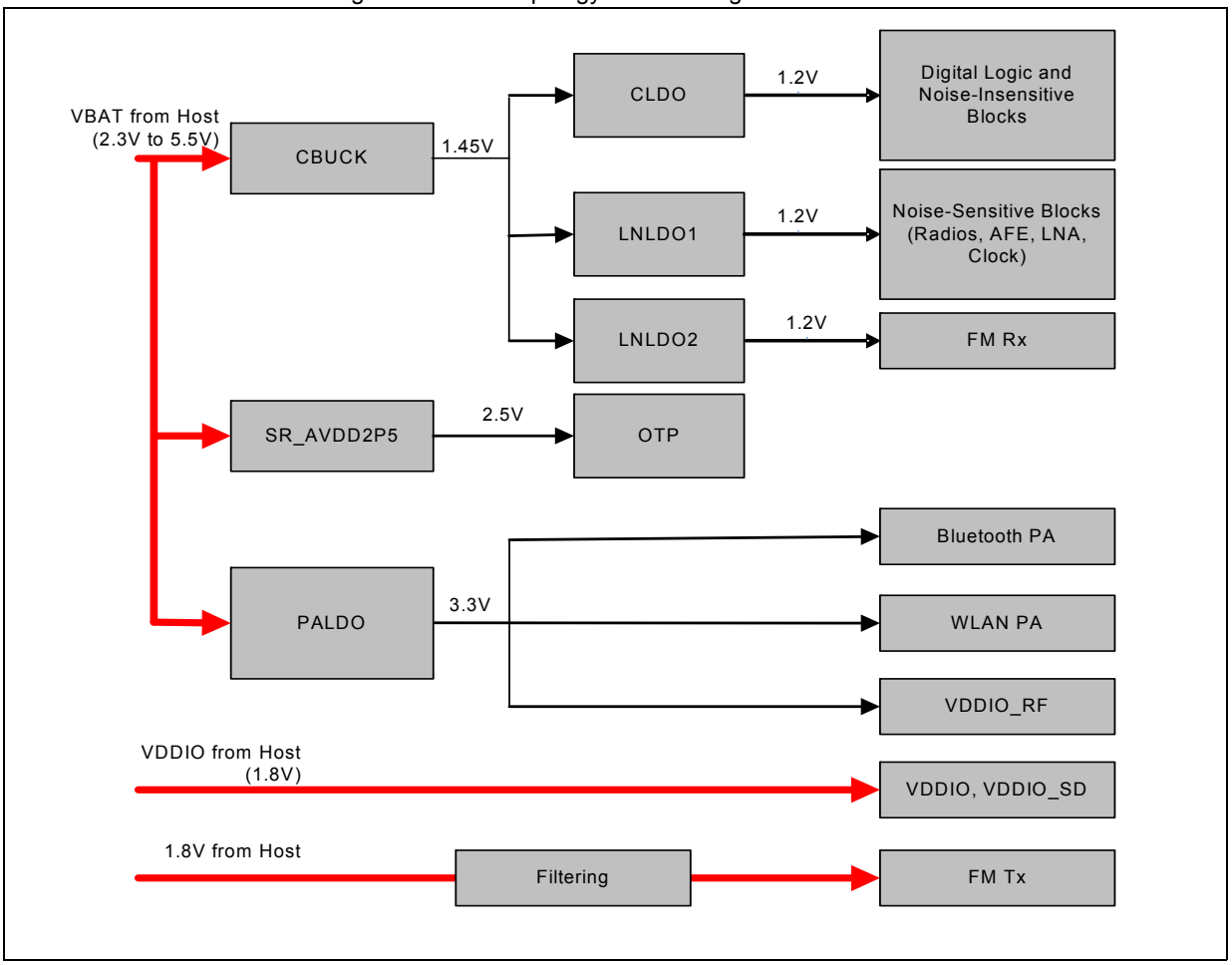
The LNLDO2 regulator is controlled by the Bluetooth core via a configuration file. By default, LNLDO2 is set for 1.2V output and is DISABLED. The Bluetooth configuration file must program the LNLDO2 to enable it.

8 Power Topologies

8.1 Power Topology 1: VBAT with FM and Class 1 Bluetooth

In this power topology (see Figure 2), the host provides VBAT (2.3V to 5.5V), 1.8V, and VDDIO (typically 1.8V). The topology uses the CYW4329 CBUCK, PALDO, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that do not have 3.3V or 1.2V regulated supplies that are available for the CYW4329 to use. It provides the best possible efficiency for such systems. The trade-off to this approach is that it requires a larger number of external components. This topology also assumes that the application needs FM support *and* Class 1 Bluetooth.

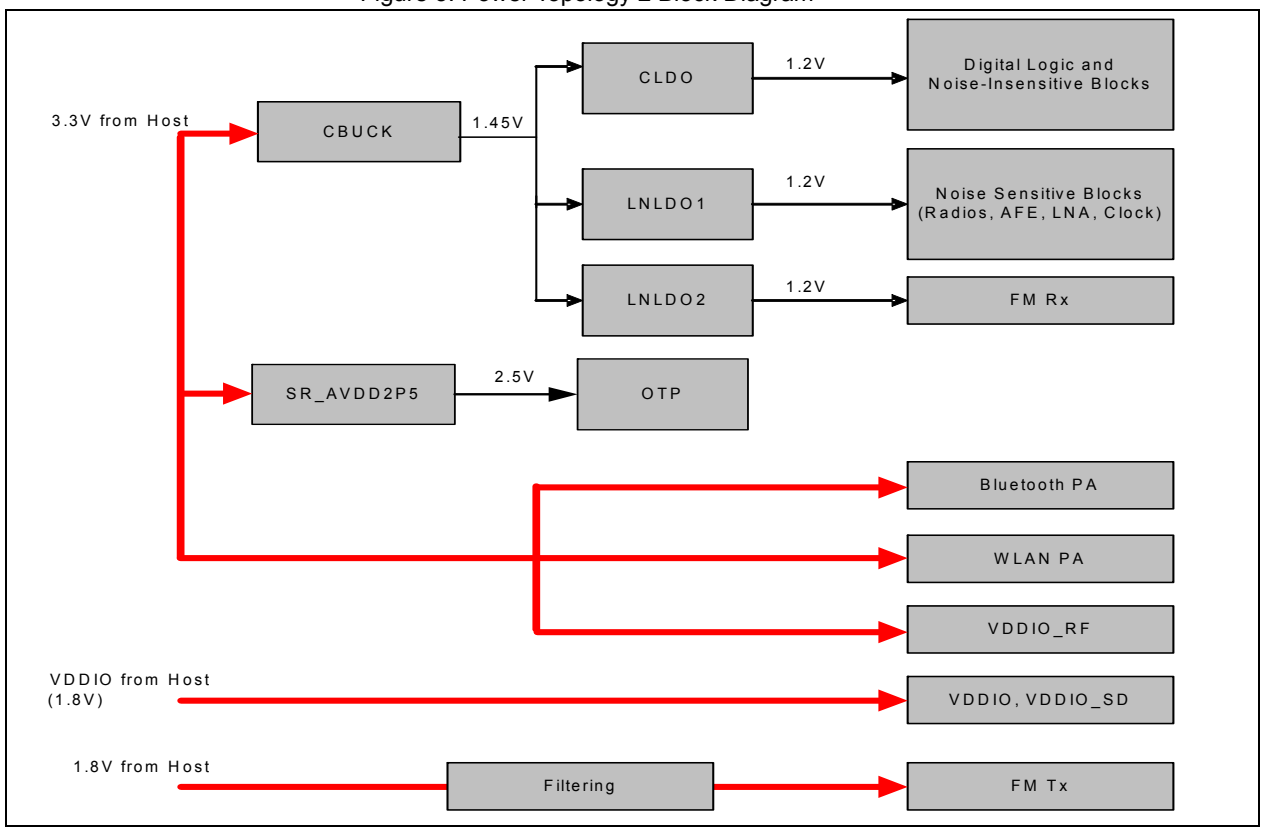
Figure 2. Power Topology 1 Block Diagram



8.2 Power Topology 2: Host Provides 3.3V, FM, and Class 1 Bluetooth Support

In this power topology (see Figure 3), the host provides only 3.3V, 1.8V, and VDDIO (typically 1.8V). The topology uses the CYW4329 CBUCK, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that have a regulated 3.3V rail with sufficient current allocated for the CYW4329 (direct support of VBAT is not required). The CYW4329 provides 2.5V and 1.2V regulated supplies using its integrated regulators. This topology provides high efficiency and has fewer external components than Topology 1. The topology assumes FM support, and Class 1 Bluetooth support. There is another variation of this topology for applications where the 3.3V supply of the host does not have enough load capacity to supply both the CBUCK and WLAN PA. In this case, an alternate topology could be used where the 3.3V supply of the host is used for the WLAN PA and VBAT is used to supply CBUCK.

Figure 3. Power Topology 2 Block Diagram

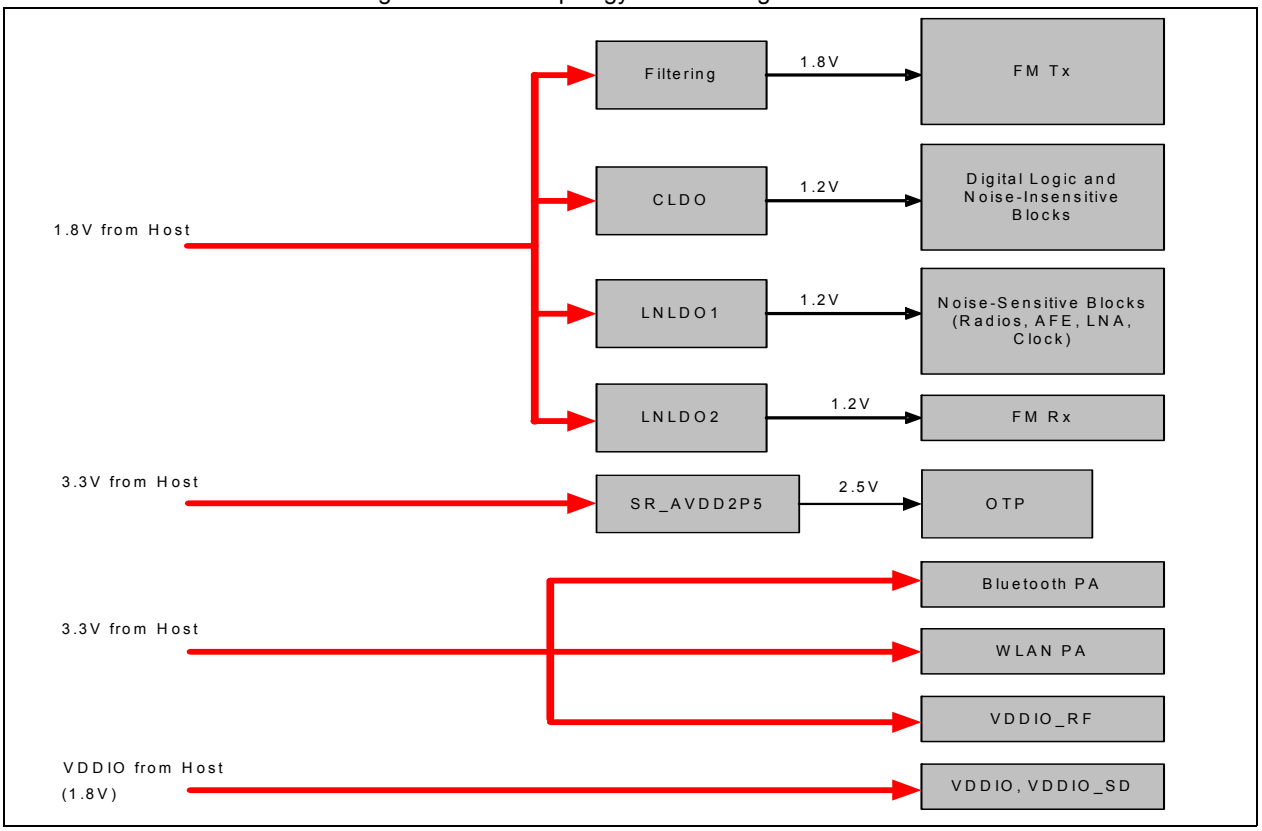


8.3 Power Topology 3: Host Provides 3.3V and 1.8V, FM, and Class 1 Bluetooth Support

In this power topology (see Figure 4), the host provides regulated 3.3V and 1.8V supplies. The 1.8V rail, however, is not just for VDDIO. It also has enough current to directly feed the CYW4329 1.2V LDO inputs. This capability results in a reduction of external components as the CYW4329 CBUCK regulator is no longer used. The trade-off for this approach is that it will be less efficient because the voltage drop from 1.8V to 1.2V is handled completely by linear regulators. This functionality is in contrast to Topologies 1–2, in which the CBUCK outputs 1.45V, and the less efficient LDOs only have to drop the voltage from 1.45V to 1.2V. This topology assumes FM support and Class 1 Bluetooth support.

Also note that, as an example, this topology uses a 1.8V host supply as the input for the CLDO, LNLDO1, and LNLDO2 regulators. However, these regulators support a range of input voltages. As long as it has enough current available, a host supply rail at any voltage from 1.4V to 2V could be used to feed these regulators. Lower voltages have the benefit of improved efficiency.

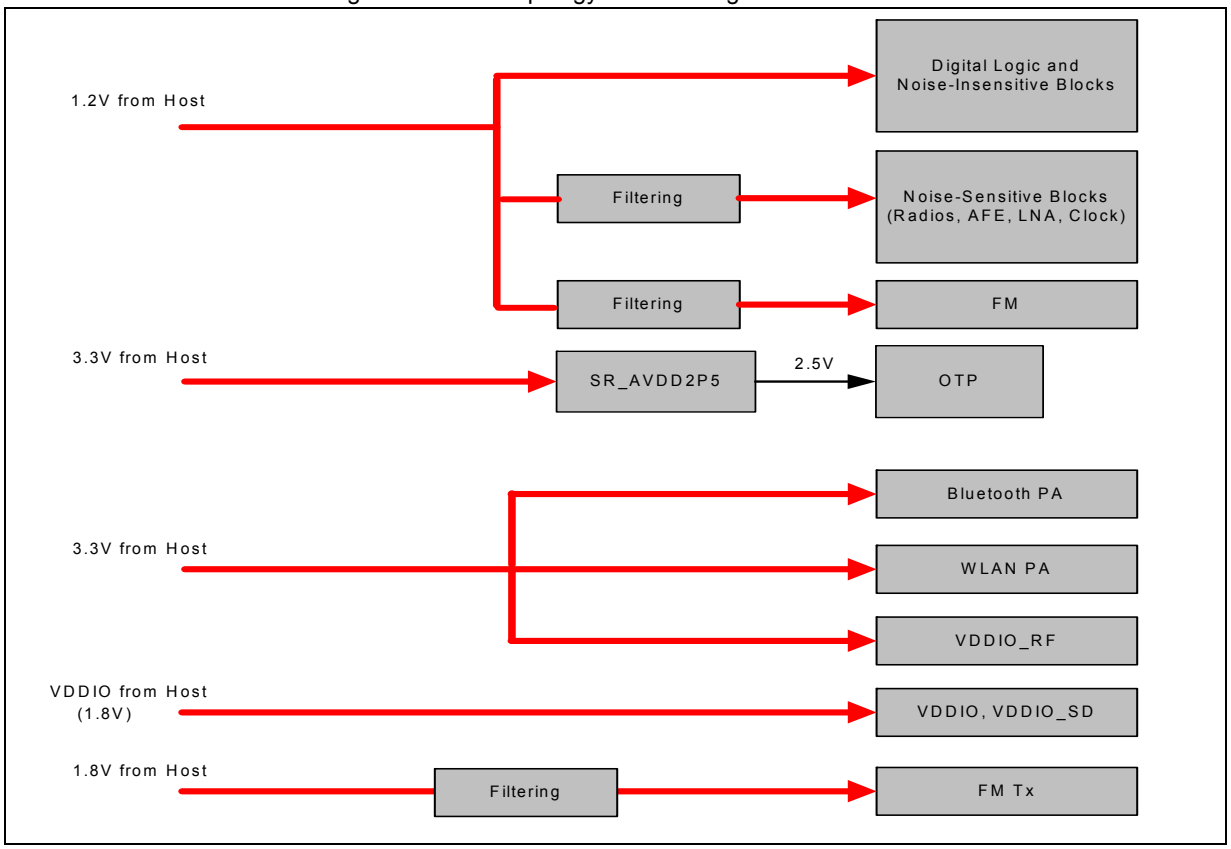
Figure 4. Power Topology 3 Block Diagram



8.4 Power Topology 4: Host Provides 3.3V, 1.8V, and 1.2V, FM, and Class 1 Bluetooth Support

In this power topology (see Figure 5), the host provides regulated power rails for 3.3V, 1.8V (for VDDIO and FM Tx), and 1.2V supplies. The host-supplied 1.2V rail directly feeds the 1.2V digital logic and noise-insensitive blocks of the CYW4329. This 1.2V rail is also filtered and then used to provide 1.2V to the noise-sensitive (radio, AFE, LNA, and so on) portions of the CYW4329. FM support is also provided, and the FM Rx core gets a dedicated filtered version of the host 1.2V supply. FM Tx gets a filtered 1.8V supply from the host. Effectively, all of the CYW4329 regulators (switching and LDOs) are bypassed except for the low-current LDO that outputs 2.5V for the CYW4329 OTP block. This topology is ideal for systems that have regulated 3.3V, 1.8V, and 1.2V supplies available (with sufficient load currents) that can be allocated to the CYW4329. It provides the lowest external component count and also provides the best efficiency. Other than the small 3.3V to 2.5V LDO for OTP, no other regulation occurs in the CYW4329 circuit. The end efficiency is based on the efficiency of the system regulators only. One trade-off to this approach is that the cleanliness of the 1.2V rail is critical because it does not benefit from the noise rejection characteristics of the CYW4329 on-chip LNLDOs. The topology assumes Class 1 Bluetooth support.

Figure 5. Power Topology 4 Block Diagram



9 Sequencing of Reset and Regulator Control Signals

The CYW4329 has four signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 6 and Figure 7 on page 9, Figure 8 and Figure 9 on page 10). The timing values indicated are minimum required values; longer delays are also acceptable.

Note that the WL_REG_ON and BT_REG_ON are ORed in the CYW4329. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the CYW4329 regulators.

Also note that the reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.

Note: The CYW4329 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the 0.6V threshold. Wait at least 110 ms after VDDC and VDDIO are available before initiating SDIO accesses. The external reset signals are logically ORed with this POR. So if either the internal POR or one of the external resets are asserted, the device will be in reset.

9.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU (along with BT_REG_ON) to decide whether to power down the internal CYW4329 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be disabled.
- **BT_REG_ON**: Used by the PMU (along with WL_REG_ON) to decide whether to power down the internal CYW4329 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be disabled.
- **WL_RST_N**: Low Asserting Reset for WLAN Core. This pin must be driven high or low (not left floating). *If WL_RST_N is low (regardless of BT_RST_N state), the WLAN core will be shut down*.
- **BT_RST_N**: Low asserting reset for Bluetooth core. This pin must be driven high or low (not left floating).

9.2 Control Signal Timing Diagrams

Figure 6. WLAN = ON, Bluetooth = ON

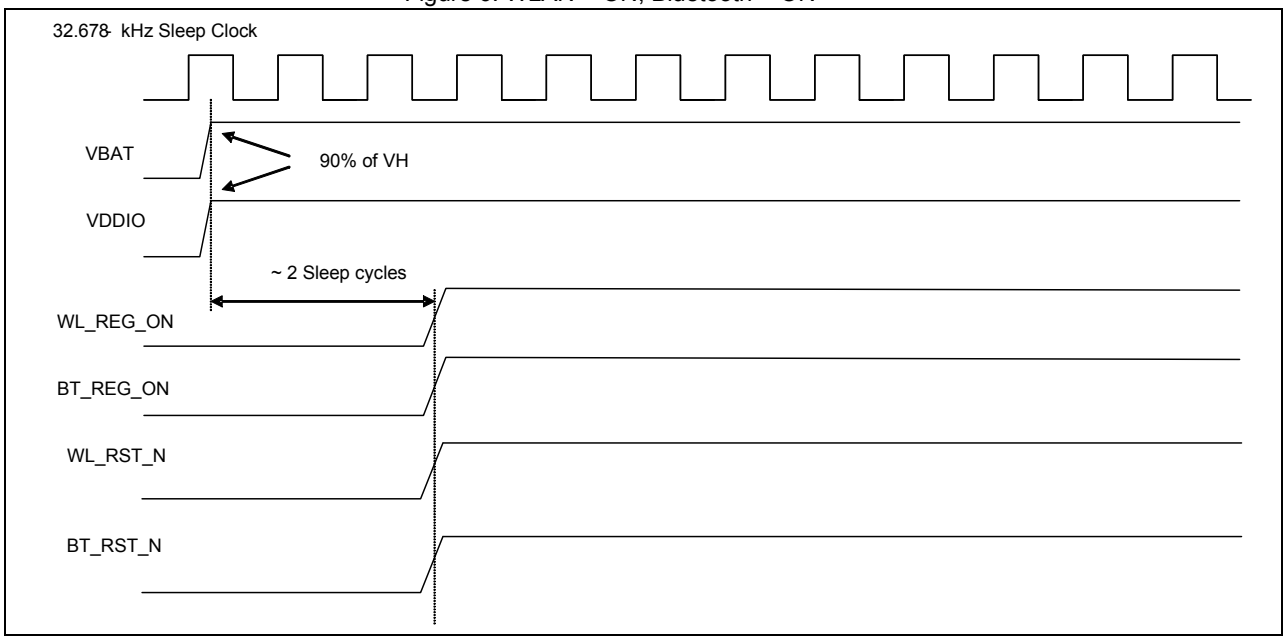


Figure 7. WLAN = OFF, Bluetooth = OFF

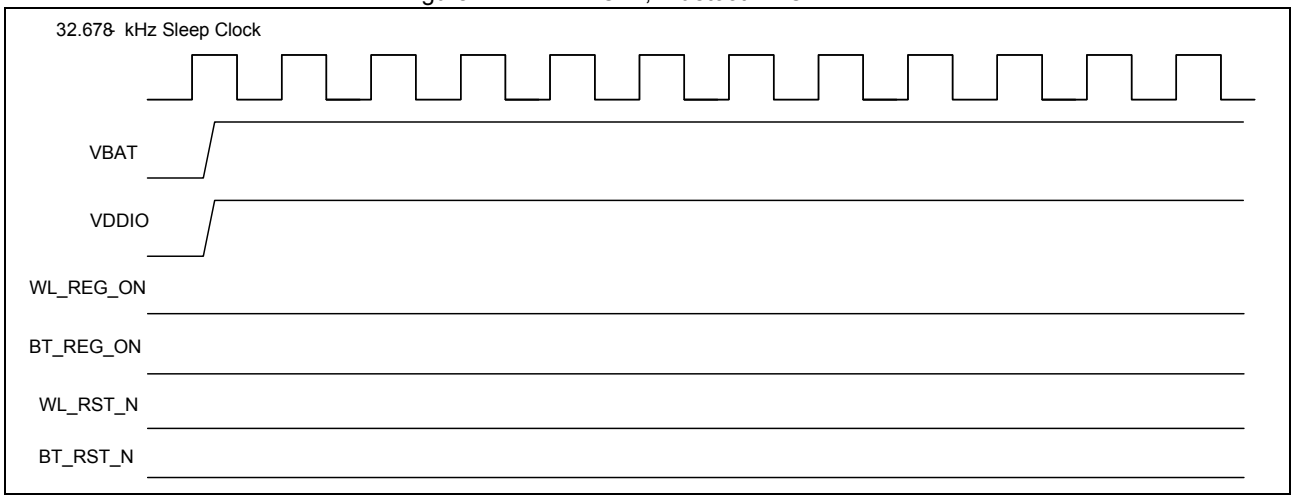


Figure 8. WLAN = ON, Bluetooth = OFF

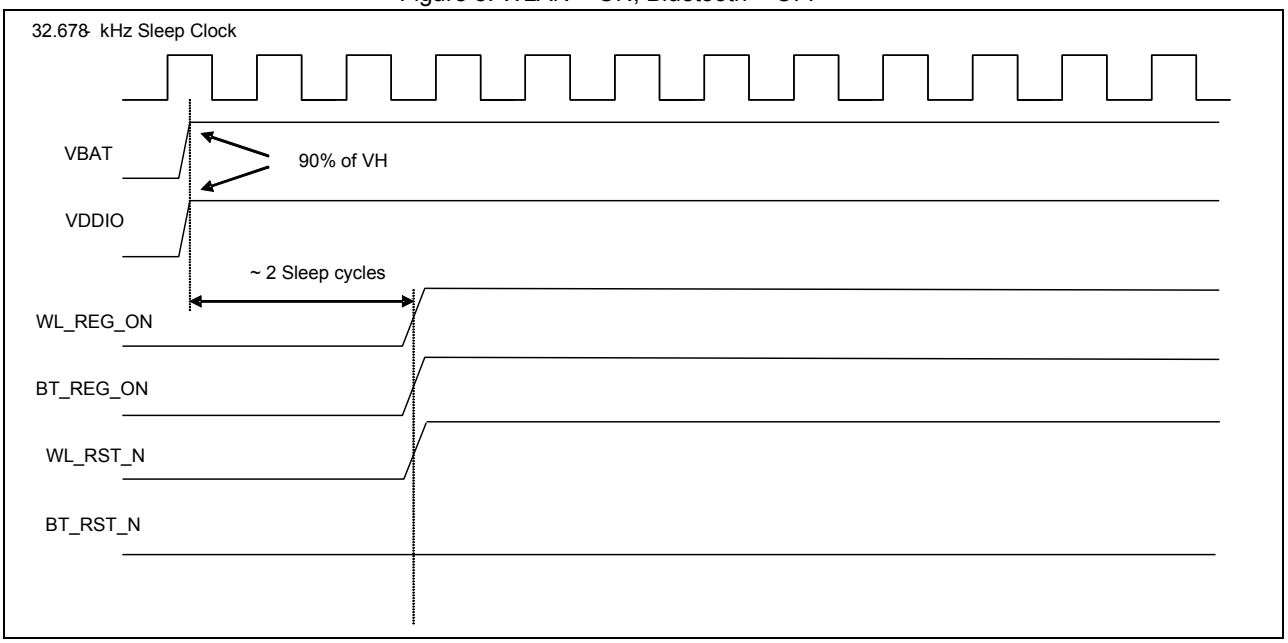
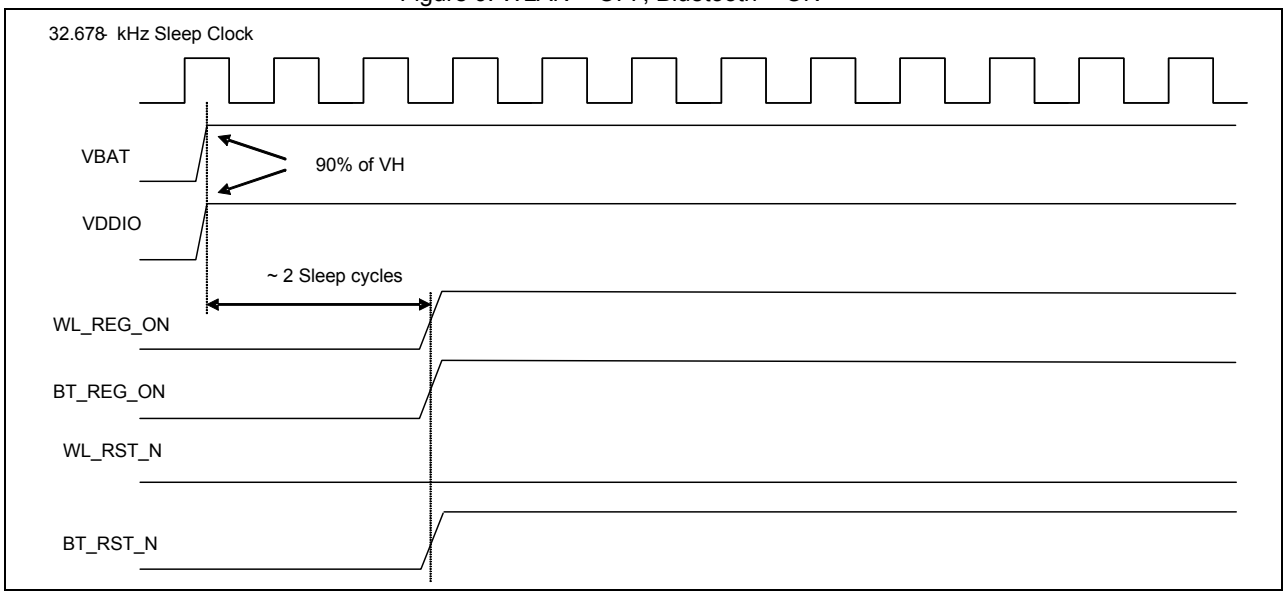


Figure 9. WLAN = OFF, Bluetooth = ON



10 Low Power States

The CYW4329 has four external controls lines, BT_RST_N, WL_RST_N, BT_REG_ON, and WL_REG_ON, in addition to clocks and power supplies that enable control of the state of the device. To cover all low power states, however, it is necessary to also include firmware control, which results when the WLAN driver, the Bluetooth Configuration file, or both are loaded. It is especially important to understand these states to be able to minimize current consumption in the end product.

The details of controlling the external control lines relative to clocks and supply rails have already been discussed earlier. The information in Table 2 explains each state and the associated required controls.

Table 2. Low Power States

State	State Description	Power[a]	Sleep CLK	REG_ON[b]	BT_RST_N	WL_RST_N	BT Config Loaded	WL Driver Loaded	FW Commands/ Comments	*Power Status* [c]
0	OFF (No Power)	OFF	OFF	LOW	LOW	LOW	NO	NO	–	Disabled (0 µA)
1	OFF (VBAT[d] + VDDIO enabled)	ON	Don't Care	LOW	Don't Care	Don't Care	NO	NO	–	Lowest power (typically <25 µA)
2	RESET	ON	ON	HIGH	LOW	LOW	NO	NO	–	Not low power[e] (typically 3 mA)
3	Default ON	ON	ON	HIGH	HIGH	HIGH	NO	NO	–	Not low power[f] (typically 5 mA)
4	ON (WL Only)	ON	ON	HIGH	HIGH	HIGH	NO	YES	WL Driver may be loaded before BT Config to read BD ADDR from OTP.	Application and FW dependent[f] Not low power
5	ON (BT Only)	ON	ON	HIGH	HIGH	HIGH	YES	NO	BT Config loaded. BD_ADDR set.	Application and FW dependent[g] Not low power
6	ON (BT + WL)	ON	ON	HIGH	HIGH	HIGH	YES	YES	BT Config loaded. BD_ADDR set.	Application and FW dependent[g] Not low power
7	BT & WL Sleep	ON	ON	HIGH	HIGH	HIGH	YES	YES	WL in Low power mode, BT in Sleep.	System Sleep (typically <250 µA)
8	WL Sleep (BT HW Rst)	ON	ON	HIGH	LOW	HIGH	NO[g]	YES	WL entered into low power mode.	WL sleep (typically <200 µA)
9	BT Sleep (WL HW Rst)	ON	ON	HIGH	HIGH	LOW	YES	NO[h]	BT entered into Sleep.	BT Sleep (typically <160 µA)

a. Power can be in applied in many possible topologies, which are not distinguished in the table. Therefore, if there are any questions about application power sequences that are not addressed, contact Broadcom support for assistance.

b. For the state table, "REG_ON" represents WL_REG_ON or BT_REG_ON. The signals are OR'd internal to the device.

c. Current values listed under **Power Status** are best estimates. Actual current values might vary, depending on the application design. Current values listed are combined VBAT and VDDIO values.

d. For this table, VBAT = 3.6V.

e. Although the device is held in hardware reset, the regulators are in the default state. The device must be controlled either from WL Driver or BT Config to transition to a controlled low power mode.

f. This table is not intended to detail all operating modes relative to software control and associated currents.

g. When BT_RST_N is transitioned to LOW the loaded BT config and any other HCI command settings will be lost.

h. When WL_RST_N is transitioned to LOW the loaded WL driver and any other WL specific commands will be lost.

The following example illustrates the transitioning from OFF to a WL Low-Power Sleep mode:

1. The device is OFF.
2. VBAT and VDDIO are applied (plus other voltage supplies relevant to the specific application).
3. Sleep CKLK enabled and REG_ON set to Logic High (note sequence in previous section of this document).
4. WL_RST_N set to logic High.
5. WL Driver is downloaded.
6. WL is commanded to transition to Low power.

10.1 Sequence for Transitioning CYW4329 to Bluetooth Sleep Mode

The CYW4329 can transition to Bluetooth Sleep mode only through the combined procedure of loading the configuration file and issuing a set of HCI commands, as shown in the following example. Although there are variants of Sleep mode operation, this example focuses on the most common model using external GPIOs for Host Wake and BT Wake (known as Sleep Mode 1).

Transition to Bluetooth Sleep Mode 1 (top-level steps):

1. From the OFF state, the device is powered into the ON state (with either WL_RST_N being high or low).
2. An HCI reset command is sent via the UART interface.
3. The UART baud rate is set for the application using an HCI Vendor-Specific command.
4. The Config file download process commences (a set of HCI is commands is required).
5. The BD ADDR is written to the device using an HCI Vendor-Specific command).
6. An HCI reset command is sent via the UART interface.
7. The HCI **Set_Sleepmode_Param** command is sent to the device.
   - This command sets the sleep mode (Sleep mode 1 "UART" uses GPIOs to wake the device from sleep and also to signal that the host is required to wake. Refer to application note BCM2048-AN600-R, *UART Sleep Mode Operation*, for more details).
   - BT WAKE polarity is essential to transitioning the device to sleep mode. The **Set_Sleepmode_Param** command allows you to set the polarity. If the device is to be in sleep when BT_Wake (BT_GPIO_0) is LOW, ensure that the polarity of BT_Wake is set to *Active High*.
8. Toggle the polarity of BT_Wake (BT_GPIO_0) to enter and exit sleep mode.

10.2 Sequence for Transitioning CYW4329 to WLAN Low-Power Sleep Mode

In the low-power sleep state, WLAN is not associated and does not wake up to listen for beacons. This is the lowest power consumption state for WLAN in which WLAN is not being held in reset, and power is being applied to the CYW4329. In this state, the system clock is disabled but the Sleep CLK is still running. The CYW4329 WLAN radio is disabled. Finally, the SDIO interface is put into Power Save mode.

To disable Bluetooth functionality and transition the WLAN operation to low-power Sleep mode:

1. From OFF, the device is powered into the WLAN ON state following the RST and REG_ON sequencing requirements described earlier.
2. Execute the following commands:

wl up

wl deepsleep 1

dhd idleclock stopped

11 Power Supply Layout Guidelines

Refer to the CYW4329 layout application note (4329-AN100R) for critical guidelines regarding layout and placement of the power supply section.

12 Switcher Inductor Recommendations

The following inductor is used for the CBUCK Cypress reference design: TDK VLF3010AT-3R3MR87.

The component benefits from having received the most extensive amount of testing at Cypress. It is understood, however, that some target systems have mechanical requirements that will require different inductors. This section describes critical items that must be considered when a substitute for these inductors is being considered. Note that complete qualification of an inductor requires more than a review of the data sheet. It also requires in-system component testing, which can be time consuming. We recommend using only the substitute parts that we have already evaluated (see Recommended Inductors for the CBUCK Regulator on page 14).

12.1 Inductor Specifications and Implications

The follow specifications are critical to proper switcher stability and functionality and *cannot* be compromised:

1. Nominal Inductance value:

- Usually measured at 1 MHz test frequency at 20°C.
- The nominal value for the CBUCK regulator is 3.3 μH.

2. Tolerance of nominal inductance value:

- L ≤ ±30%

3. The inductor for the CBUCK must not collapse to too low an inductance value causing the switcher to oscillate before the over-current limit protection activates. The inductor is nominally 3.3 μH and must be at least 1.5 μH at currents of 500 mA and across temperature. Because inductor data sheets typically show only "Inductance versus DC current" plots at nominal values, the plot should be shifted to account for the worst case tolerance (–30%, for example) of the part as well.

4. Inductor structure:

- Wire-wound or multilayered compound.
- Recent developments have seen new multilayered compound inductors, which are lower profile and have a smaller footprint compared to wire-wound inductors. Multilayered compound inductors are also typically less expensive. However, a big disadvantage with multilayered parts is that there is a significant droop in inductance over loads. Multilayered inductor data sheets typically show inductance droop versus DC loads. However, bench testing has shown that these inductors actually droop almost instantaneously in response to fast transient load levels.
- Some of the new ultralow-profile wire-wound inductors also exhibit inductance droop problems similar to the multilayered devices.
- Extensive bench testing with the actual switchers is required to ensure that these types of devices are suitable in presence of switcher transients.

The following specifications affect switcher efficiency. Design tradeoffs (smaller footprint at the cost of lower efficiency, for example) can be considered for these specifications:

- DCR (also known as Rdcor ESR) ≤ 200 mohm to avoid reduced efficiency (approximately 5% reduction). Make sure that DCR does not exceed 320 mohm.

Other specifications that depend on the requirements of the target system:

- Shielding (metal case/magnetic) versus nonshielding
- Footprint and height

12.2 Recommended Inductors for the CBUCK Regulator

The following inductors are recommended alternatives to use with the CBUCK regulator.

Table 3. Recommended Parts for Use with the CBUCK Regulator

Part No.	Mfgr	Dimensions (mm)			Inductance (µH)	Tolerance (± µH in %)	Maximum DCR (mohm)	Typical DCR (mohm)	Peak Efficiency (1.45V out, 3.3VBAT, 150-mA Load)	Notes	Isat Based on +40°C (mA)	Isat Based on 30% L Change (mA)
		W	L	H								
VLF3010AT-3R3MR87	TDK	2.6	2.8	1.0	3.3	20	170	150	90%	a	1000	870
CDRH2D18/HP-3R3NC	Sumida	3.0	3.0	2.0	3.3	30	86	69	90%	–	1550	1450
1117AS-3R3M	TOKO	2.8	3.0	1.0	3.3	20	156	130	–	–	1300	1200
MIPSA2520D3R3	FDK	2.5	2.0	1.2	3.3	30	156	120	87%	b	1000	–
VLS252010T-3R3M	TDK	2.0	2.5	1.0	3.3	20	304	253	–	c	940	1200
LQM31PN4R7M00	Murata	1.6	3.2	0.95	4.7	20	300	240	85%	d	800	–
LQM2HPN3R3MG0	Murata	2.0	2.5	0.9	3.3	20	125	100	–	b	1200	–
CPL2512T3R3M	TDK	1.5	2.5	1.2	3.3	20	312	240	85%	e	730	730
VLS3012T3R3M1R3	TDK	3.0	3.0	1.2	3.3	20	120	100	–	–	1700	1500
FLF3215T-3R3M	TDK	2.5	3.2	1.65	3.3	20	78	65	–	–	1600	1200
CDRH26D09NP-3R3PC	Sumida	2.8	2.6	1.0	3.3	25	260	208	85%	–	750	900

a.Used in Cypress reference designs.

b.Limited bench testing

c.Efficiency expected to drop by approximately 5% due to high DCR.

d.Efficiency drops by approximately 5% due to high DCR. The 4.7-µH inductor was chosen in this specific case so that the inductance of the component will be greater than 2 µH in spite of drooping at 700-mA loads.

e.Efficiency drops by approximately 5% due to high DCR.

12.3 Regulator Capacitor Considerations

When choosing capacitors for the CYW4329 regulators, it is important to make sure that across tolerance, temperature, and with aging that the capacitor continues to provide the minimum required capacitance required by the regulators. One factor that also needs to be considered is how the capacitor's value is affected by DC bias. If a capacitor is biased at a voltage close (3.3V bias is "close" to a 6.3V rating) to its rating, a significant drop in capacitance can occur. This DC bias effect can be particularly severe in smaller form factor capacitors. For cases where the DC bias is significant, it is recommended that the highest possible voltage rating is used when a capacitor is chosen. If a higher voltage rating is not available, a capacitor with a larger value can be used.

Table 4 lists the nominal and minimum required capacitance for each regulator. The nominal capacitance is the value listed by the capacitor vendor for a given part number. The minimum value is the actual capacitance after factoring in the following:

- Part-to-part variance (tolerance)
- DC bias capacitance droop effect
- Temperature capacitance droop effect

Because of these effects, there may be cases where a higher nominal value needs to be chosen to meet the minimum capacitance requirements. For example, If a the 6.8-µF capacitor chosen for the VBAT_Input droops below 3 µF due to the DC bias droop effect, then that device either needs to be changed for a 6.8-µF part with a higher voltage rating (and less DC bias droop) or for a part with a higher nominal capacitance, such as a 10 µF part.

Table 4. Nominal and Minimum Capacitance Requirements

Supply	Nominal Capacitance	Minimum Capacitance	Recommended Device
CBUCK output	4.7 µF	3 µF	TDK® C1608X5R0J475MT
PALDO output	3.3 µF	2.2 µF	Murata® GRM188R61A335KE15
CLDO output	4.7 µF	3 µF	TDK C1608X5R0J475MT
LNLDO1 output	4.7 µF	3 µF	TDK C1608X5R0J475MT
LNLDO2	1 µF	0.76 µF	Murata GRM155R61A105KE15
VBAT (SWR's shared input)	6.8 µF	4.7 µF	TDK C1608X5R0J685K

The following tools give a good simulation of Murata and TDK capacitors regarding effects of DC bias, and so on:

http://www.tdk.co.jp/eseat/

http://www.murata.com/designlib/mccdl/index.html

If the CBUCK regulator requires an alternate capacitor, see Table 5. The parts are listed in order of their preference. Any parts that are not on the list require Cypress approval.

Table 5. Recommended Parts for Usage of Alternate Capacitor with the CBUCK Regulator

Preference Order	*Part No.*	*Package*	*Dielectric*	*Capacitance* (µF)	*Tolerance* (%)	*Voltage Rating (V)*	*Mfgr*
1	GRM188R60J475ME84D	0603	X5R	4.7	20	6.3	Murata
2	GRM188R60J475ME19D	0603	X5R	4.7	20	6.3	Murata
3	GRM188R61A475KE15	0603	X5R	4.7	20	10	Murata
4	GRM155R60G106M	0402	X5R	10	20	4	Murata
5	ADK105BJ106MV_D	0402	X5R	10	20	4	Taiyo Yuden
6	This is a parallel combination of:						
a	GRM155R61A105K	0402	X5R	1	10	10	Murata
b	GRM155R60J475M	0402	X5R	4.7	20	6.3	Murata

12.4 Leakage Considerations

To achieve the lowest possible power consumption in low power modes, leakage current must be considered and minimized. The following are recommendations will aid in this goal:

- Avoid external pull-up or pull-down resistors:
  - 10 kilohm @ 3.3V = 330 µA, even 100 kilohm @ 3.3V is 33 µA
  - The CYW4329 has internal PU/PD resistors where necessary. These resistors can be turned off when not needed.
  - There are no internal PU/PD resistors on the xRST_N signals. These signals should always be driven from the host.
- Stop the host SDIO clock (or slow it down) for lowest power consumption.
- Consider external components such as LNAs and so on: How much current do they take in their bypass or disable modes?
- Consider shutting off the supply voltages of external components when they are not being used. This can be done using the PALDO output for their supply or by using an external FET enabled by XTAL_PU

13 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Cypress Items		
UART Sleep Mode Operation Application Note	BCM2048-AN600-R	CypressDeveloper Community
Other Items		
Seat 2010	http://www.tdk.co.jp/eseat/	
Murata Chip Capacitor Characteristics Data Library	http://www.murata.com/products/design_support/mccdl/index.html	

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**	–	–	12/22/2008	4329-AN200-R Initial release
*A	–	–	06/06/2011	4329-AN201-R Updated: Table 3, “Recommended Parts for Use with the CBUCK Regulator,” on page 14 Regulator Capacitor Considerations on page 15 Added: Table 5, “Recommended Parts for Usage of Alternate Capacitor with the CBUCK Regulator,” on page 15
*B	5464599	UTSV	11/23/2016	Updated in Cypress template Added Cypress part numbering scheme
*C	5881131	AESATMP9	09/12/2017	Updated logo and copyright.

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