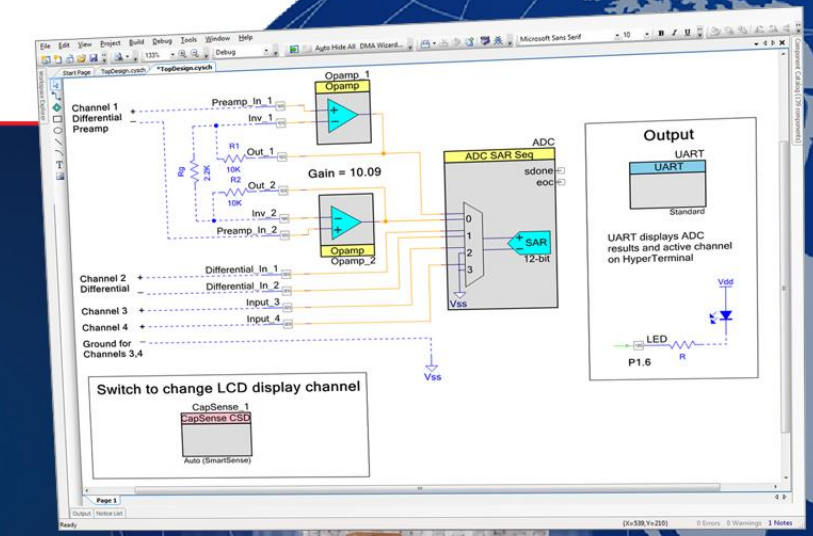
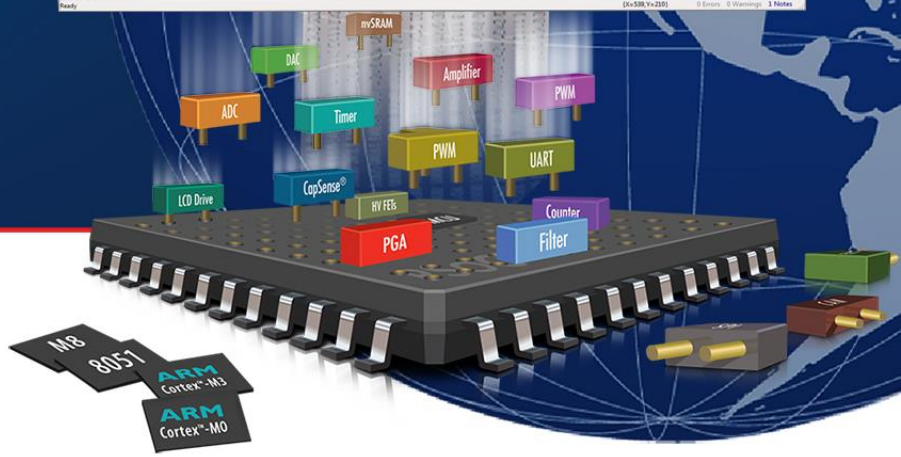
Techniques for EMC (Electro Magnetic Compatibility) countermeasure in Hardware





SHUS

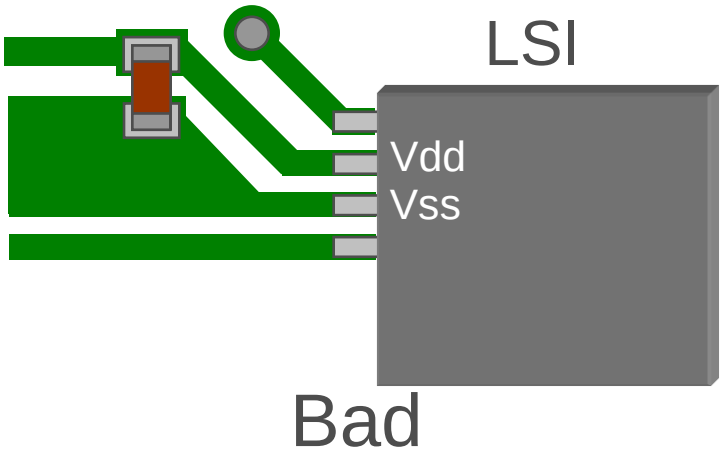
04/28/2016

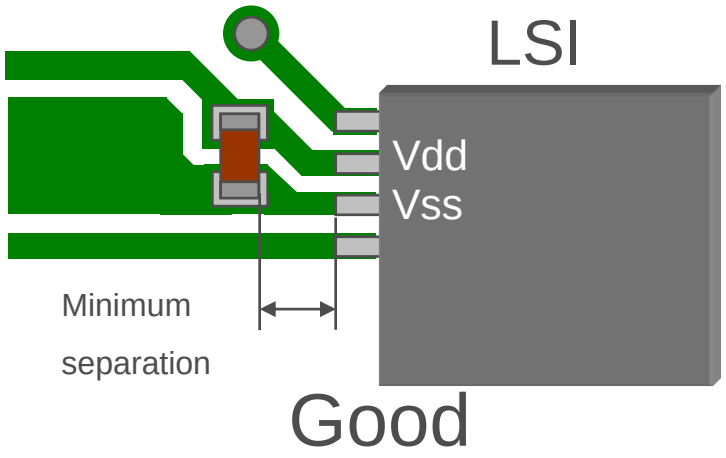
EMC Countermeasures in Hardware

1. Bypass capacitors (related to bypass capacitors)
2. GND patterns (related to GND patterns)
3. Power supply and GND wiring (related to power supply and GND wiring)
4. Pattern around oscillators
5. Countermeasures of MODE and Reset pin
6. Signal wiring
7. Global pins
8. Other

1. Bypass capacitors

1. Bypass capacitors (1)



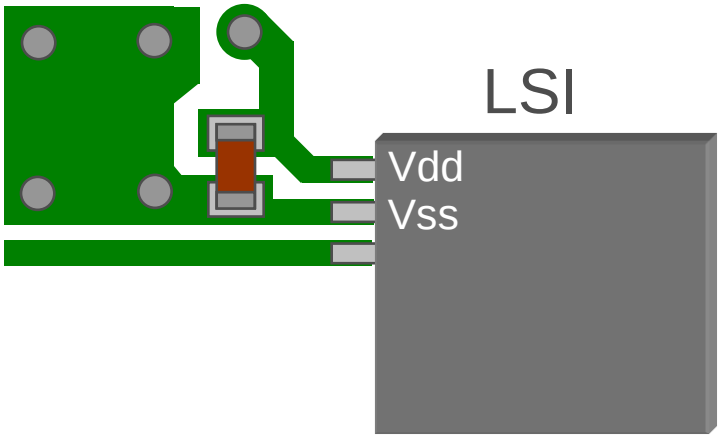


In to connect bypass capacitors with the LSI power and GND terminal, two effects of the following can look forward to it.

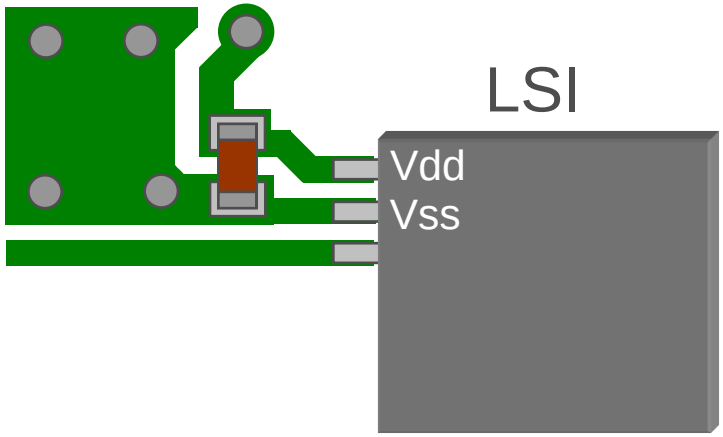
- It prevents a noise invasion into the LSI from the power line (The measure of EMS).
- It doesn't betray the noise which occurs to the power terminal of the LSI to the power line (The measure of EMI).

To get the effect, locate bypass capacitors as close as possible to the power supply and GND pins of the LSI.

1. Bypass capacitors (2)



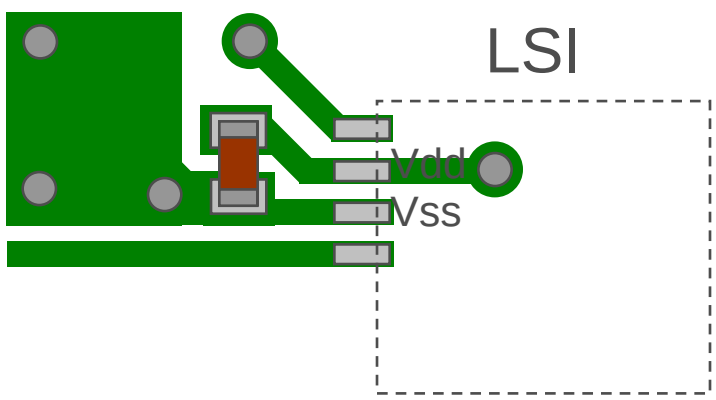
Bad



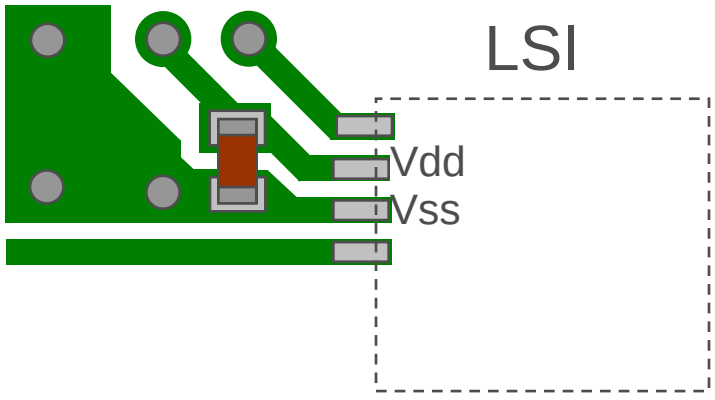
Good

It is important for power supply (Vdd, Vss) patterns to pass through both ends of the bypass capacitor with the least noise. In the bad example above, because there is a branch in the Vdd line between the LSI and bypass capacitor, the line passes through a point with a large amount of noise. This needs to be changed by shifting the Vdd line into the sequence LSI → bypass capacitor → branch point, as shown in the good example.

1. Bypass capacitors (3)



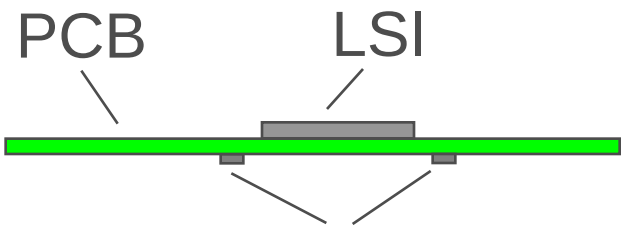
Bad



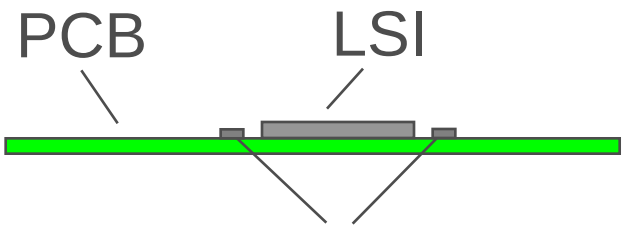
Good

In the bad example above, because the line does not form the sequence LSI → bypass capacitor → branch point, it passes through a point with large noise. This needs to be changed into the sequence LSI → bypass capacitor → branch point, as shown in the good example.

1. Bypass capacitors (4)



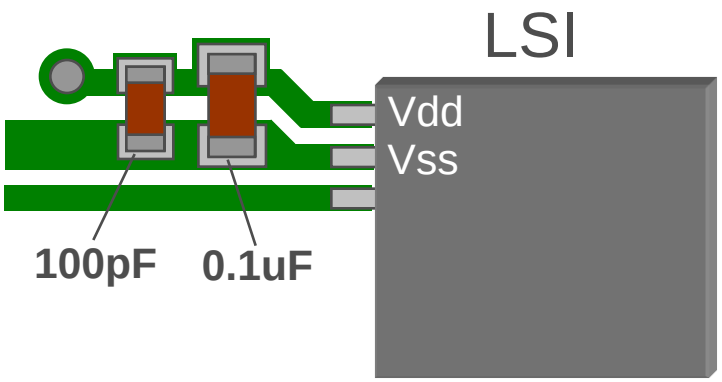
Bad



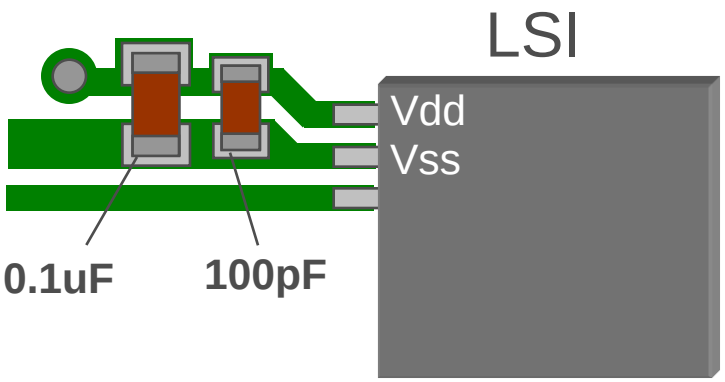
Good

If a bypass capacitor is located on the opposite surface (reverse side) of the PCB from the LSI mounting surface, the lines will be connected through a via, and the effectiveness of the bypass capacitor will be degraded due to the inductance component of the via. It is therefore best to locate bypass capacitors on the LSI mounting surface.

1. Bypass capacitors (5)



Bad

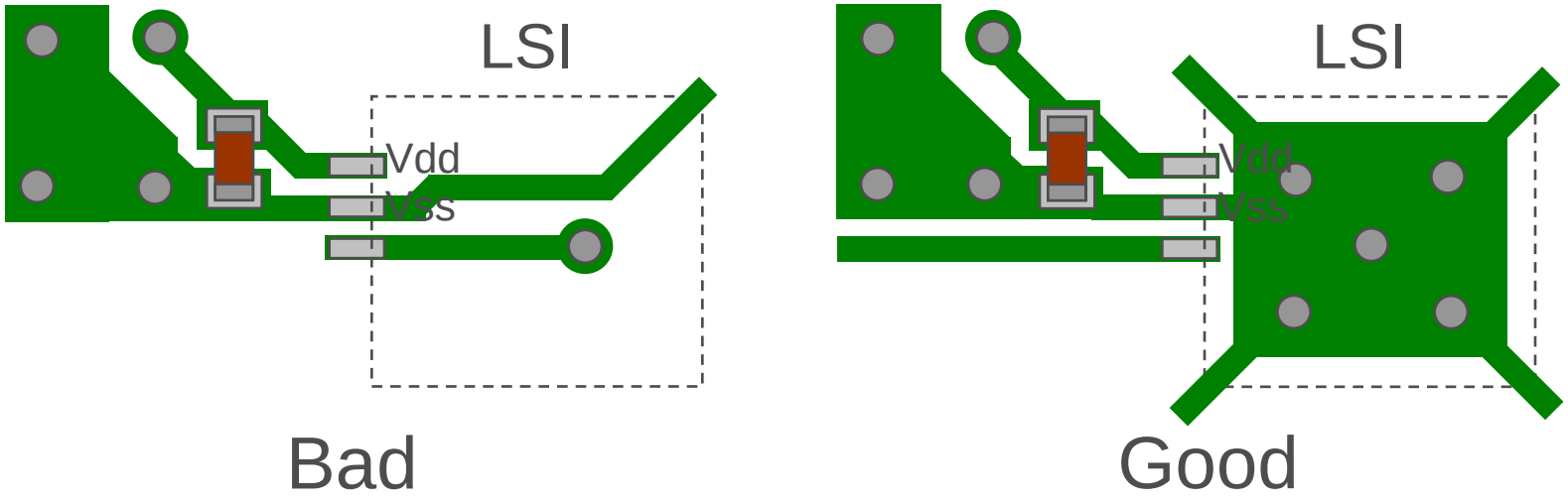


Good

If bypass capacitors with different capacitances are mounted in parallel, the resonance point can be shifted to a higher frequency and the radiative noise at higher frequencies reduced by placing the bypass capacitor with the lowest capacitance closer to the LSI power supply and GND pins. Therefore, in the examples above it is best to arrange the 100pF capacitor closest to the power supply and GND pins.

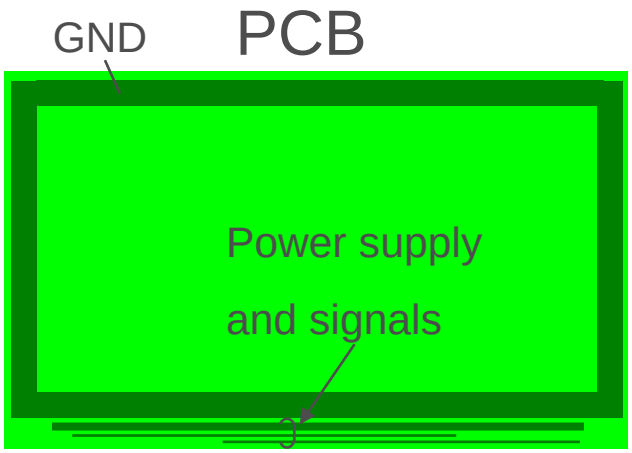
2. GND patterns

2. GND patterns (1)



The area directly under the LSI (on the LSI mounting surface) is the best location for reducing EMI. This needs to be made into solid GND to reduce radiative noise. (Radiative noise can be reduced by stabilizing the GND level.)

2. GND patterns (2)



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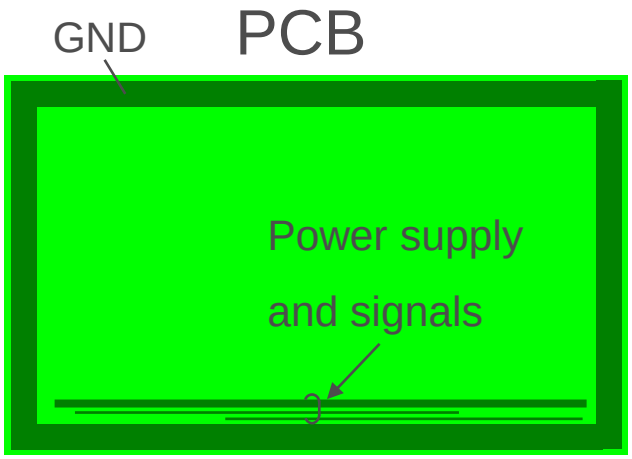
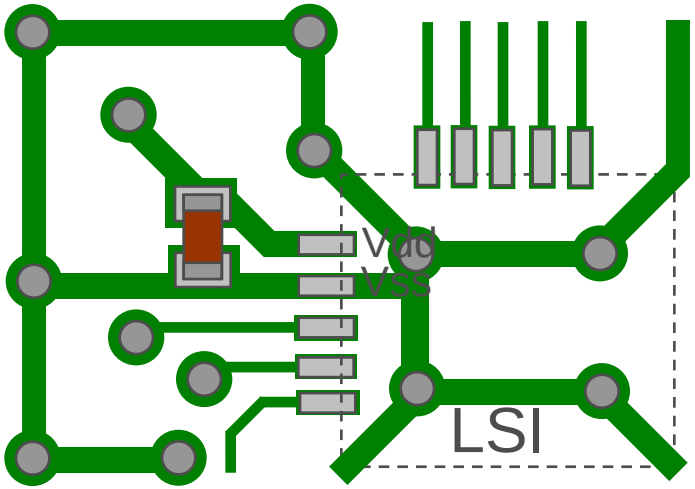


Good

The wiring closest to the perimeter of the PCB has the least coupling with the ground wiring and can easily radiate large amounts of noise. It is best to place GND pattern around the perimeter and not run power supply (Vdd) or signal lines.

2. GND patterns (3)



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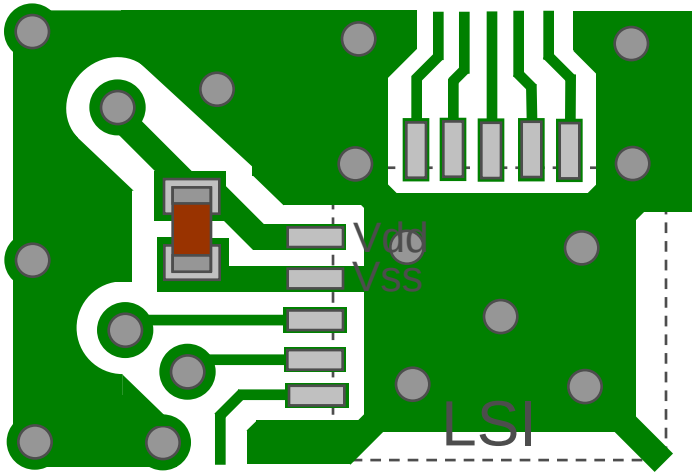
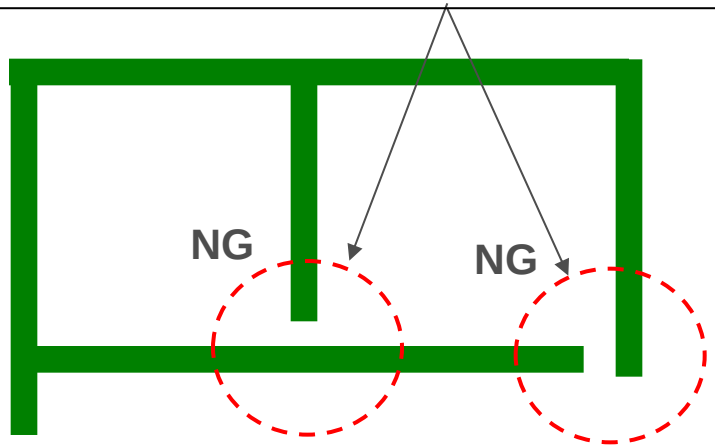


Good

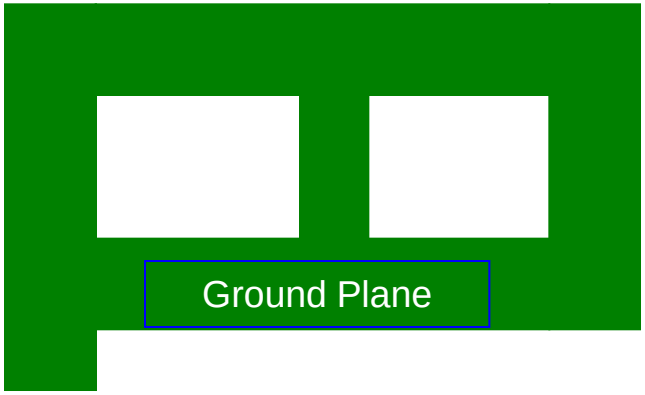
Because the radiative noise can be reduced by increasing the area of the GND pattern on the board, empty areas should be made into GND.
(Radiative noise can be reduced by stabilizing the GND level.)

2. GND patterns (4)

The levels at the ends of wires can be effected by a small amount of noise.



Bad



Good

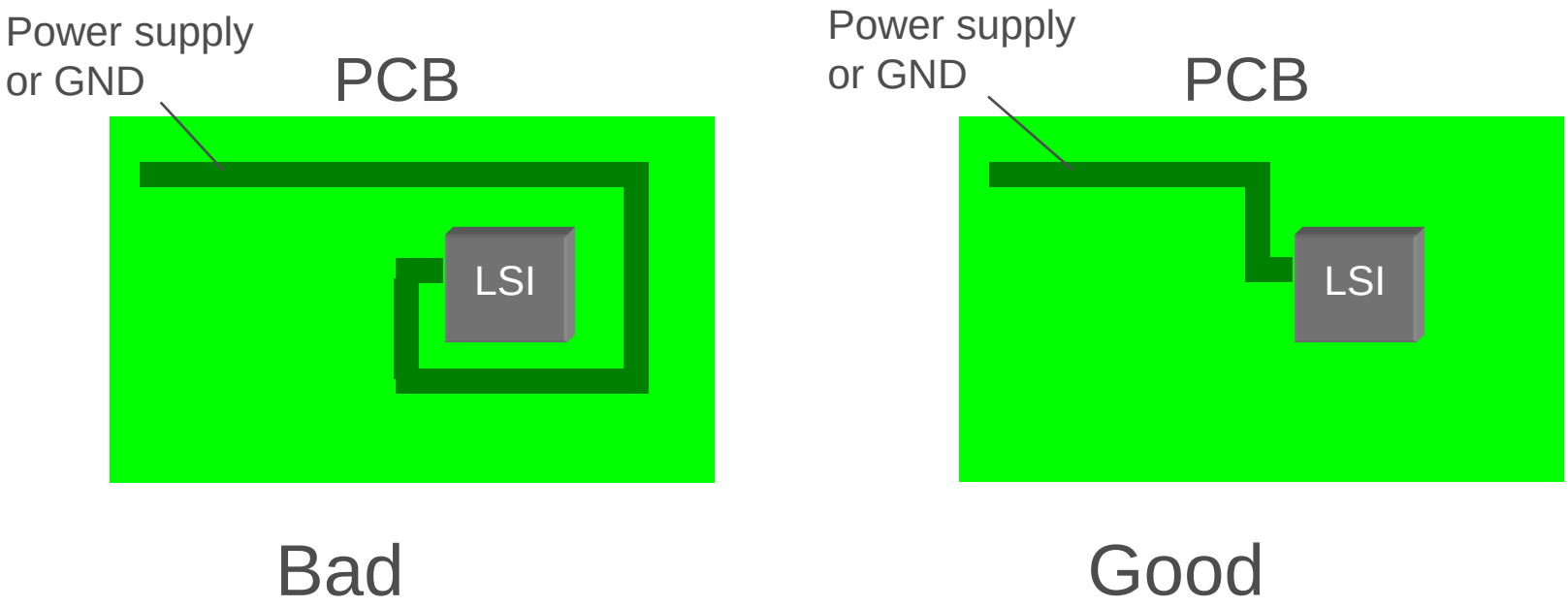
Try as much as possible to avoid creating open loops in the GND pattern of the board.

→ Create broad ground areas using closed loops.

→ Make loops as small as possible.

3. Power supply and GND wiring

3. Power supply and GND wiring (1)

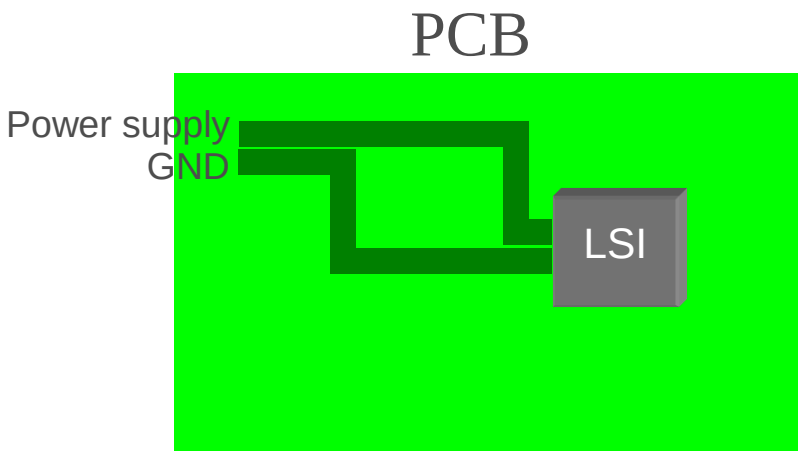


Bad

Good

If a power supply or GND pattern forms a loop shape, the radiated noise will be proportional to the area of the loop. Therefore, avoid making loops in the wiring.

3. Power supply and GND wiring (2)



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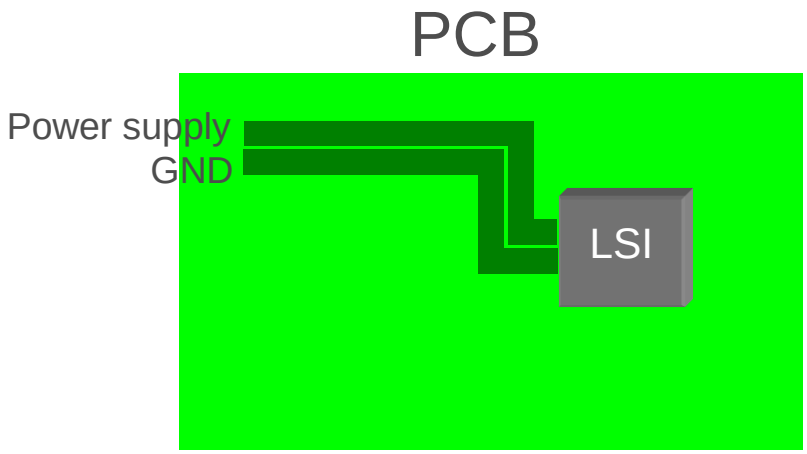


Good

Power supply current loops can be made smaller and radiative noise reduced by running power supply patterns beside and parallel to GND pattern.

3. Power supply and GND wiring (3)

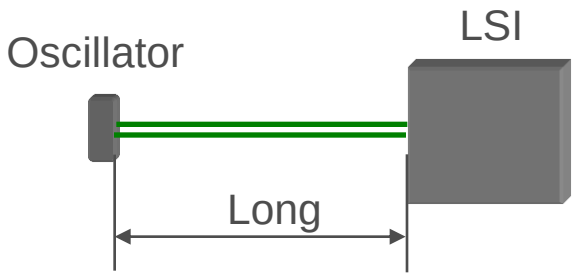
Bad

Good

Radiative noise is strong from sharp, 90-degree corners. It is therefore best if the power supply and GND pattern corners are 45 degrees or curved.
(Applies to both inner and outer layers.)

4. Pattern around oscillators

4. Pattern around oscillators (1)



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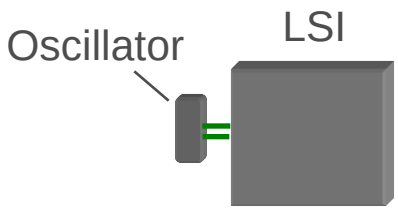
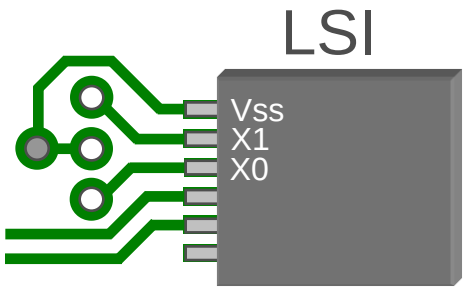


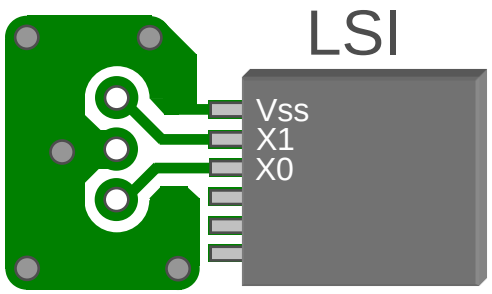
Good

Because high-frequency noise at integral multiples of the oscillator frequency are radiated from oscillator wiring, make the wiring as short as possible.

4. Pattern around oscillators (2)



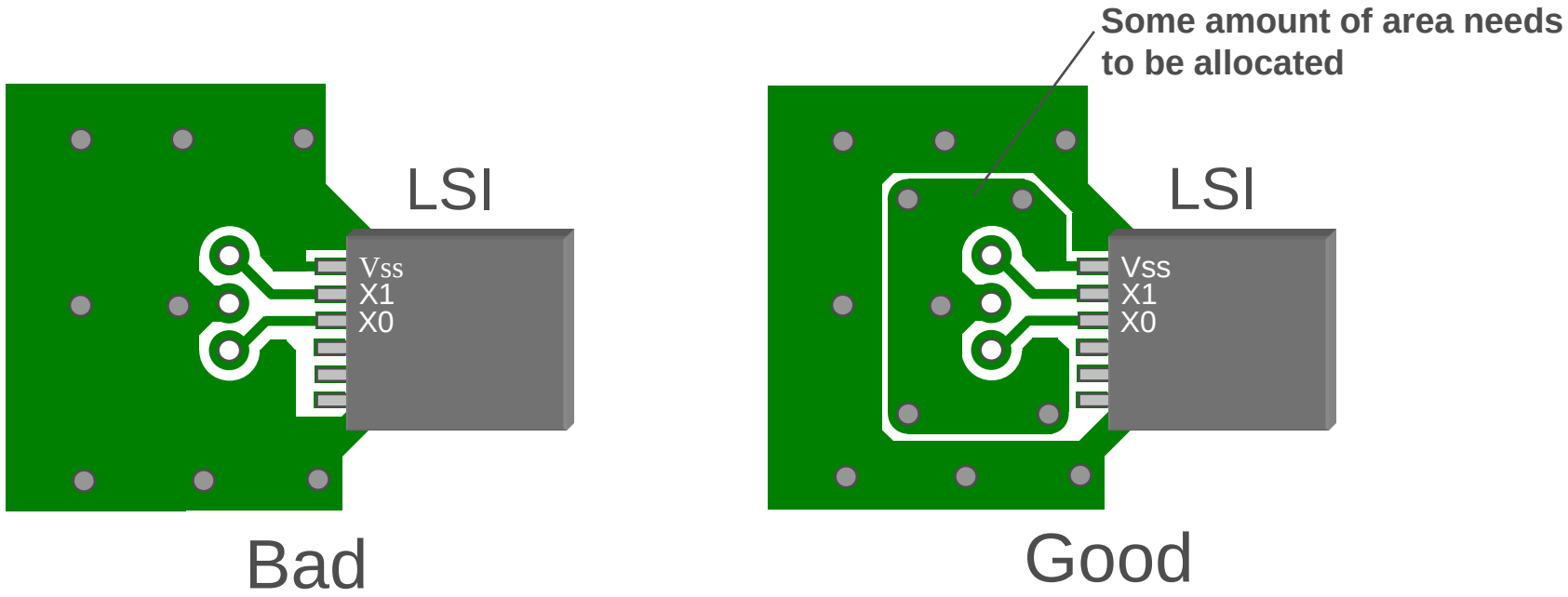
Bad



Good

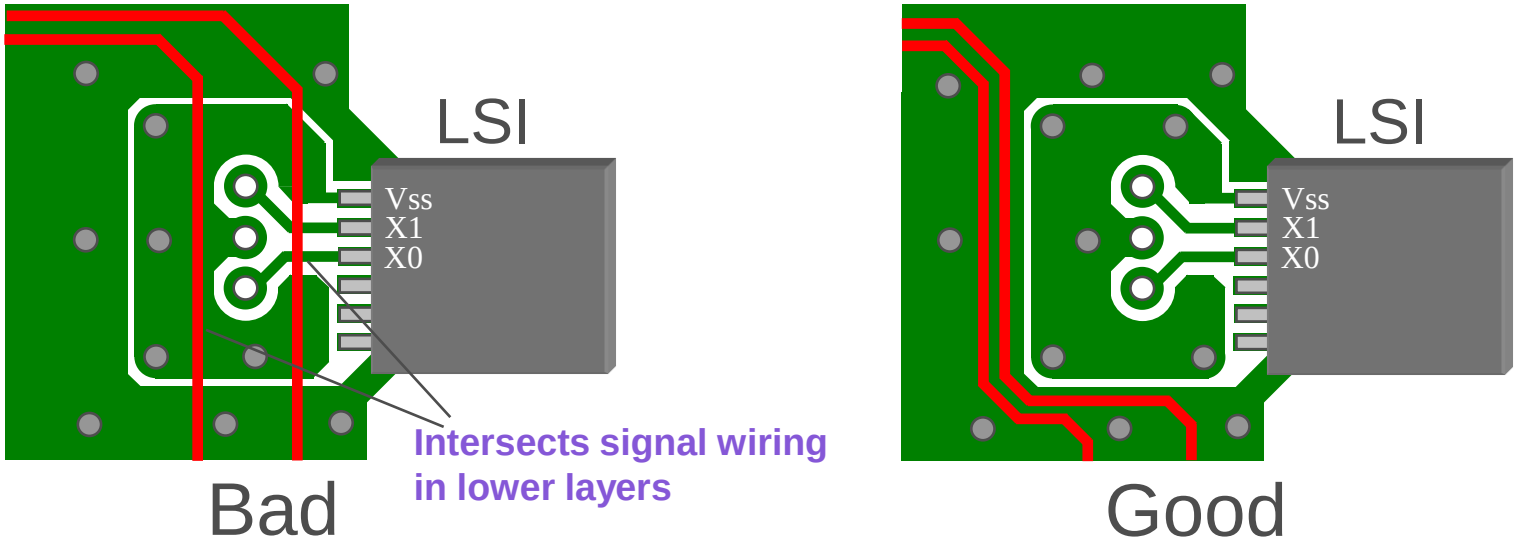
Radiative noise is reduced by surrounding oscillator wiring with GND pattern instead of running the wiring next to other signal wires or power supply (Vdd) lines.

4. Pattern around oscillators (3)



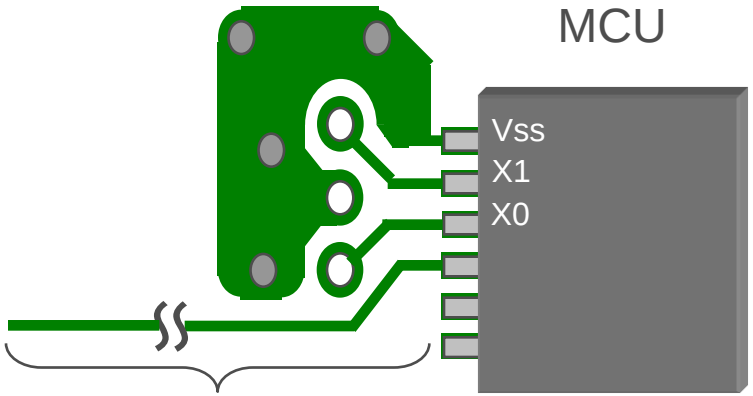
Because there is a lot of noise on GND connected to the load capacitance of the oscillator, fluctuations in the PCB GND can be suppressed and radiative noise reduced by creating a gap separating the PCB GND.
However, some amount of area needs to be allocated to the separated GND.
Caution is required because this gap also needs to be created in other layers so that there are no solid connections with GND planes in other layers through the vias.

4. Pattern around oscillators (4)



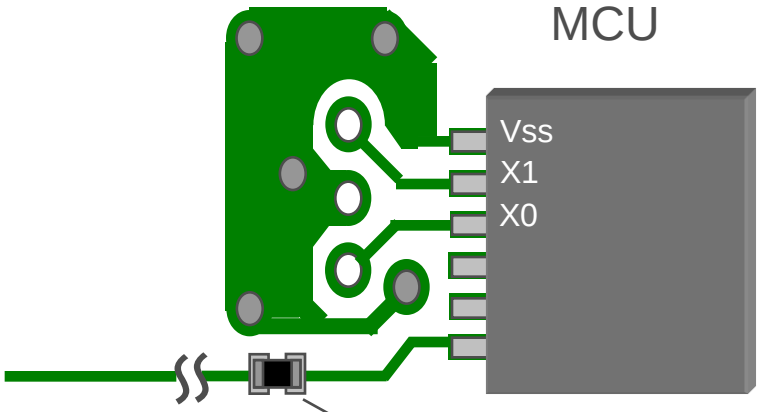
Care is required to ensure that the GND and up and down lines of the oscillator do not cross power supply (Vcc) or signal wiring.
If these lines cross, the oscillator may affect power supply or signal wire, power supply or signal wire may affect the oscillator.

4. Pattern around oscillators (5)



Long wiring
(=antenna)

Bad



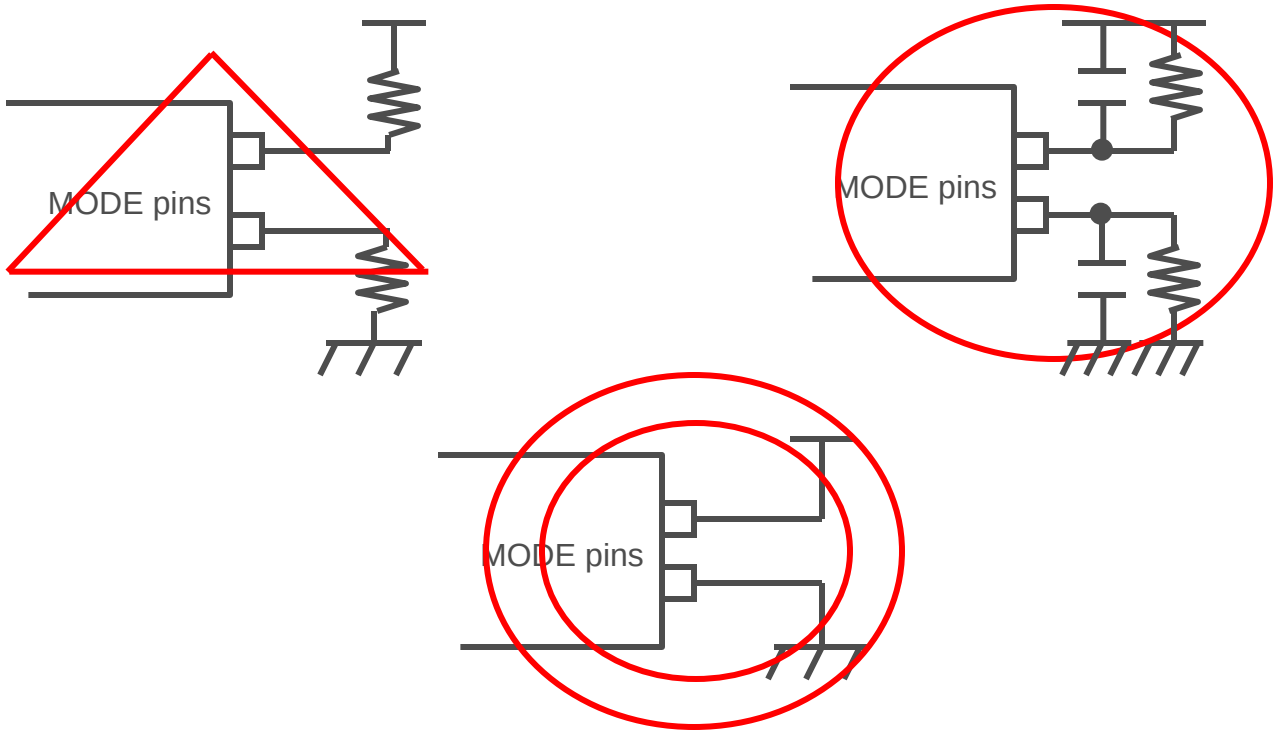
The dumping resistance is necessary when the GND width isn't enough.
(For the limitation on the high frequency electric current.)

Good

The metal case of the crystal oscillator floats electrically, and will form an antenna that radiates noise if used as-is. The case therefore needs to be forced to GND.
(Oscillator products equipped with a pin for connecting the case to GND are also currently available, and may also be used.)

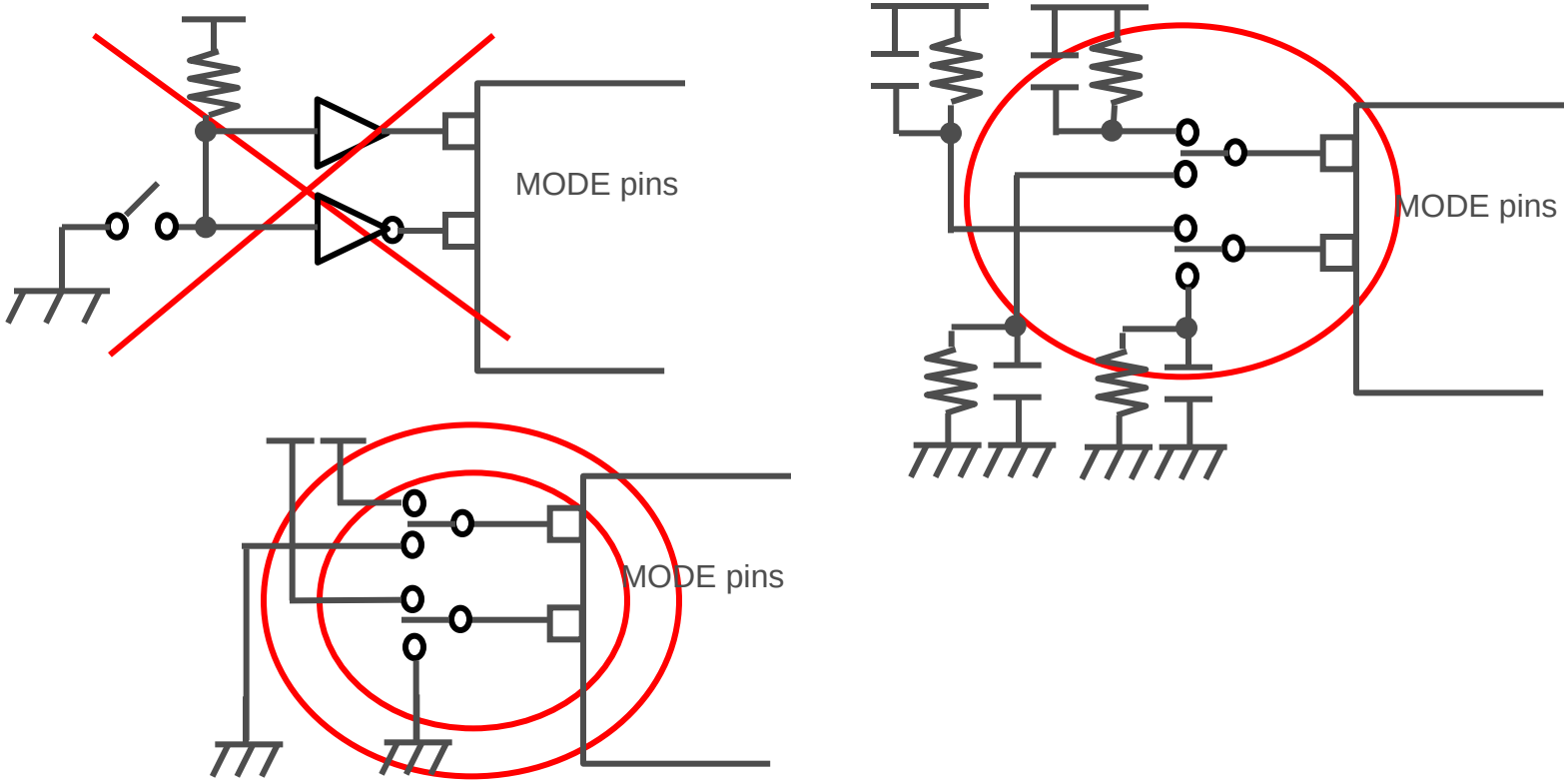
5. Countermeasures of MODE and Reset pins

5. Countermeasures of MODE and Reset pins (MODE part 1)



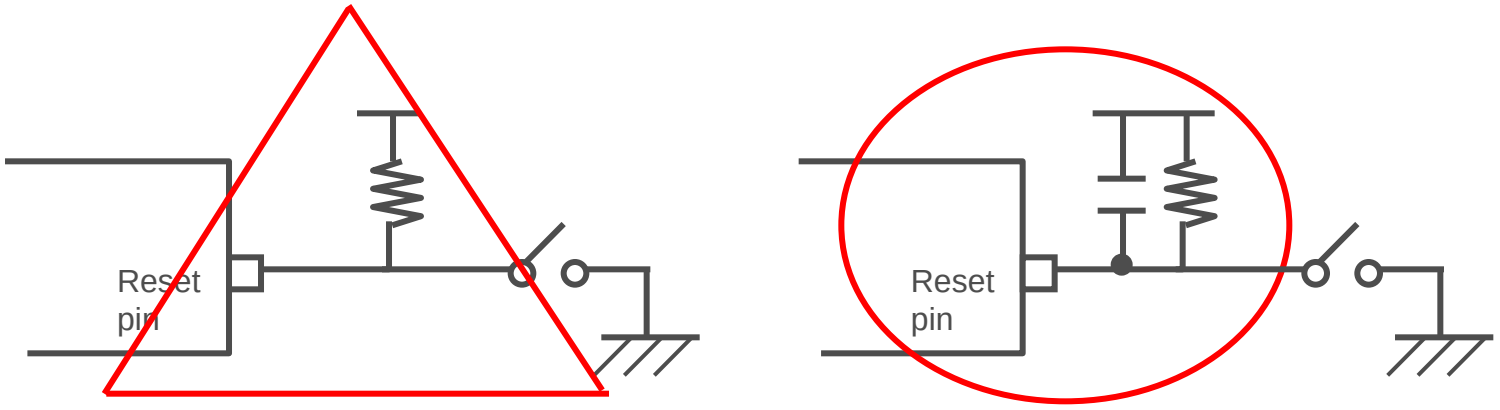
In principle, the MODE pins should be connected directly to the power supply or GND. (Recommended)

5. Countermeasures of MODE and Reset pins (MODE part 2)



When performing on-board reprogramming of FLASH products, the MOD pins should be switched mechanically, not logically.(Recommended)

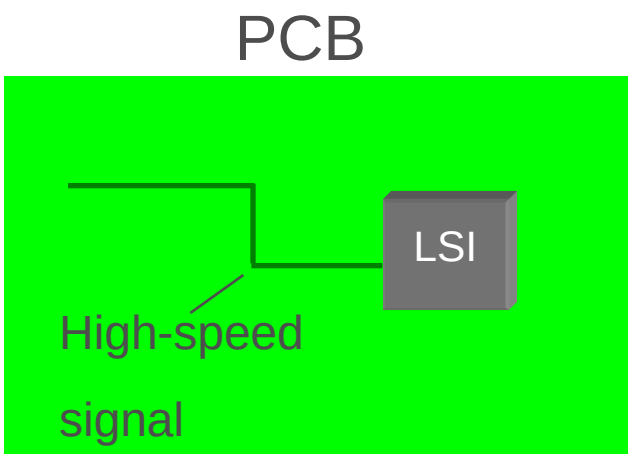
5. Countermeasures of MOD and Reset pins (Reset)



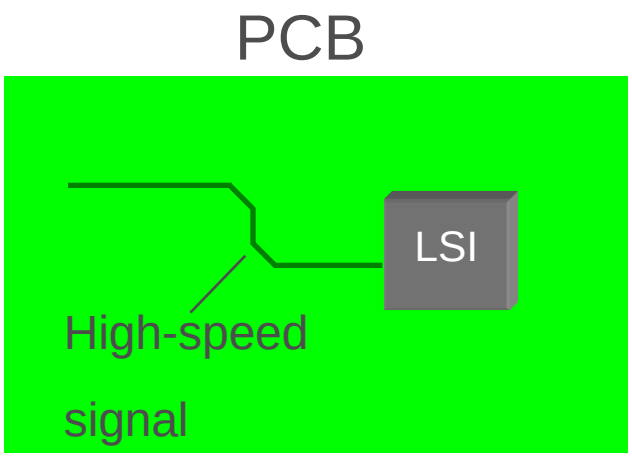
To prevent the reset pin from entering a Hi-z state, it should be pulled up using a resistance of several KΩ (approx. 1KΩ).

6. Signal wiring

6. Signal wiring (1)



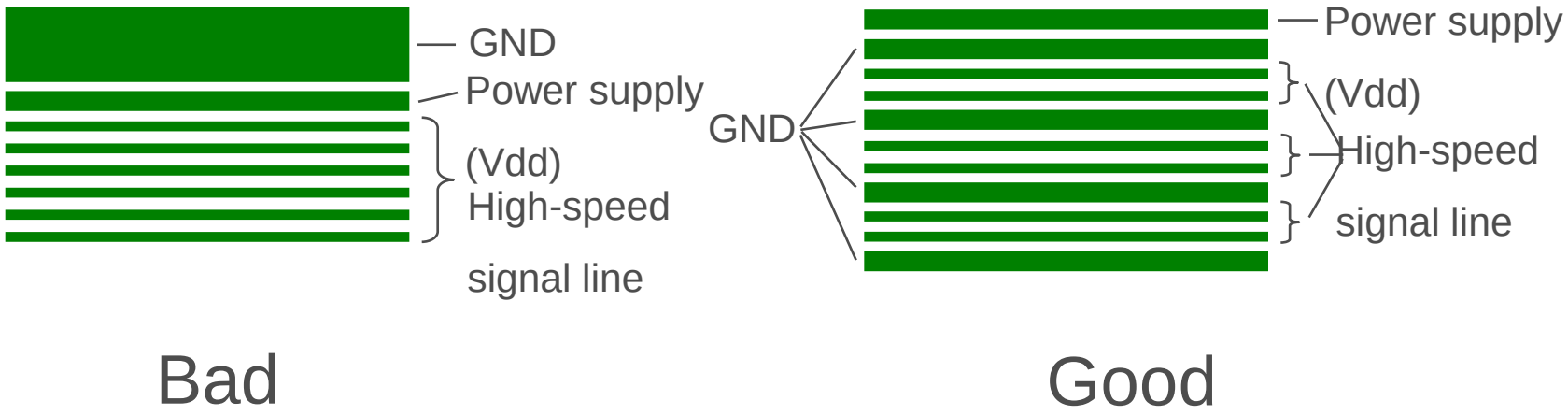
Bad



Good

The wiring of high-speed signals will strongly radiate noise at sharp 90-degree corners, the same as power supply and GND patterns. Therefore, the patterns of high-speed signals should also be curved at 45 degrees.
(Applies to both inner and outer layers.)

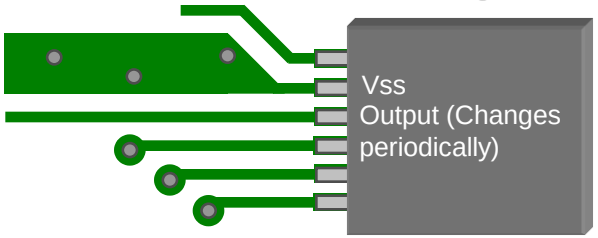
6. Signal wiring (2)



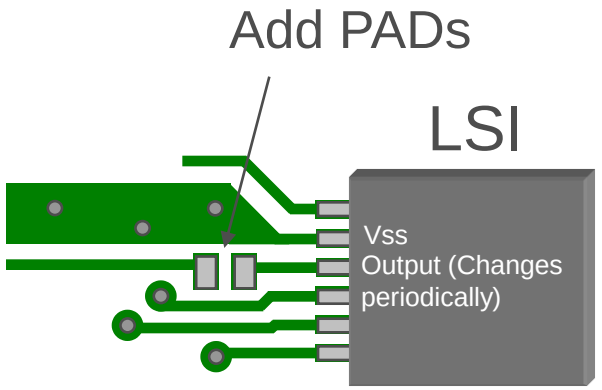
High-speed signal wiring should be run paired with GND wiring in the same way as for power supply (Vdd) wiring. If you cannot fit many lines, GND wires can also be arranged for groups of several signal lines.

<u>High-speed signal lines</u>
These are signal lines on the PCB that change at high frequencies (clocks, buses, etc.) or signals that are low frequency but have steep rising or falling edges.

6. Signal wiring (3)



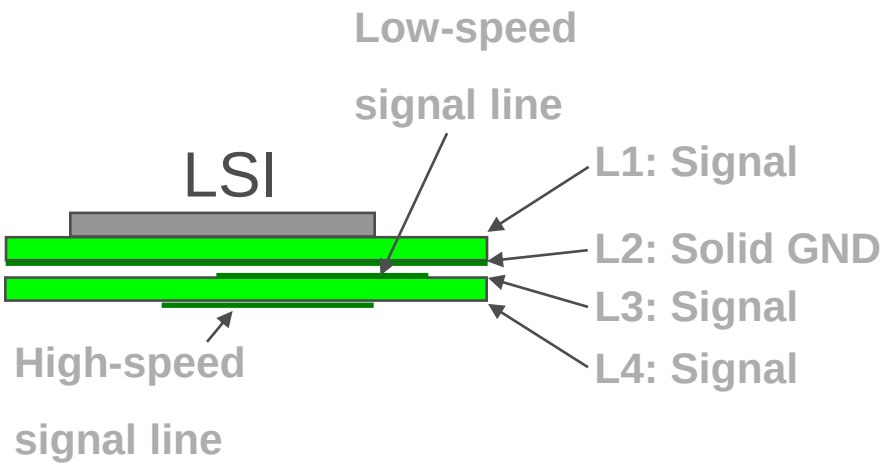
Example requiring attention



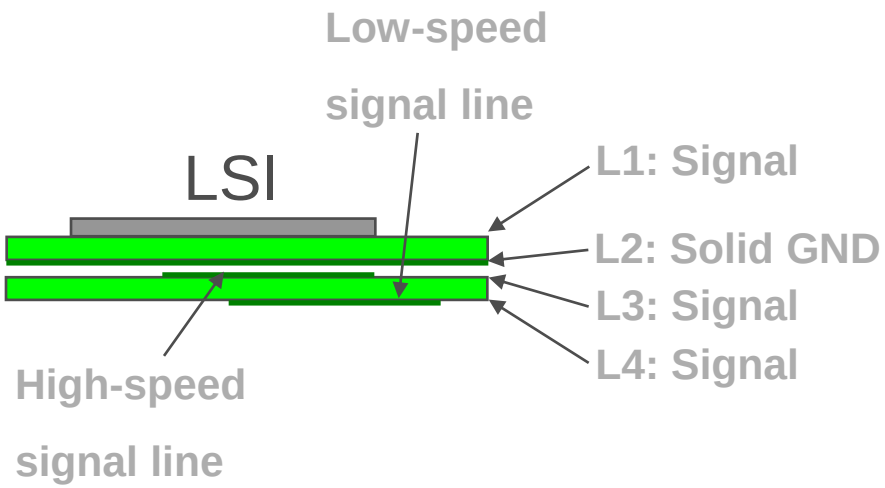
Revised example

If there is some margin in the timing and drive capacity of an output pin that changes periodically, fit pads (lands) in advance so that a damping resistor can be added. When filtering out high frequencies is required, adjust by increasing the value of the damping resistor. (If deemed unnecessary under testing, apply a zero ohm short.) The damping resistor should be placed close to the output pin.

6. Signal wiring (4)



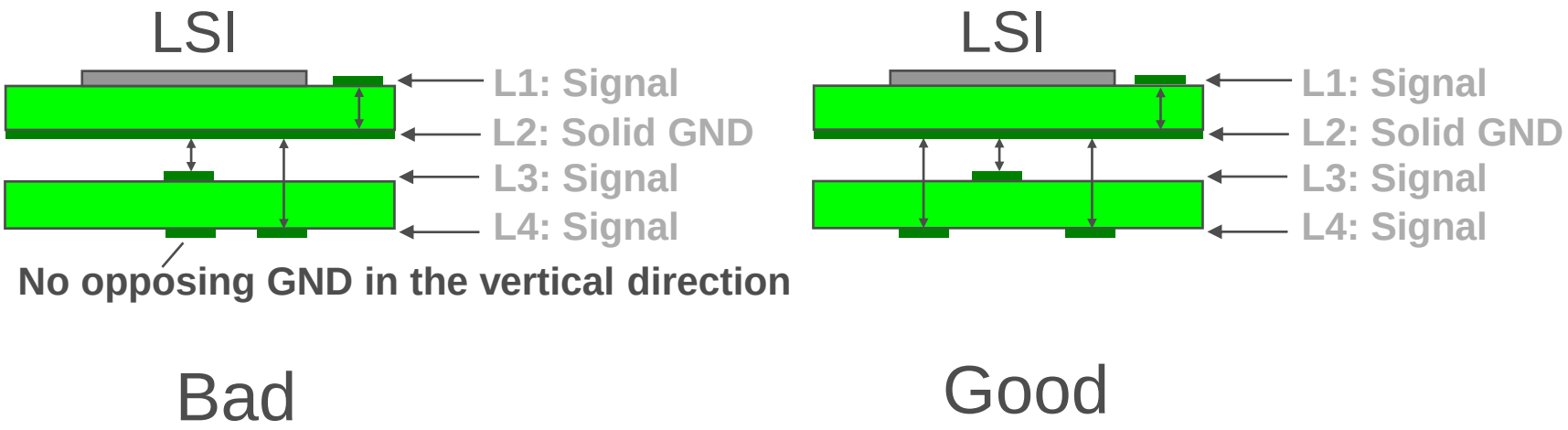
Bad



Good

In the case of multi-layer boards, high-speed signals should be wired on a layer above or below a solid GND layer (L1 or L3 in the above diagram).

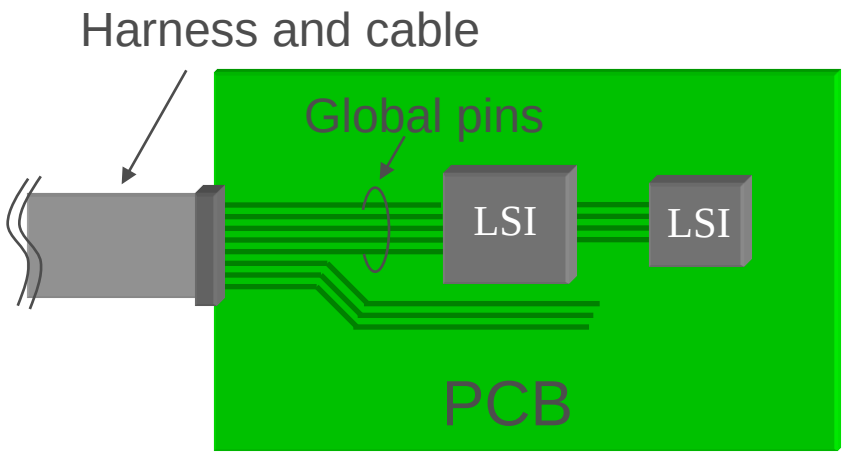
6. Signal wiring (5)



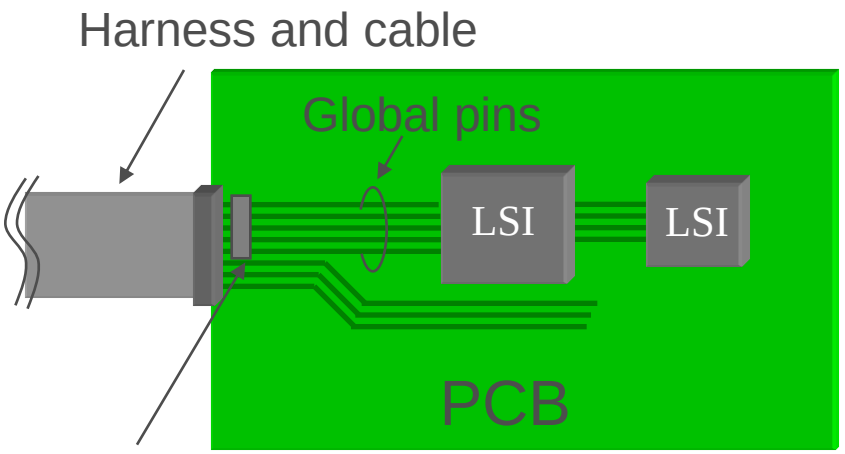
In the case of multi-layer boards, the wiring in the L3 and L4 layers shown in the above diagram should be offset so that they are not stacked vertically. (This is to ensure opposing GND.)

7. Global pins

7. Global pins



Bad



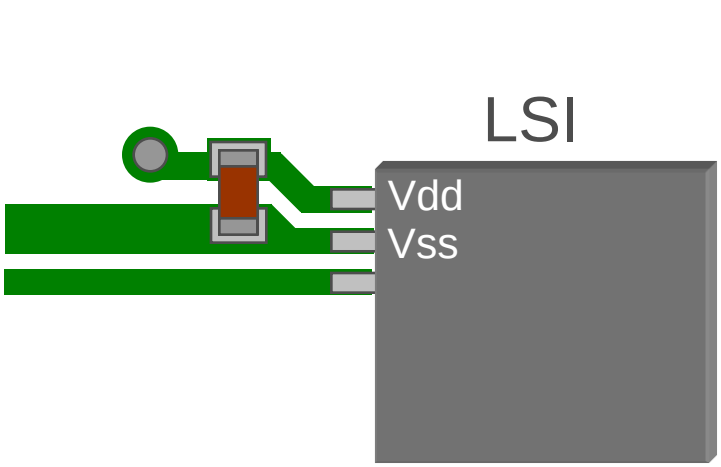
Protective component (Examples: Varistor, Zener, Ferrite, etc.)

Good

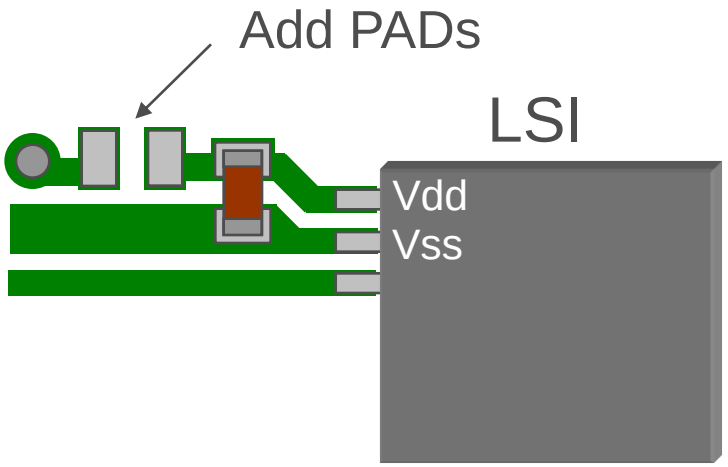
Global pins (LSI pins that are connected directly to a harness and cable), including power supply (Vdd, AVcc, AVRH, AVRL), apply surges and ESD directly to the LSI pins, causing damage to the LSI due to overvoltage, overcurrent, and latch-up, and inducing LSI malfunctions due to applying noise. Protective components suitable for the type of noise therefore need to be inserted.

8. Other

8. Other (1)



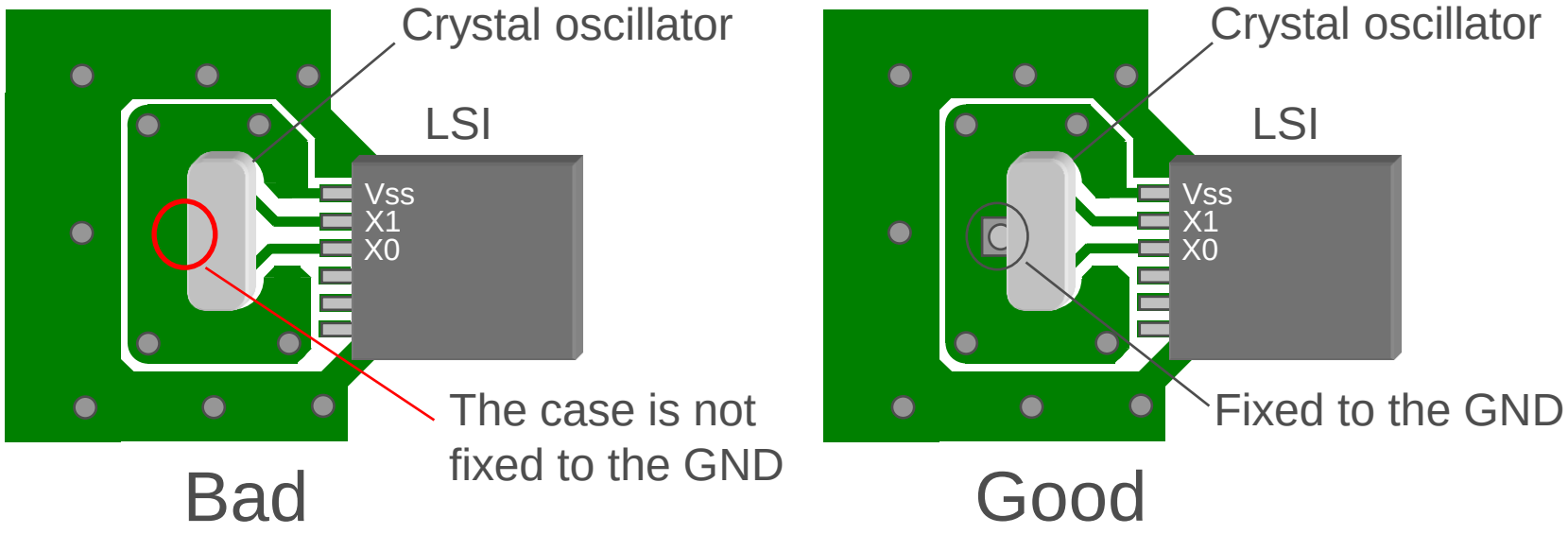
Example requiring attention



Revised example

Radiative noise due to LSI power supply current variations is often a problem. Equip the power supply pins (Vdd) with pads (lands) in advance so that ferrite (beads) can be added. When reducing radiative noise due to power supply current variations is required, adjust using the ferrite value.
(If deemed unnecessary under testing, apply a zero ohm short.)

8. Other (2)



The metal case of the crystal oscillator floats electrically, and will form an antenna that radiates noise if used as-is. The case therefore needs to be forced to GND.
(Pin floating islands (floating wiring and metal cases) to GND.)

8. Other (3)

Bad

Good

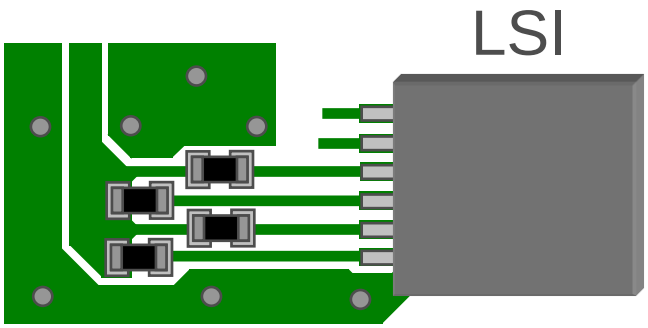
Use smaller components and strengthen the GND.

Reference Component (chip capacitor, chip resistor) mainstream sizes change

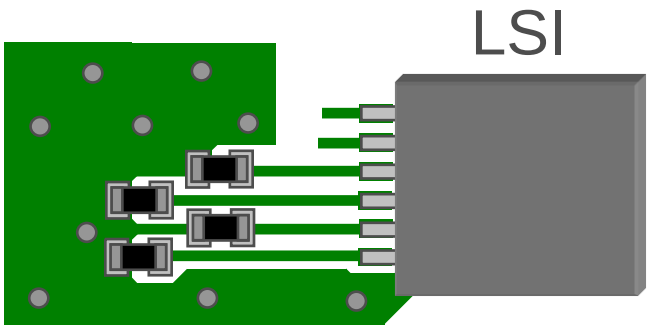
- 1985: 3216 (3.2mm×1.6mm)
- 1990: 2012 (2.0mm×1.2mm)
- 1995: 1005 (1.0mm×0.5mm)
- 2008: 0603 (0.6mm×0.3mm)

. . .

8. Other (4)



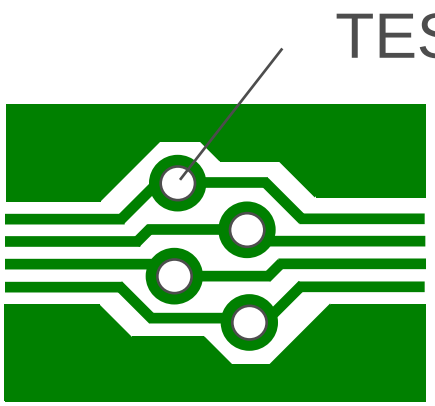
For pull-up



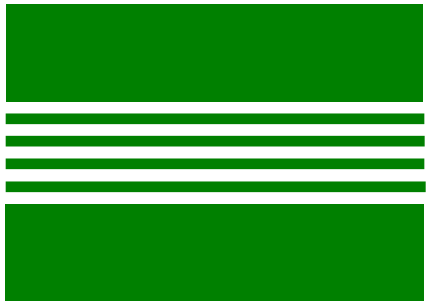
For pull-down

If the fixed level of fixed-input pins can be either H or L, give priority to pull-down over pull-up. This is because pull-up requires power supply (Vdd) wiring for that purpose, and reduces the GND area compared to pull-down.

8. Other (5)



With TEST pads



Without TEST pads

Because the wiring becomes crowded and the GND area is also reduced when TEST pads are fitted, pads should be limited to the bare minimum and avoided where possible.

- End -