



**18-Mbit (512K × 36/1M × 18)  
Flow-Through SRAM**

**Features**

- Supports 133 MHz bus operations
- 512K × 36 and 1M × 18 common I/O
- 3.3 V core power supply (V<sub>DD</sub>)
- 2.5 V or 3.3 V I/O supply (V<sub>DDQ</sub>)
- Fast clock-to-output time
  - 6.5 ns (133 MHz version)
- Provides high performance 2-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Available in JEDEC-standard Pb-free 100-pin TQFP
- ZZ sleep mode option

**Functional Description**

The CY7C1381S/CY7C1383S is a 3.3 V, 512K × 36 and 1M × 18 synchronous flow through SRAMs, designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining chip enable ( $\overline{CE}_1$ ), depth-expansion chip enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ ), burst control inputs ( $\overline{ADSC}$ ,  $\overline{ADSP}$ , and  $\overline{ADV}$ ), write enables ( $\overline{BW}_x$ , and  $\overline{BWE}$ ), and global write ( $\overline{GW}$ ). Asynchronous inputs include the output enable ( $\overline{OE}$ ) and the ZZ pin.

The CY7C1381S/CY7C1383S allows interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe ( $\overline{ADSP}$ ) or the cache controller address strobe ( $\overline{ADSC}$ ) inputs. Address advancement is controlled by the address advancement ( $\overline{ADV}$ ) input.

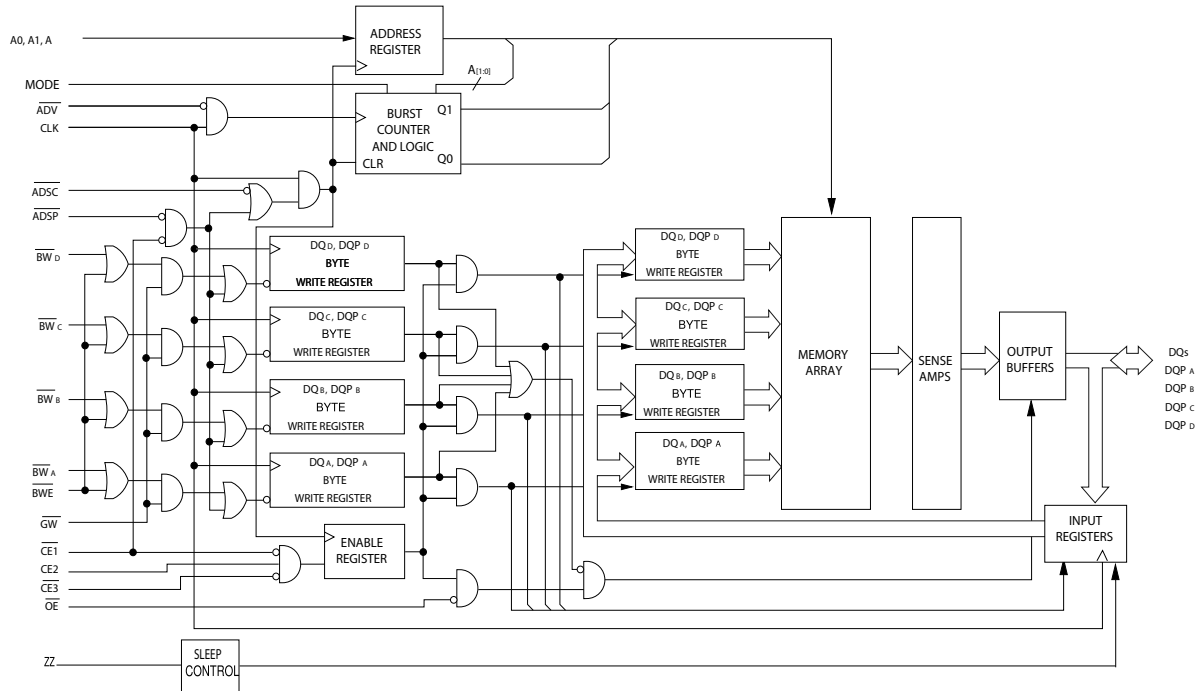
Addresses and chip enables are registered at rising edge of clock when address strobe processor ( $\overline{ADSP}$ ) or address strobe controller ( $\overline{ADSC}$ ) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ( $\overline{ADV}$ ).

The CY7C1381S/CY7C1383S operates from a +3.3 V core power supply while all outputs operate with a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

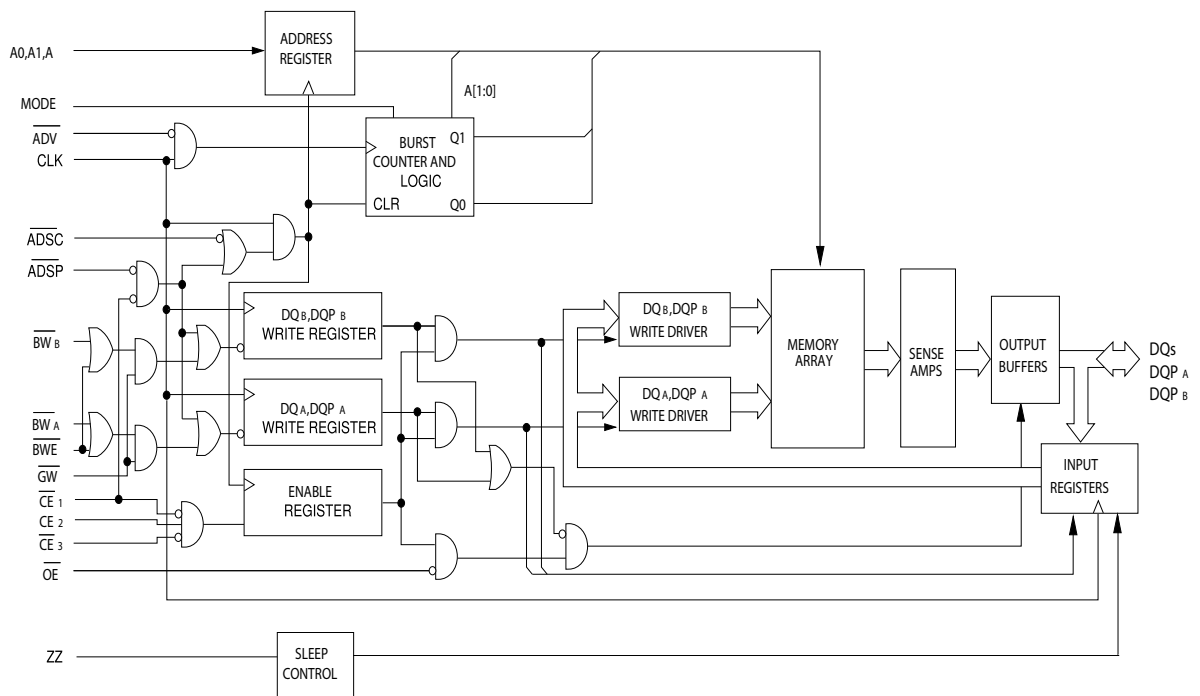
**Selection Guide**

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	210	mA
Maximum CMOS Standby Current	70	mA

**Logic Block Diagram – CY7C1381S**



**Logic Block Diagram – CY7C1383S**

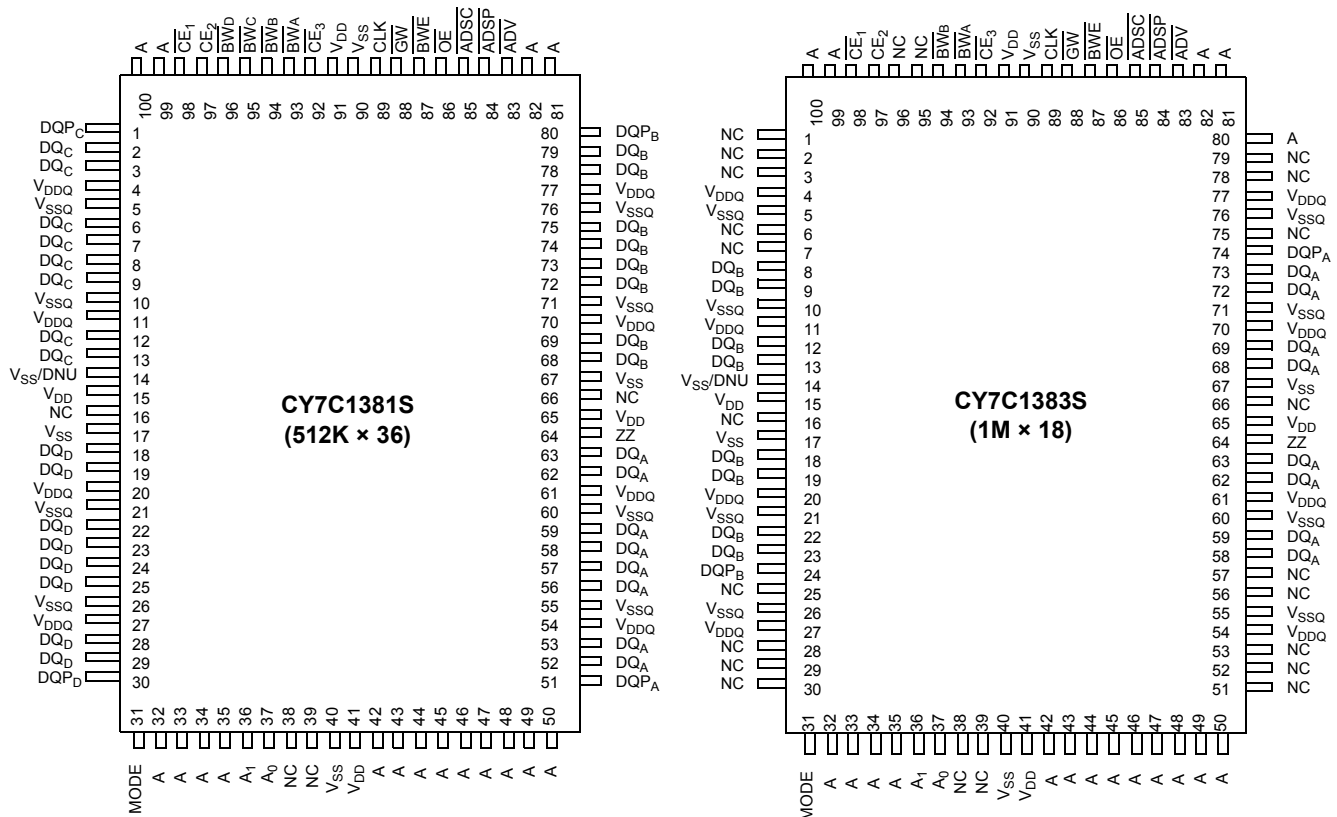


## Contents

<b>Pin Configurations</b> .....	<b>4</b>	<b>Thermal Resistance</b> .....	<b>11</b>
<b>Pin Definitions</b> .....	<b>5</b>	<b>AC Test Loads and Waveforms</b> .....	<b>11</b>
<b>Functional Overview</b> .....	<b>6</b>	<b>Switching Characteristics</b> .....	<b>12</b>
Single Read Accesses .....	6	<b>Timing Diagrams</b> .....	<b>13</b>
Single Write Accesses Initiated by $\overline{\text{ADSP}}$ .....	6	<b>Ordering Information</b> .....	<b>17</b>
Single Write Accesses Initiated by ADSC .....	6	Ordering Code Definitions .....	17
Burst Sequences .....	6	<b>Package Diagrams</b> .....	<b>18</b>
Sleep Mode .....	6	<b>Acronyms</b> .....	<b>19</b>
Interleaved Burst Address Table .....	7	<b>Document Conventions</b> .....	<b>19</b>
Linear Burst Address Table .....	7	Units of Measure .....	19
ZZ Mode Electrical Characteristics .....	7	<b>Document History Page</b> .....	<b>20</b>
<b>Truth Table</b> .....	<b>8</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>22</b>
<b>Truth Table for Read/Write</b> .....	<b>9</b>	Worldwide Sales and Design Support .....	22
<b>Truth Table for Read/Write</b> .....	<b>9</b>	Products .....	22
<b>Maximum Ratings</b> .....	<b>10</b>	PSoC® Solutions .....	22
<b>Operating Range</b> .....	<b>10</b>	Cypress Developer Community .....	22
<b>Electrical Characteristics</b> .....	<b>10</b>	Technical Support .....	22
<b>Capacitance</b> .....	<b>11</b>		

**Pin Configurations**

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enable)**



## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address Inputs Used to Select One of the Address Locations.</b> Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$ , $CE_2$ , and $\overline{CE}_3$ are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
$\overline{BW}_A$ , $\overline{BW}_B$ , $\overline{BW}_C$ , $\overline{BW}_D$	Input-Synchronous	<b>Byte Write Select Inputs, Active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input-Synchronous	<b>Global Write Enable Input, Active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$ ).
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	<b>Chip Enable 1 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
$CE_2$	Input-Synchronous	<b>Chip Enable 2 Input, Active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. $CE_2$ is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	<b>Chip Enable 3 Input, Active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	<b>Output Enable, Asynchronous Input, Active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	<b>Advance Input Signal.</b> Sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	<b>Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ADSP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-Synchronous	<b>Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
$\overline{BWE}$	Input-Synchronous	<b>Byte Write Enable Input, Active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input-Asynchronous	<b>ZZ Sleep Input.</b> This active HIGH input places the device in a non-time critical sleep condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ <sub>s</sub>	I/O-Synchronous	<b>Bidirectional Data I/O Lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>x</sub> are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$ .
DQP <sub>x</sub>	I/O-Synchronous	<b>Bidirectional Data Parity I/O Lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> . During write sequences, DQP <sub>x</sub> is controlled by $\overline{BW}_x$ correspondingly.
MODE	Input-Static	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.
V <sub>DD</sub>	Power Supply	<b>Power Supply Inputs to the Core of the Device.</b>

## Pin Definitions (continued)

Name	I/O	Description
V <sub>DDQ</sub>	I/O Power Supply	<b>Power Supply for the I/O Circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the Core of the Device.</b>
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O Circuitry.</b>
NC	–	<b>No Connects.</b> Not internally connected to the die. 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V <sub>SS</sub> /DNU	Ground/DNU	This pin can be connected to ground or can be left floating.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133 MHz device).

The CY7C1381S/CY7C1383S supports secondary cache in systems utilizing a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ( $\overline{BW_E}$ ) and byte write select ( $\overline{BW_X}$ ) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ( $\overline{CE_1}$ ,  $\overline{CE_2}$ ,  $\overline{CE_3}$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tri-state control. ADSP is ignored if  $\overline{CE_1}$  is HIGH.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ , and  $\overline{CE_3}$  are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter and/or control logic, and later presented to the memory core. If the OE input is asserted LOW, the requested data is available at the data outputs with a maximum to  $t_{CDV}$  after clock rise. ADSP is ignored if  $\overline{CE_1}$  is HIGH.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ ,  $\overline{CE_3}$  are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ( $\overline{GW}$ ,  $\overline{BW_E}$ , and  $\overline{BW_X}$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see Truth Table for Read/Write on page 9 for appropriate states that indicate a write) on the next

clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. All IOs are tri-stated during a byte write. As this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the IOs must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE_1}$ ,  $\overline{CE_2}$ , and  $\overline{CE_3}$  are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW_X}$ ) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter, the control logic, or both, and delivered to the memory core. The information presented to  $DQ_{[A:D]}$  is written into the specified address location. Byte writes are allowed. All IOs are tri-stated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the IOs must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C1381S/CY7C1383S provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by  $A_{[1:0]}$ , and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode.  $\overline{CE_1}$ ,  $\overline{CE_2}$ ,  $\overline{CE_3}$ , ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**Interleaved Burst Address Table**

 (MODE = Floating or  $V_{DD}$ )

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Address Table**

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	80	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The truth table for CY7C1381S/CY7C1383S follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-State
Deselected Cycle, Power Down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

1. X = Don't Care, H = Logic HIGH, L = Logic LOW.
2.  $\overline{WRITE}$  = L when any one or more byte write enable signals, and  $\overline{BWE}$  = L or  $\overline{GW}$  = L.  $\overline{WRITE}$  = H when all byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW}$  = H.
3. The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
5.  $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).



### Truth Table for Read/Write

The read/write truth table for CY7C1381S follows. [6, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ <sub>A</sub> , DQP <sub>A</sub> )	H	L	H	H	H	L
Write Byte B (DQ <sub>B</sub> , DQP <sub>B</sub> )	H	L	H	H	L	H
Write Bytes A, B (DQ <sub>A</sub> , DQ <sub>B</sub> , DQP <sub>A</sub> , DQP <sub>B</sub> )	H	L	H	H	L	L
Write Byte C (DQ <sub>C</sub> , DQP <sub>C</sub> )	H	L	H	L	H	H
Write Bytes C, A (DQ <sub>C</sub> , DQ <sub>A</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	H	L	H	L
Write Bytes C, B (DQ <sub>C</sub> , DQ <sub>B</sub> , DQP <sub>C</sub> , DQP <sub>B</sub> )	H	L	H	L	L	H
Write Bytes C, B, A (DQ <sub>C</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>C</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	H	L	L	L
Write Byte D (DQ <sub>D</sub> , DQP <sub>D</sub> )	H	L	L	H	H	H
Write Bytes D, A (DQ <sub>D</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>A</sub> )	H	L	L	H	H	L
Write Bytes D, B (DQ <sub>D</sub> , DQ <sub>B</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	H	L	H
Write Bytes D, B, A (DQ <sub>D</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	H	L	L
Write Bytes D, B (DQ <sub>D</sub> , DQ <sub>B</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> )	H	L	L	L	H	H
Write Bytes D, B, A (DQ <sub>D</sub> , DQ <sub>C</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>C</sub> , DQP <sub>A</sub> )	H	L	L	L	H	L

### Truth Table for Read/Write

The read/write truth table for CY7C1383S follows. [6, 7]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Write Bytes D, C, A (DQ <sub>D</sub> , DQ <sub>B</sub> , DQ <sub>A</sub> , DQP <sub>D</sub> , DQP <sub>B</sub> , DQP <sub>A</sub> )	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	L
Write Byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	L	H
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

**Notes**

6. X = Don't Care, H = Logic HIGH, L = Logic LOW.

7. Table only lists a partial listing of the byte write combinations. Any combination of  $\overline{BW}_x$  is valid. Appropriate write is done based on which byte write is active.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. For user guidelines, not tested.

Storage Temperature ..... -65 °C to +150 °C  
 Ambient Temperature with Power Applied ..... -55 °C to +125 °C  
 Supply Voltage on V<sub>DD</sub> Relative to GND ..... -0.3 V to +4.6 V  
 Supply Voltage on V<sub>DDQ</sub> Relative to GND ..... -0.3 V to +V<sub>DD</sub>  
 DC Voltage Applied to Outputs in Tri-State ..... -0.5 V to V<sub>DDQ</sub> + 0.5 V

DC Input Voltage ..... -0.5 V to V<sub>DD</sub> + 0.5 V  
 Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V  
 Latch up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>

## Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power Supply Voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage	for 3.3 V I/O	3.135	V <sub>DD</sub>	V
		for 2.5 V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH Voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	-	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	-	V
V <sub>OL</sub>	Output LOW Voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	-	0.4	V
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage [8]	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW Voltage [8]	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input Current of MODE	Input = V <sub>SS</sub>	-30	-	μA
		Input = V <sub>DD</sub>	-	5	μA
	Input Current of ZZ	Input = V <sub>SS</sub>	-5	-	μA
Input = V <sub>DD</sub>		-	30	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub> , Output Disabled	-5	5	μA
I <sub>DD</sub> [10]	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	-	210	mA
I <sub>SB1</sub>	Automatic CE Power Down Current – TTL Inputs	Max V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	-	140	mA
I <sub>SB2</sub>	Automatic CE Power Down Current – CMOS Inputs	Max V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, inputs static	-	70	mA
I <sub>SB3</sub>	Automatic CE Power Down Current – CMOS Inputs	Max V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = f <sub>MAX</sub> , inputs switching	-	130	mA

### Notes

8. Overshoot: V<sub>IH(AC)</sub> < V<sub>DD</sub> + 1.5 V (pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL(AC)</sub> > -2 V (pulse width less than t<sub>CYC</sub>/2).
9. T<sub>power up</sub>: Assumes a linear ramp from 0 V to V<sub>DD(min)</sub> within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.
10. The operation current is calculated with 50% read cycle and 50% write cycle.

## Electrical Characteristics (continued)

Over the Operating Range

Parameter <sup>[8, 9]</sup>	Description	Test Conditions	Min	Max	Unit
$I_{SB4}$	Automatic CE Power Down Current – TTL Inputs	Max $V_{DD}$ , Device Deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$ , inputs static	–	80	mA

## Capacitance

Parameter <sup>[11]</sup>	Description	Test Conditions	100-pin TQFP Package	Unit
$C_{IN}$	Input capacitance	$T_A = 25$ °C, $f = 1$ MHz, $V_{DD} = 3.3$ V, $V_{DDQ} = 2.5$ V	5	pF
$C_{CLK}$	Clock input capacitance		5	pF
$C_{IO}$	Input/Output capacitance		5	pF

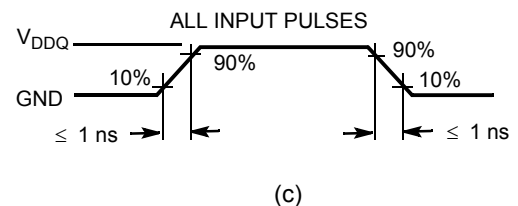
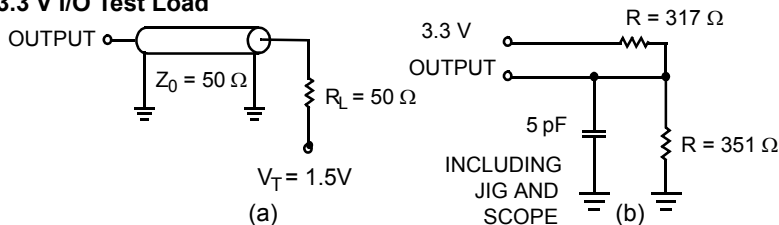
## Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	100-pin TQFP Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	°C/W
$\Theta_{JC}$	Thermal resistance (junction to case)		4.08	°C/W

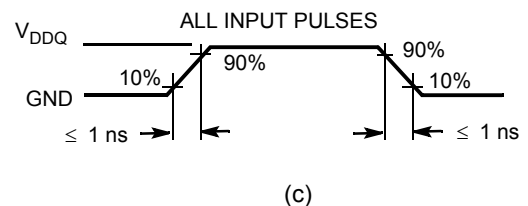
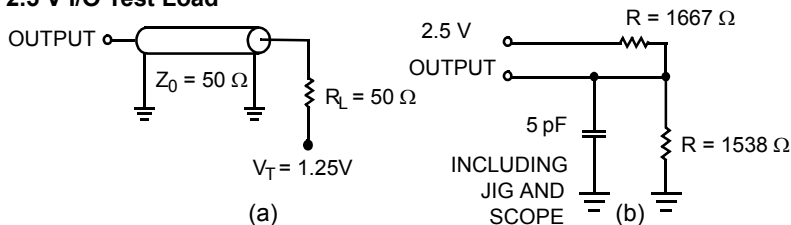
## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

### 3.3 V I/O Test Load



### 2.5 V I/O Test Load



**Note**

11. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

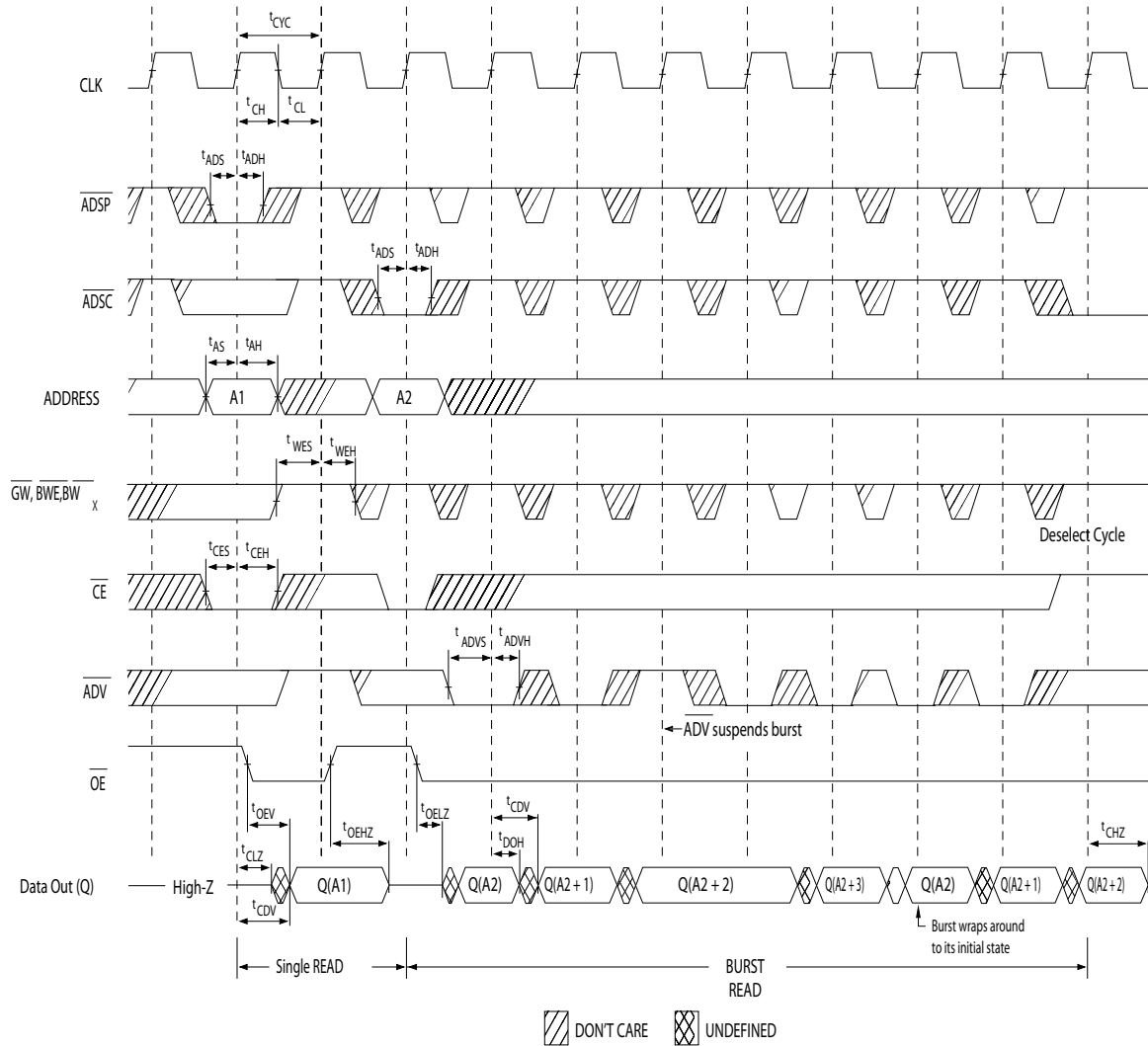
Parameter <sup>[12, 13]</sup>	Description	133 MHz		Unit
		Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (Typical) to the first Access <sup>[14]</sup>	1	–	ms
<b>Clock</b>				
t <sub>CYC</sub>	Clock Cycle Time	7.5	–	ns
t <sub>CH</sub>	Clock HIGH	2.1	–	ns
t <sub>CL</sub>	Clock LOW	2.1	–	ns
<b>Output Times</b>				
t <sub>CDV</sub>	Data Output Valid After CLK Rise	–	6.5	ns
t <sub>DOH</sub>	Data Output Hold After CLK Rise	2.0	–	ns
t <sub>CLZ</sub>	Clock to Low Z <sup>[15, 16, 17]</sup>	2.0	–	ns
t <sub>CHZ</sub>	Clock to High Z <sup>[15, 16, 17]</sup>	0	4.0	ns
t <sub>OEV</sub>	$\overline{\text{OE}}$ LOW to Output Valid	–	3.2	ns
t <sub>OELZ</sub>	$\overline{\text{OE}}$ LOW to Output Low Z <sup>[15, 16, 17]</sup>	0	–	ns
t <sub>OEHZ</sub>	$\overline{\text{OE}}$ HIGH to Output High Z <sup>[15, 16, 17]</sup>	–	4.0	ns
<b>Setup Times</b>				
t <sub>AS</sub>	Address Setup Before CLK Rise	1.5	–	ns
t <sub>ADS</sub>	ADSP, ADSC Setup Before CLK Rise	1.5	–	ns
t <sub>ADVS</sub>	$\overline{\text{ADV}}$ Setup Before CLK Rise	1.5	–	ns
t <sub>WES</sub>	$\overline{\text{GW}}$ , $\overline{\text{BWE}}$ , $\overline{\text{BW}}_{[\text{A:D}]}$ Setup Before CLK Rise	1.5	–	ns
t <sub>DS</sub>	Data Input Setup Before CLK Rise	1.5	–	ns
t <sub>CES</sub>	Chip Enable Setup	1.5	–	ns
<b>Hold Times</b>				
t <sub>AH</sub>	Address Hold After CLK Rise	0.5	–	ns
t <sub>ADH</sub>	ADSP, ADSC Hold After CLK Rise	0.5	–	ns
t <sub>WEH</sub>	$\overline{\text{GW}}$ , $\overline{\text{BWE}}$ , $\overline{\text{BW}}_{[\text{A:D}]}$ Hold After CLK Rise	0.5	–	ns
t <sub>ADVH</sub>	$\overline{\text{ADV}}$ Hold After CLK Rise	0.5	–	ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.5	–	ns
t <sub>CEH</sub>	Chip Enable Hold After CLK Rise	0.5	–	ns

### Notes

12. Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.
13. Test conditions shown in (a) of [Figure 2 on page 11](#) unless otherwise noted.
14. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power is supplied above V<sub>DD(minimum)</sub> initially, before a read or write operation can be initiated.
15. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC test conditions shown in part (b) of [Figure 2 on page 11](#). Transition is measured ± 200 mV from steady-state voltage.
16. At any voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system condition.
17. This parameter is sampled and not 100% tested.

## Timing Diagrams

Figure 3. Read Cycle Timing [18]

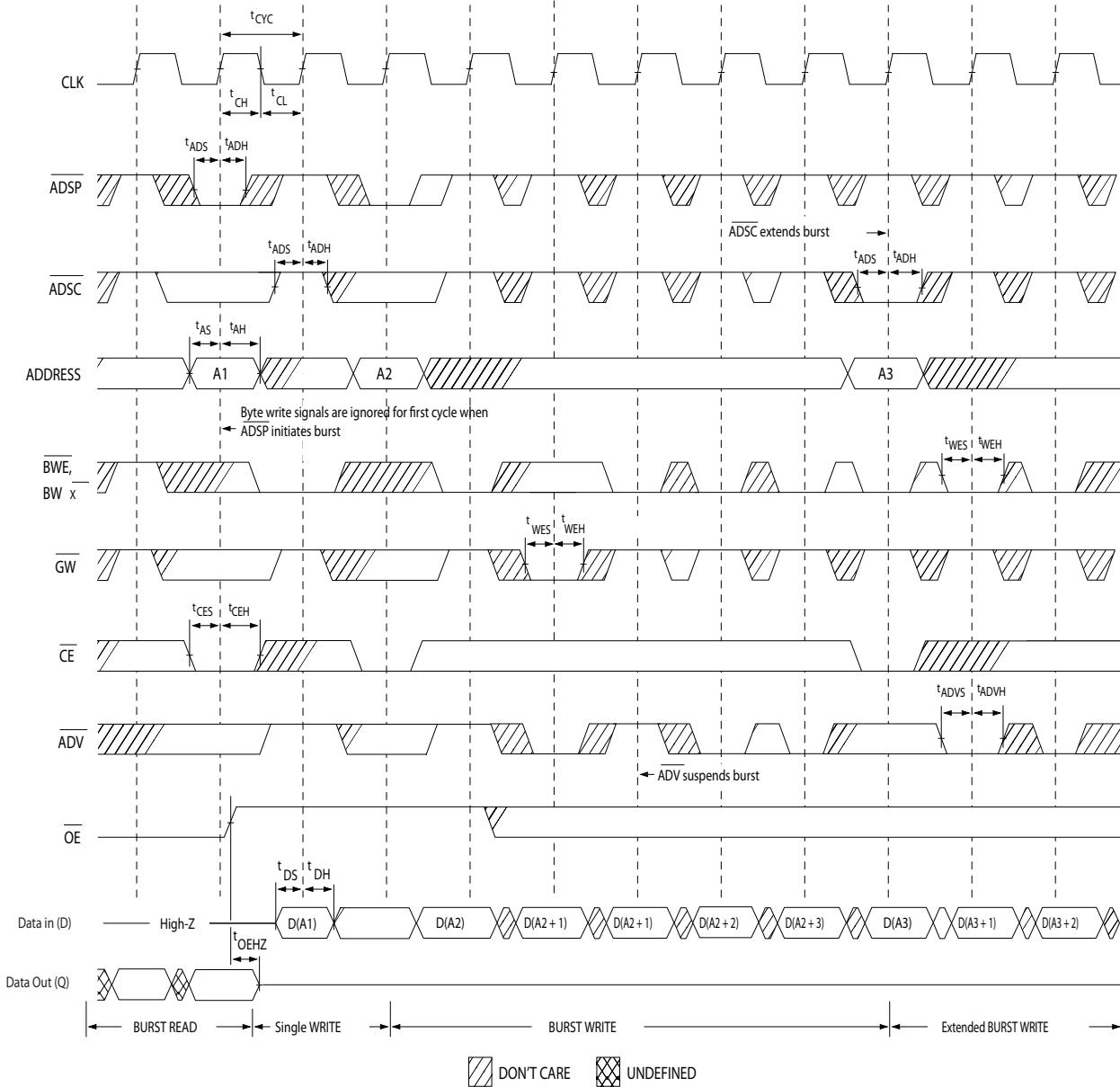


**Note**

18. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

**Timing Diagrams** (continued)

**Figure 4. Write Cycle Timing** [19, 20]

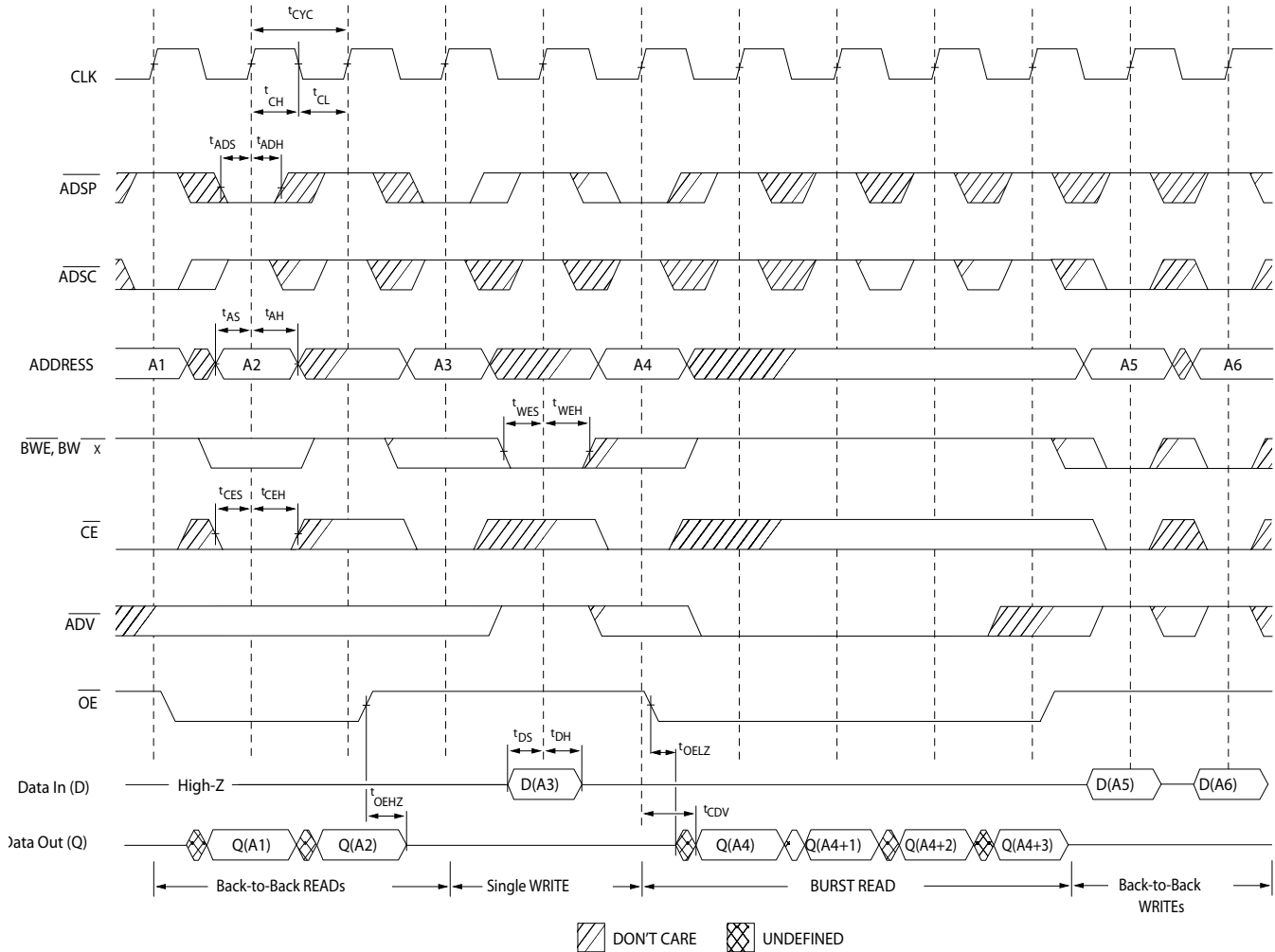


**Notes**

19. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.  
20. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and BW<sub>x</sub> LOW.

**Timing Diagrams** (continued)

**Figure 5. Read/Write Cycle Timing** [21, 22, 23]

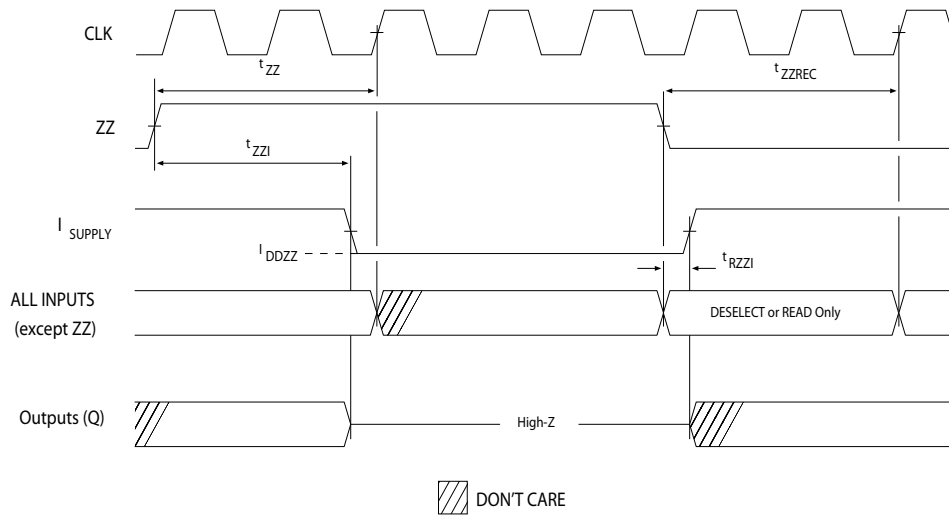


**Notes**

- 21. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 22. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by ADSP or ADSC.
- 23.  $\overline{GW}$  is HIGH.

**Timing Diagrams** (continued)

**Figure 6. ZZ Mode Timing** [24, 25]



**Notes**

- 24. Device must be deselected when entering ZZ mode. See [Truth Table on page 8](#) for all possible signal conditions to deselect the device.
- 25. DQs are in high Z when exiting ZZ sleep mode.

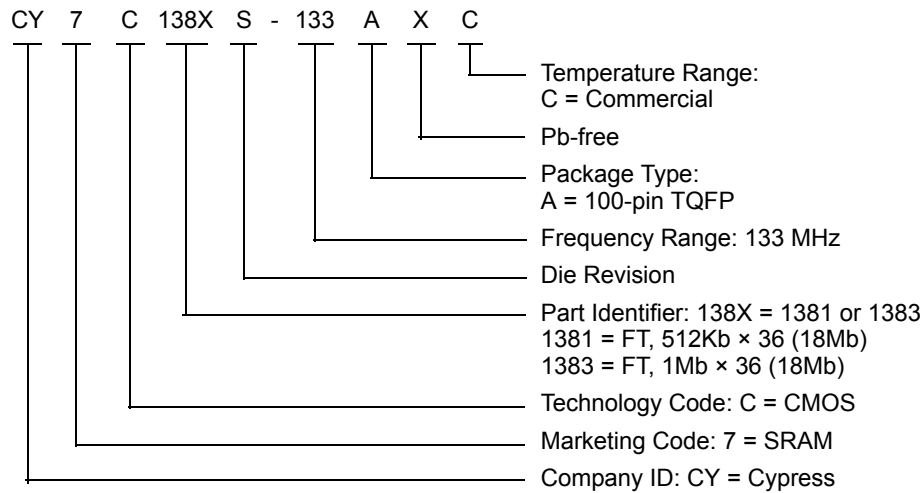


## Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit [www.cypress.com](http://www.cypress.com) for actual products offered.

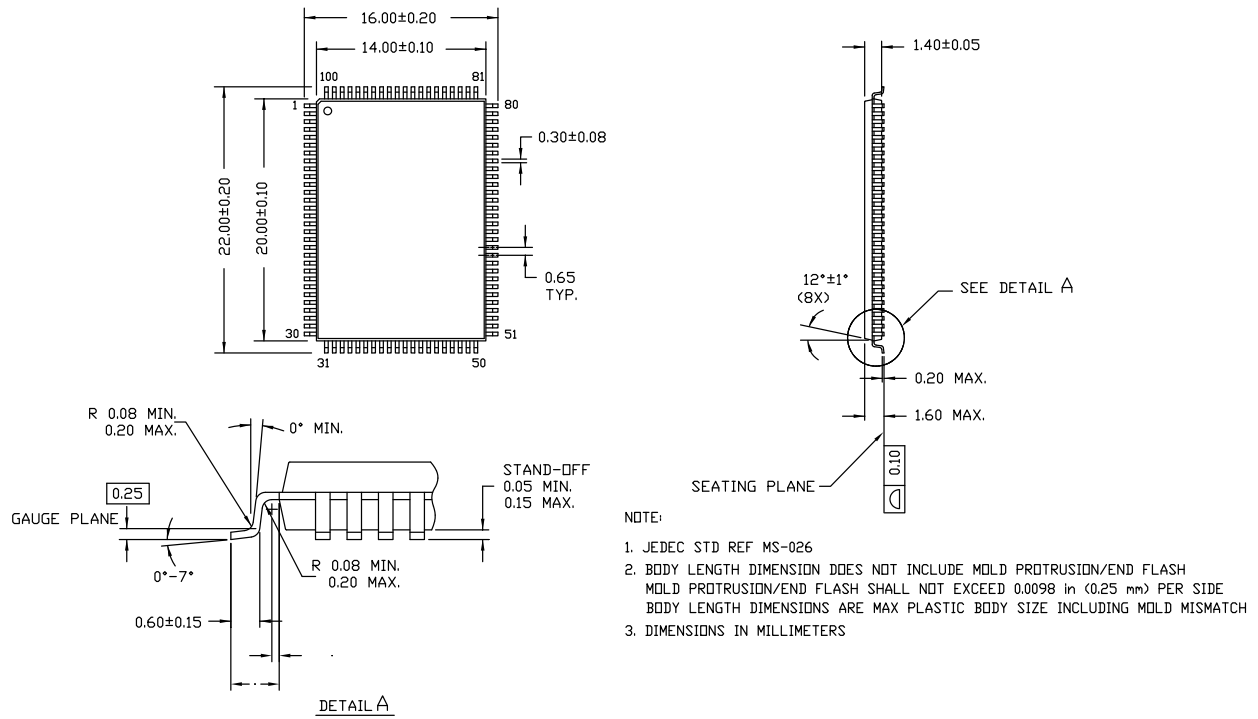
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1381S-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1383S-133AXC			

## Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 \*E

## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1381S/CY7C1383S, 18-Mbit (512K × 36/1M × 18) Flow-Through SRAM Document Number: 001-43825				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	1898286	See ECN	VKN / AESA	New data sheet.
*A	2082246	See ECN	JASM	Changed status from Preliminary to Final.
*B	2950645	06/11/2010	VKN	Updated <a href="#">Ordering Information</a> (Removed invalid parts). Updated <a href="#">Package Diagrams</a> .
*C	3196490	03/15/2011	NJY	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated to new template.
*D	3569737	04/02/2012	PRIT	Updated <a href="#">Functional Description</a> (Removed the Note “For best practices or recommendations, please refer to the Cypress application note AN1064, SRAM System Design Guidelines on <a href="http://www.cypress.com">www.cypress.com</a> .” and its reference, removed the Note “ $\overline{CE}_3$ , $CE_2$ are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in 1 chip enable.” and its reference). Updated <a href="#">Pin Configurations</a> (Removed 119-ball BGA and 165-ball FBGA package related information). Updated <a href="#">Pin Definitions</a> (Removed the Note “ $\overline{CE}_3$ , $CE_2$ are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in 1 chip enable.” and its references, removed JTAG related information). Updated <a href="#">Functional Overview</a> (Removed the Note “ $\overline{CE}_3$ , $CE_2$ are for 100-pin TQFP and 165-ball FBGA packages only. 119-ball BGA is offered only in 1 chip enable.” and its references). Removed IEEE 1149.1 Serial Boundary Scan (JTAG). Removed TAP Controller State Diagram. Removed TAP Controller Block Diagram. Removed TAP Timing. Removed TAP AC Switching Characteristics. Removed 3.3 V TAP AC Test Conditions. Removed 3.3 V TAP AC Output Load Equivalent. Removed 2.5 V TAP AC Test Conditions. Removed 2.5 V TAP AC Output Load Equivalent. Removed TAP DC Electrical Characteristics and Operating Conditions. Removed Identification Register Definitions. Removed Scan Register Sizes. Removed Identification Codes. Removed Boundary Scan Order (corresponding to 119-ball BGA and 165-ball FBGA). Updated <a href="#">Operating Range</a> (Removed Industrial Range). Updated <a href="#">Electrical Characteristics</a> (Removed 100 MHz frequency related information). Updated <a href="#">Capacitance</a> (Removed 119-ball BGA and 165-ball FBGA package related information). Updated <a href="#">Thermal Resistance</a> (Removed 119-ball BGA and 165-ball FBGA package related information). Updated <a href="#">Switching Characteristics</a> (Removed 100 MHz frequency related information). Updated <a href="#">Package Diagrams</a> (Removed 119-ball BGA and 165-ball FBGA package related information).
*E	3975671	04/20/2013	PRIT	Replaced all instances of IO with I/O across the document. Completing Sunset Review.

**Document History Page** (continued)

Document Title: CY7C1381S/CY7C1383S, 18-Mbit (512K × 36/1M × 18) Flow-Through SRAM Document Number: 001-43825				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*F	5187232	03/23/2016	PRIT	Updated <a href="#">Package Diagrams</a> : spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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