AN211622

HyperFlash™ and HyperRAM™ Layout Guide

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Associated Part Family: S26KL-S, S26KS-S, S27KL-S, S27KS-S

AN211622 discusses the layout considerations when placing a Cypress HyperFlash or HyperRAM device on a PCB.

1 Introduction

This document is meant to provide general design recommendations for a PCB designed with Cypress HyperBus™ NOR Flash (S27KL/S27KS) and DRAM Memory (S26KL/S26KS) products. These guidelines include both signal integrity and power delivery guidelines.

In general, to achieve maximum performance, the PCB design should provide impedance-controlled routing for signals, support a low-impedance power delivery system, and control EMI.

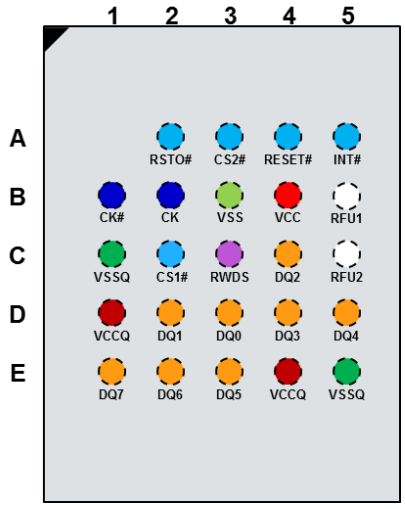
This document does not eliminate the need for you to perform signal integrity/power delivery simulations; you should use this document as an initial reference towards PCB design with Cypress HyperBus memory. You should use Cypress-provided IBIS models (as well as IBIS models from controller vendors) for signal timing/crosstalk simulations. In addition, you should always empirically verify actual signal characteristics on prototype and validation build units.

If your design cannot meet these recommendations, detailed simulations should be performed to determine whether the exceptions will impact HyperBus performance.

2 Signal Descriptions

The following tables and diagrams describe various pins (and their functions) used in HyperBus memory devices.

Figure 1. HyperBus FAB024 and VAA024 Ball Map (Top View, Balls Down)



Note: RFU1 and RFU2 are grouped together as RFU in Table 3.

Table 1. Mandatory I/O Summary

Symbol	Type	Description
CS#	Master Output, Slave Input	Chip Select. HyperFlash bus transactions are initiated with a HIGH to LOW transition. HyperFlash bus transactions are terminated with a LOW to HIGH transition.
CK, CK#	Master Output, Slave Input	Differential Clock. Command / Address / Data information is input or output with respect to the crossing of the CK and CK# signals. CK# is only used on the 1.8-V devices and may be left open or connected to CK on 3-V devices.
DQ[7..0]	Input / Output	Data Input / Output. Command / Address / Data information is transferred on these DQs during read and write transactions.
RWDS	Input / Output	Read Write Data Strobe. Output data during read transactions are edge aligned with RWDS.

Table 2. Optional I/O Summary

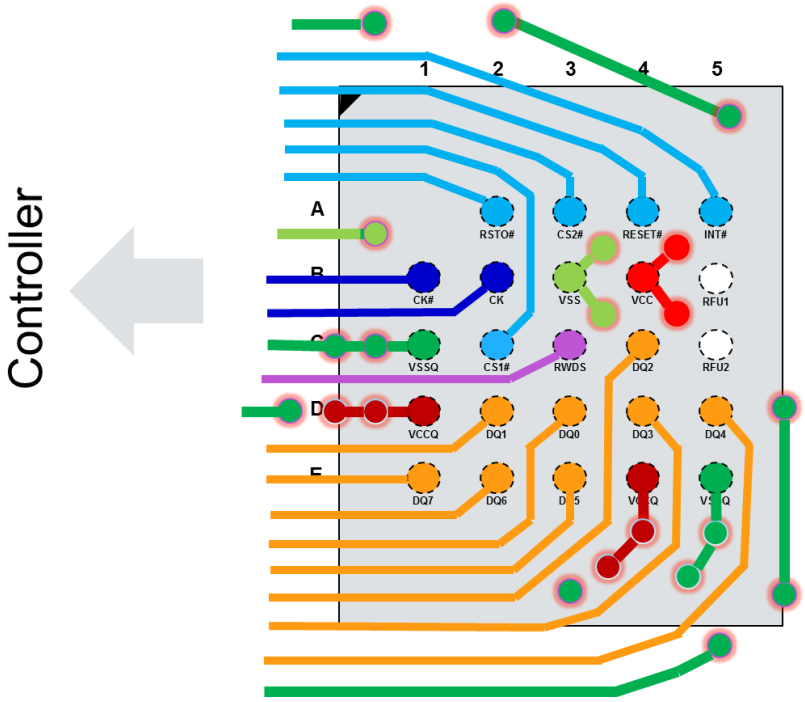
Symbol	Type	Description
RESET#	Master Output, Slave Input, Internal Pull-up	Hardware Reset. When LOW, the device will self-initialize and return to the array read state. RWDS and DQ[7:0] are placed into the HI-Z state when RESET# is LOW. RESET# includes a weak pull-up; if RESET# is left unconnected, it will be pulled up to the HIGH state.
RSTO#	Master Input, Slave Output, Open Drain	RSTO# Output. RSTO# is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system-level reset signal. Upon completion of the internal POR, the RSTO# signal will transition from LOW to HI-Z after a user-defined timeout period has elapsed. Upon transition to the HI-Z state, the external pull-up resistance will pull RSTO# HIGH and the device immediately is placed into the Idle state.
INT#	Master Input, Slave Output, Open Drain	INT Output. When LOW, the device indicates that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.

Table 3. Other Connectors Summary

Symbol	Type	Description
VCC	Power Supply	Core Power
VCCQ	Power Supply	Input / Output Power
VSS	Power Supply	Core Ground
VSSQ	Power Supply	Input / Output Ground
NC	No Connect	Not Connected Internally. The signal/ball may be used in PCB as part of a routing channel.
RFU	Reserved	Reserved for Future Use. May or may not be connected internally, the signal/ball should be left unconnected and unused on PCB as a part of a routing channel for future compatibility. The signal/ ball may be used by a signal in the future.
DNU	No Connect	Do Not Use. Reserved for use by Cypress. The signal/ball is connected internally. The signal/ball must be left open on the PCB

3 Package Breakout Recommendations

Figure 2. FAB024 and VAA024 PCB Breakout



Note: Even though both CS1# and CS2# breakouts are shown above, only breakout the chip selects needed for the specific configuration (see the applicable datasheet)

- As shown in Figure 2, it is possible to breakout all signals on the top layer before redirecting them towards the controller. This is only one of the options for breakout. If multiple layers are available for breakout, different breakout strategies can be used as long as routing and power delivery guidelines shown in this section and the General Signal Routing Guidelines section are met.
- **VSSQ** and **VSS** should be taken to VSS plane layer with at least two vias next to each solder ball. Traces from land pad to via should be as thick as possible.
- **VCC** and **VCCQ** should be taken to VCC plane layer with at least two vias next to each solder ball. Traces from land pad to via should be as thick as possible.
- As shown in Figure 2, priority is given to first breakout **DQ (0-7)** as well as **RWDS** in the direction of the controller to allow for the smallest data channel length between HyperBus memory and controller.
- **CK** and **CK#** should be broken out in a coupled fashion, i.e., maintain the trace width and trace spacing between these signals identical throughout the breakout region as much as possible (this is true when they exit the breakout area). In addition, shield the clocks with VSS guard traces if possible.
- All signals should be broken out on the top layer while maintaining a solid VSS underneath. This will allow better impedance control and smaller impedance mismatch between breakout traces and traces outside the breakout area.
- The VSS guard traces shown above are meant to act as additional referencing against signals of other interfaces and should really be more planar and well stitched with the VSS layer (shown as traces only for pictorial reasons).
- Within the PCB breakout region, use the following SMT recommendations:
  - Ball-to-ball pitch: 1.00 mm
  - Ball pad size: 0.35 mm
  - SR opening size: 0.5 mm

- Minimum trace width and trace spacing: 4 mil or larger spacing between traces (at least 4-mil trace width: 4-mil trace spacing).Once the routing clears the breakout region, it is recommended to follow the general routing guidelines reflected in this section.
- Whenever through-hole vias are used to move breakout traces to inner layers, the potential via coupling effect (from one signal via to another signal via) should be considered at the breakout region. Preferably, no vias should be used for DQ0-DQ7 and RWDS signal routes. If they have to be used, minimize the via count and use same number of vias on all DQ0-7 and RWDS. It is preferred to use µvias or buried vias instead of through-hole vias.

4 General Signal Routing Guidelines

The following guidelines define recommended impedance, trace width/spacing, total length limitation, and length-matching requirements to achieve optimal signal integrity and timing margins.

- The exact values of signal trace width and trace spacing should be determined based on the trace impedance requirement.
- It is preferred to have to solid VSS as reference for all signal routing layers. Reference planes should avoid any gaps or voids to minimize return current discontinuity.
- Isolate the ground return path of analog signals from digital noise whenever applicable.
- Cypress recommends that the VSS plane be used as the primary reference or return path for all signals. Whenever a power layer is used as reference plane, it is important to ensure that the power layer is low-noise and there is proper stitching at the reference plane transitions to guarantee return path continuity (especially at high frequency). The power layer should only be considered as a secondary signals reference option where a solid continuous ground reference is present.
- All recommended signal routing lengths are defined from package pin (source) to package pin (destination) by considering HyperBus package length compensation.
- Electrical properties of the recommended signal routing are based on dielectric material with FR4 assumption.
- It is assumed that 1 inch ~166 ps (assuming FR4 material). You should use your signal integrity tools to ensure the accuracy of this assumption.
- Consider performing signal integrity simulations using Cypress-provided IBIS models to determine actual guidelines suitable for your application. The following guidelines should be used as a starting reference.
- Normally, signal delay is measured between T***vm*** (timing reference voltage, which is usually VCCQ/2) of the source and T***vm*** of the destination. However, pay attention to the signal polarity in the datasheet to determine the edge the timing is measured at (rising or falling edge).

4.1 Microstrip versus Stripline versus Co-Planar Signal Routing

Table 4. Comparison of Microstrip, Stripline, and Co-planar Signal Routing

Microstrip Line	Stripline	Coplanar Line
Suffers from dispersion and non-TEM (Transverse Electrical and Magnetic) modes	Pure TEM mode	Suffers from dispersion and non-TEM modes
Easy to fabricate	Difficult to fabricate	Fairly difficult to fabricate
High-density trace	Mid-density trace	Low-density trace
Fair for coupled-line structures	Good for coupled-line structures	Not suitable for coupled-line structures
Need through-holes to connect to ground	Need through-holes to connect to ground	No through-hole required to connect to ground

- Either microstrip or stripline signal routing is allowed as long as the continuous trace impedance of 50 ohm (±10%) is maintained through the entire routing path. Manufacturing tolerances of layer thickness, dielectric constant and so on should be modeled in the impedance calculation.
- In general, whenever through-hole vias are used on the board, they cause impedance discontinuities due to additional capacitive loading as well as possible inductive stubs at high frequency. Any via that attaches to a trace will change the delay of that trace. It is therefore preferred to use µvias or buried vias and keep the via count at a minimum.
- In order to preserve a tight skew relationship, DQ0-DQ7 and RWDS should have the same number of vias and layer changes. This will help to ensure that data signals along with the accompanying strobe will see the same effective delay.
- It is recommended to route DQ0-DQ7 and RWDS on the same signal layer.
- CK and CK# should be routed in a coplanar fashion while maintaining the single-ended impedance of 50 ohms and differential impedance of 100 ohms (nominal value).

4.2 Signal-Routing Length Constraints

4.2.1 Maximum Total Length

The absolute maximum total length of DQ signals (including RWDS) with respect to its reference plane is defined by the total load capacitance, which directly impacts the signal quality.

- The total load capacitance is preferred to be < 20 pF.
- Total load capacitance includes the following:
  - Total line length capacitance (~3.3 pF/inch with FR4 assumption),
  - Max package pin capacitance of the controller package
  - Any parasitic capacitance associated with vias, and so on.

4.2.2 Length Matching

- Length matching refers to trace lengths from the HyperBus memory package pin to the signal pin of the controller and must include the effective electrical length of the vias.

Signal Group	Length Match Tolerance (166 MHz)	Length Match Tolerance (100 MHz)
CK to CK#	± 10 mils	± 20 mils
RWDS to DQ0-7	± 25 mils	± 50 mils
DQx (0-7) to DQy (0-7)	± 50 mils	± 100 mils
CK/CK# to DQ0-7	± 500 mils	
CK/CK# to CS#	± 1500 mils	
CK/CK# to RWDS	+/-1500 mils	
RESET# to RSTO# to CS#	± 2000 mils	

4.2.3 Signal Spacing Constraints from Other Signals

- CK and CK# : > 2H
- RWDS > 2H
- DQ0~DQ7 >1.5H
- CS#, CS2# : > 1.5H
- INT#, RESET, RST_N : > 1.5H
  - Where H is the height of the dielectric between signal and VSS (reference layer)

4.2.4 Termination

You should review the drive strength/impedance of the controller I/O for CK, CS#, RWDS, and DQ as well as transmission line routing to determine whether series termination is needed on these lines.

5 Power Delivery Guidelines

The following power delivery guidelines will help to ensure that there are no power issues in the system:

- VSS/VSSQ balls should be connected to a solid ground plane with its own unique via and if possible > 1 vias. This will improve IR drop.
- VCC/VCCQ balls should be connected to a single supply plane with its own unique via and if possible > 1 vias. This will improve IR drop.
- Isolate VCC/VCC of HyperBus from other noisy supply floods. If the supplies of HyperBus and non-HyperBus bus have to be co-located on the same plane layer, maintain a > 40-mil gap. In addition, if possible, add shielding VSS guard traces between the planes for further isolation.
- It is recommended to keep supply trace lengths ≤ 400 mil and trace width ≥ 20 mils. This applies to HyperBus memory, MCU, as well as voltage regulator routing.
- Maintain low-impedance routing (traces > 20mils) from voltage regulator to HyperBus supply pins as well as from voltage regulator to controller HyperBus I/F supply pins.

  It is recommended to add VCC/VSS test points as close to the HyperBus memory package as well as next to the voltage regulator. This will allow measurement of the VCC-VSS waveform at both VRM as well as HyperBus memory package.

Follow decoupling guidelines provided by the microcontroller and VRM vendors.

5.1.1 Decoupling Capacitors Recommendations

- Place the following PCB decoupling capacitors as close to the HyperBus memory package as possible:
  - At least two 1-µF 0402 ceramic capacitors
  - At least four 0.1-µF 0402 ceramic capacitors
  - Put one 1-µF capacitor closest to D1 (VCCQ) and another closest to E4. Similarly, two 0.1-µF capacitors closest to D1 and another two closest to E4.
  - If VCC and VCCCQ are shorted, make sure that the short is as low-impedance as possible. If the short is not low-impedance, it is recommended to add 0.1-µF and 1-uF capacitors close to the VCC pin.
- The selected capacitor should have low ESL and ESR.
- VCC and VSS trace routing from the capacitor should be as wide as possible to avoid inductive/resistive effects.
- X7R or X5R capacitors are recommended with rated voltage ≥ 6.3 V.
- Capacitor placements on either top layer or bottom layer are allowed as long as the capacitor is electrically close to the DQ routing and VCCQ/VSSQ pins (For example, do not place capacitors at the bottom when using a very thick board).

6 Test Points and Oscilloscope Measurements

Signal quality, timing, and power delivery characterization should be performed per industry standard, high-speed digital signal evaluation techniques. Some of these techniques are outlined below:

- Test points should be added as close to controller for DQ0-7/RWDS and close to the HyperBus memory package for all signals.
- When controller is driving, the meaningful signal to look at is as close to HyperBus memory as possible; when HyperBus memory is driving, the opposite is true.
- While creating a test pad, the stub (extra inductance and capacitance) resulting from such a pad should be minimized. If you can probe at the breakout via, it is better than creating test pad stubs. In addition, in the case of a 4-layer PCB with through-hole vias, if possible, probe the signals at the bottom of the PCB on these vias.
- While performing scope measurements, use 6-GHz or greater bandwidth scope and high-impedance probes. This will allow you to see the waveform transition (such as rising and falling portion of the waveform) more accurately.
- Always measure VCC-VSS at the controller, voltage regulator, next to the connector (either side), and at HyperBus memory. This needs to be done before making any signal measurements to ensure that the supply is not noisy. A noisy supply will impact signal timing. In addition, these measurements establish the IR drop from regulator to controller or regulator to HyperBus memory.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals such as clock or RWDS.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5188738	AHCL	03/24/2016	New application note
*A	5471322	AHCL	10/12/2016	Clarified decoupling recommendation Updated template
*B	5740230	SZZX	05/19/2017	Changed low-impedance probes in section 6 to high-impedance probes.

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