Using Low-Power Modes in TRAVEO™ Family S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/ S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/ S6J3400 Series MCUs

About this document

Scope and purpose

AN209715 describes how to use low-power modes in the TRAVEO™ family S6J3110/S6J3120/S6J3200/S6J3310/ S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/S6J3400 series MCUs. Major topics include entering low-power modes and returning to normal operation modes.

Associated Part Family

TRAVEO™ Family S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/ S6J3370/S6J3400 Series

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1 Introduction

The power-saving state (PSS) mode in the TRAVEO™ family S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/S6J3400 series MCUs allows you to reduce the overall power consumption while retaining essential functionality. This application note describes the PSS mode and provides information on how to enter the PSS mode and return to the normal operation mode: the RUN mode.

2 TRAVEO™ Family power modes

The TRAVEO™ family S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/S6J3400 series MCUs feature PSS modes and RUN modes.

- RUN mode − Normal operation and CPU sleep
- PSS mode − Timer mode, STOP mode, and Partial Wake Up (PWU) mode.

Table 1 shows the power modes that S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/S6J3400 series support.

Table 1 Power modes comparison

Power mode / Series	RUN mode		PSS mode				
	Normal operation	CPU sleep	Timer mode	STOP mode	PWU mode	Timer mode (Shutdown)	STOP mode (Shutdown)
S6J3110	Provided	Provided	Provided	Provided	Provided	Provided	Provided
S6J3120	Provided	Provided	Provided	Provided	Provided	Provided	Provided
S6J3200	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3310	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3320	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3330	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3340	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3350	Provided	Provided	Provided	Provided	Not provided	Provided	Provided
S6J3360	Provided	Provided	Provided	Provided	Provided	Provided	Provided
S6J3370	Provided	Provided	Provided	Provided	Provided	Provided	Provided
S6J3400	Provided	Provided	Provided	Provided	Provided	Provided	Provided

2.1 S6J3110/S6J3120 Series power modes

Based on the power consumption and functionality, S6J3110 series power modes are arranged in the order listed in **Table 2**, which shows the typical current for each power mode in the S6J3110 series. For the current in the S6J3120 series power modes, refer to the **Datasheet**.

Table 2 Power mode specs (S6J3110 series)

Power mode		Current range of S6J311E series (typical) VDD = 5.0 V +5 %/–10%, VSS = 0.0 V, Ta = 25 °C
RUN mode	Normal operation	140 mA: Operating at 144 MHz
	CPU sleep	82 mA: Operating at 144 MHz
PSS mode	Timer mode	946.0 µA: Slow-CR source oscillation

TRAVEO™ Family power modes

Power mode		Current range of S6J311E series (typical) VDD = 5.0 V +5 %/–10%, VSS = 0.0 V, Ta = 25 °C
	STOP mode	945.1 µA
	PWU mode	47.1 µA: PWU operation cycle, 32 ms
	Timer mode (shutdown)	40.9 µA: Slow-CR source oscillation
	STOP mode (shutdown)	40.1 µA

For more information on the power modes, refer to the **Hardware Manual**.

Table 3 highlights the differences among the power modes in terms of peripheral availability.

Table 3 Power mode peripheral availability for S6J3110/S6J3120 series

Peripheral	Normal operation	CPU sleep	Timer mode[1]	STOP mode	PWU mode	Timer mode[1] (Shutdown)	STOP mode (Shutdown)
CPU (PD3)	ON	OFF	OFF	OFF	OFF[2]	OFF[2]	OFF[2]
Flash memory (PD3)	ON	OFF	OFF[3]	OFF[3]	OFF[2]	OFF[2]	OFF[2]
Backup RAM (PD4)	ON	OFF	OFF[4]	OFF[4]	OFF[4]	OFF[4]	OFF[4]
Internal regulator	Main[5]	Main[5]	Main[5]	Main[5]	Standby[6]	Standby[6]	Standby[6]
Power domain (PD1)	ON	ON	ON	ON	ON	ON	ON
Power domain (PD2/PD3)	ON	ON	ON	ON	OFF	OFF	OFF
Power domain (PD4)	ON	ON	ON	ON	ON	ON	ON
Power domain (PD6)	ON	ON	ON	ON	OFF	OFF	OFF

There are five power domains in the MCU. Each can be isolated and can select power ON or power OFF. Power Domain 1 (PD1) is always the power-supplying area, which includes some modules such as a real-time clock (RTC), an external interrupt control, and a hardware watchdog timer that should work during low-power modes. Power Domain 2 (PD2) includes most peripheral modules, and Power Domain 3 (PD3) includes mainly the CPU and flash memory. Power Domain 4 (PD4) includes only two backup RAMs. Power Domain 5 (PD5) is not included in this MCU, and Power Domain 6 (PD6) includes a few peripheral modules.

[1] Timer mode selects between two resource clocks. One is the Slow-CR oscillator, which is for both the S6J3110 and S6J3120 series, and the other is the Main oscillator, which is only for the S6J3120 series.

[2] OFF – Power down

[3] OFF – Flash is in deep sleep.

[4] OFF – Backup RAM sleeps, but RAM data is retained.

[5] Main – Regulator is in main mode. All parts of the regulator are running.

[6] Standby – Regulator is in standby mode. Some parts of the regulator are running.

2.2 S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350 series power modes

S6J3200 series power modes are arranged in the order listed in **Table 4**, which shows the typical current for each power mode in the S6J3200 series. For the current in the S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350 series power modes, refer to the **Datasheet**.

Table 4 Power mode specs (S6J3200 series)

Power mode		Current range of S6J3200 series (typical) Vcc5 = 5.0 V, Vcc12 = 1.2V, VSS = 0.0 V, Ta = 25 °C
RUN mode	Normal operation	45 mA: Vcc5 820 mA: Vcc12 (CPU: 240 MHz, GDC 2D and 3D : 200 MHz)
PSS mode	Timer mode (shutdown)	85.0 µA: Vcc5 (32 kHz for sub oscillation PD1=ON, PD4=ON, PD6=OFF)
	STOP mode (shutdown)	65.0 µA: Vcc5 (PD1=ON, PD4=ON)

For more information on the power modes, refer to the **Hardware Manual**.

Table 5 highlights the differences among the power modes in terms of peripheral availability.

Table 5 Power mode peripheral availability for S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350 series

Peripheral	Normal operation	CPU sleep	Timer mode[7]	STOP mode	Timer mode[7] (Shutdown, PD6 ON)	Timer mode[8] (Shutdown, PD6 OFF)	STOP mode (Shutdown)
CPU (PD2)	ON	OFF	OFF	OFF	OFF[9]	OFF[9]	OFF[9]
Flash memory (PD2)	ON	OFF	OFF[10]	OFF[10]	OFF[9]	OFF[9]	OFF[9]
Backup RAM (PD4)	ON	OFF	OFF[11]	OFF[11]	OFF[11]	OFF[11]	OFF[11]
Internal regulator	Main[12]	Main[12]	Main[12]	Standby[13]	Main[12]	Standby[13]	Standby[13]
Power domain (PD1)	ON	ON	ON	ON	ON	ON	ON
Power domain (PD2/PD3/PD5)	ON	ON	ON	ON	OFF	OFF	OFF
Power domain (PD4)	ON	ON	ON	ON	ON	ON	ON
Power domain (PD6)	ON	ON	ON	ON	ON	OFF	OFF

[7] Timer mode – Possible source clocks are Main oscillator, Sub oscillator, Slow-CR, and Fast-CR.

[8] Timer mode – Possible source clocks are Main oscillator, Sub oscillator, and Slow-CR.

[9] OFF – Power down

[10] OFF – Flash is in deep sleep.

[11] OFF – Backup RAM sleeps, but RAM data is retained.

[12] Main – Regulator is in main mode. All parts of the regulator are running.

[13] Standby – Regulator is in standby mode. Some parts of the regulator are running.

There are six power domains in the MCU. Each can be isolated and can select power ON or power OFF. Power Domain 1 (PD1) is always the power-supplying area, which includes some modules such as a real-time clock (RTC), an external interrupt control, and a hardware watchdog timer that should work during low-power modes. Power Domain 2 (PD2) includes mainly the CPU, flash memory, and most peripheral modules. Power Domain 3 (PD3) and Power Domain5 (PD5) are included in PD2. Power Domain 4 (PD4) includes only two backup RAMs. Power Domain 6 (PD6) includes a few peripheral modules.

2.3 S6J3360/S6J3370/S6J3400 series power modes

S6J3400 series power modes are arranged in the order listed in **Table 6**, which shows the typical current for each power mode in the S6J3400 series. For the current in the S6J3360/S6J3370 series power modes, refer to the datasheet.

Table 6 Power mode specs (S6J3400 series)

Power mode		Current range of S6J3400 series (typical) VCC = AVCC = 5.0 V ±0.5V, VSS = AVSS = 0.0 V, Ta = 25 °C
RUN mode	Normal operation	85 mA: Operating at 132 MHz
	CPU sleep	55 mA: Operating at 132 MHz, Peripheral at 33 MHz
PSS mode	Timer mode	1300.0 µA: Slow-CR source oscillation
	STOP mode	1300.0 µA
	Timer mode (shutdown)	245.0 µA: Slow-CR source oscillation
	STOP mode (shutdown)	245.0 µA

For more information on the power modes, refer to the **Hardware Manual**.

Table 7 highlights the differences among the power modes in terms of peripheral availability.

Table 7 Power mode peripheral availability for S6J3360/S6J3370/S6J3400 series

Peripheral	Normal operation	CPU sleep	Timer mode[14]	STOP mode	PWU mode	Timer mode[14] (Shutdown)	STOP mode (Shutdown)
CPU (PD2)	ON	OFF	OFF	OFF	OFF[15]	OFF[15]	OFF[15]
Flash memory (PD2)	ON	OFF	OFF[16]	OFF[16]	OFF[15]	OFF[15]	OFF[15]
Backup RAM (PD4)	ON	OFF	OFF[17]	OFF[17]	OFF[17]	OFF[17]	OFF[17]
Internal regulator	Main[18]	Main[18]	Main[18]	Main[18]	Standby[19]	Standby[19]	Standby[19]
Power domain (PD1)	ON	ON	ON	ON	ON	ON	ON

[14] Timer mode – Possible source clocks are Main oscillator, Sub oscillator, Slow-CR, and Fast-CR.

[15] OFF – Power down

[16] OFF – Flash is in deep sleep.

[17] OFF – Backup RAM sleeps, but RAM data is retained.

[18] Main – Regulator is in main mode. All parts of the regulator are running.

[19] Standby – Regulator is in standby mode. Some parts of the regulator are running.

Peripheral	Normal operation	CPU sleep	Timer mode[14]	STOP mode	PWU mode	Timer mode[14] (Shutdown)	STOP mode (Shutdown)
Power domain (PD2)	ON	ON	ON	ON	OFF	OFF	OFF
Power domain (PD4)	ON	ON	ON	ON	ON	ON	ON

There are three power domains in the MCU. Each can be isolated and can select power ON or power OFF. Power Domain 1 (PD1) is always the power-supplying area, which includes some modules such as a real-time clock (RTC), an external interrupt control, and a hardware watchdog timer that should work during low-power modes. Power Domain 2 (PD2) includes mainly the CPU, flash memory and most peripheral modules. Power Domain 4 (PD4) includes only two backup RAMs.

3 Entering PSS mode and returning to RUN mode

This section describes how to enter the STOP (shutdown) mode from the RUN mode, which is operated with the PLL oscillation, and how to return to RUN mode via an external interrupt.

The following steps are necessary to change RUN mode to PSS mode:

1. Set the interrupt factors for returning from PSS mode to RUN mode.
2. If PD2 and PD3 go OFF, ensure that the PLL oscillation is stable before setting the PSS profile register.
3. Set the PSS profile group register for PSS mode.

3.1 Set interrupt factors

When interrupt factors return to the RUN mode from the PSS mode, they use peripheral resource interrupts, external interrupts, nonmaskable interrupts (NMIs), and so on. If the factor uses an external interrupt when returning from the PSS mode, you should set the external interrupt register before it enters the PSS mode. An interrupt controller does not need to be set in the shutdown mode of the PSS mode as it does in the STOP (shutdown) mode.

3.2 Stabilize PLL oscillation

Before entering the STOP (shutdown) mode, the PLL oscillation must be stable and the Fast-CR clock must be selected as the resource clock during the RUN mode. Stabilizing the PLL oscillation uses the clock gear controller.

Selecting a resource clock and clock configuration sets the RUN profile group registers and then enables the RUN profile update.

3.2.1 Clock gear control

The clock gear controller starts the following procedure. After the clock gear controller starts, wait for the clock gear operation to be completed.

1. Set the PLL clock gear start register bit: SYSC_PLL0CGCNTR.PLLCGSTR 1(b).
2. Read the PLL clock gear status register bit, SYSC_PLL0CGCNTR.PLLCGSTS, repeatedly until the PLL oscillation is stable (PLLCGSTS: 00(b)).

Note: SSGGPLL must also be stable.

3.2.2 RUN profile

After the clock gear operation is completed, disable the PLL/SSCGPLL clock and change the source clock to the Fast-CR clock to set RUN profile registers, and then update the RUN profile.

When transitioning to the PSS mode, create a 1:1:1:1 relationship among the CPU clock, the Memory Configuration clock, the System Control Unit (SCU) clock, and the MCU (MCUCH) clock. The loss of this relationship among these clocks may cause abnormal operation. **Table 8** provides an example for setting the Fast-CR clock.

The Main clock must be enabled during RUN mode even though the Fast-CR clock is selected as the source clock.

Table 8 and **Table 9** show example register settings of the RUN profile before PSS entry.

(CPU clock: Memory **Configuration** clock; SCU clock: MCUCH clock = 1:1:1:1)

Table 8 Example register settings for source clock to Fast-CR

Register	Bit	Description	Value
SYSC1_RUNCKSELR0	CD0CSL	Clock domain 0 clock selection bits	000(b)
SYSC1_RUNCKDIVR0	HPMDIV	HPM clock divider setting bits	000(b)
	SYSDIV	SYS clock divider setting bits	0_0000(b)
SYSC0_RUNCKSELR	CDMCUCCSL	Clock domain MCUC clock selection bits	000(b)
SYSC0_RUNCKDIVR	MCUCHDIV	MCU configuration AHB clock divider setting bits	0_0000(b)

Table 9 Example register settings for PLL/SSCG PLL disable

Register	Bit	Description	Value
SYSC0_RUNCKSRER	PLL0EN	PLL0 clock oscillation enable bit	0(b)
	SSCG0EN	SSCG PLL0 clock oscillation enable bit	0(b)
	MOSCEN	Main clock oscillation enable bit	1(b)

3.2.3 RUN profile update

RUN profile registers are not validated until the profile update procedure is completed as follows:

1. Set the values in the RUN profile registers you want to change.
2. Clear the status flag register for a complete RUN profile update (SYSC0_SYSICLR.RUNDFCLR0=1(b)).
3. Write 0xAB to the RUN profile update enable register (SYSC1_RUNENR=0xAB).
4. Write 0xAB to the RUN profile update trigger register (SYSC0_TRGRUNCNTR.APPLY_RUN=0xAB).
5. Read the system status register, SYSC0_SYSSTSR.RUNDF0, repeatedly until this bit goes to 1(b).

An NMI occurs when there are errors in setting the combination of RUN profile registers. Check the RUN profile error flag register (SYSC0_SYSRUNPEFR) before performing step 2.

3.3 Change PSS profile

Before entering the PSS mode, PSS profile registers should be set to the STOP (shutdown) mode in this example.

3.3.1 PSS profile

Table 10 lists the PSS profile registers for STOP (shutdown) mode.

- Power domain setting: PD2/PD3(CPU, FLASH)=OFF, PD4(Backup RAM)=ON, PD6=OFF
- Source clock setting: All-OFF (Slow-CR, Fast-CR, Main Oscillator, PLL, SSCGPLL)

Table 10 describes example settings of the PSS profile registers for STOP (shutdown) mode.

Table 10 Example register settings for STOP (Shutdown) mode

Register	Description	Value
SYSC0_PSSPDCFGR	PSS power domain setting	0x00030000
SYSC0_PSSCKSRER	PSS clock source enable	0x00000000
SYSC1_PSSCKER0	PSS clock source enable 0	0x00000000
SYSC1_PSSCKER1	PSS clock source enable 1	0x00000000
SYSC0_PSSCKSELR	PSS clock source selection	0x00000000
SYSC0_PSSCKER	PSS clock enable	0x00000000
SYSC1_PSSCKSELR0	PSS clock source selection	0x00000000
SYSC0_PSSREGCFGR	PSS regulator setting	0x00000080

3.3.2 PSS profile update and PSS mode entry

PSS profile registers are not validated until the profile update procedure is completed as follows:

1. Set the values in the PSS profile registers you want to change.
2. Write 0xBA to the PSS profile update enable register (SYSC1_PSSENR.PSSEN1=0xBA).
3. Write 0xBA to the PSS profile update enable register (SYSC0_PSSENR.PSSEN0=0xBA).
4. Execute Wait for Interrupt (WFI) of the Arm® Cortex®-R5 CPU instruction.

An NMI occurs when there are errors in setting the combination of PSS profile registers. Check the PSS profile error flag register (SYSC0_SYSPSSPEFR) before performing step 2.

After execution (step 4), the MCU goes to PSS mode. When a signal prepared during RUN mode interrupts the MCU, the MCU goes back to RUN mode, which is the same as the RUN profile setting before entering PSS mode. The MCU runs from the beginning of the program when returning to RUN mode from PSS (shutdown) mode.

4 Summary

The S6J3110/S6J3120/S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/S6J3370/S6J3400 series has several low-power modes that make it easy to reduce power consumption when the CPU does not operate.

5 Related documents

- **S6J311E/D/C/B Series Datasheet** (Doc. No. 002-05681)
- **S6J311A/9/8 Series Datasheet** (Doc. No. 002-04632)
- **S6J3110 Series Hardware Manual** (Doc. No. 002-10667)
- **S6J3120 Series Datasheet** (Doc. No. 002-04863)
- **S6J3120 Series Hardware Manual** (Doc. No. 002-04855)
- **S6J3200 Series Datasheet** (Doc. No. 002-05682)
- **S6J3200 Series Hardware Manual** (Doc. No. 002-04852)
- **S6J32E/F/G Series Datasheet** (Doc. No. 002-10689)
- **S6J32E/F/G Series Hardware Manual** (Doc. No. 002-12500)
- **TRAVEO Family Hardware Manual Platform Part for S6J3200 Series** (Doc. No. 002-04854)
- **S6J3310/20/30/40 Series Datasheet** (Doc. No. 002-10635)
- **S6J3350 Series Datasheet** (Doc. No. 002-10634)
- **S6J3310/20/30/40/50 Series Hardware Manual** (Doc. No. 002-10185)
- **TRAVEO Family Hardware Manual Platform Part for S6J3310/3320/3330/3340/3350 Series** (Doc. No. 002-07884)
- **S6J3360/70 Series Datasheet** (Doc. No. 002-03359)
- S6J3360/70 Series Hardware Manual (Contact **Technical Support**)
- **TRAVEO Family Hardware Manual Platform Part for S6J3360/3370 Series** (Doc. No. 002-07884)
- **S6J3400 Series Datasheet** (Doc. No. 001-97829)
- **S6J3400 Series Hardware Manual** (Doc. No. 002-09919)
- **TRAVEO Family Hardware Manual Platform Part for S6J3400 Series** (Doc. No. 002-07884)

Revision history

Document version	Date of release	Description of changes
**	2016-02-24	New application note.
*A	2016-07-12	Updated Associated Part Family as “Traveo Family S6J3110/S6J3120/ S6J3200/S6J3400 Series”. Added target part numbers “S6J3200/S6J3400 Series” related information in all instances across the document. Updated to new template.
*B	2017-02-17	Updated Associated Part Family as “Traveo Family S6J3110/S6J3120/ S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3400 Series”. Added target part numbers “S6J3310/S6J3320/S6J3330/S6J3340/ S6J3350 Series” related information in all instances across the document.
*C	2017-05-26	Updated Associated Part Family as “Traveo Family S6J3110/S6J3120/ S6J3200/S6J3310/S6J3320/S6J3330/S6J3340/S6J3350/S6J3360/ S6J3370/S6J3400 Series”. Added target part numbers “S6J3360/S6J3370 Series” related information in all instances across the document. Updated to new template.
*D	2019-03-11	Updated to new template. Completing Sunset Review.
*E	2021-06-22	Updated to Infineon template.

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