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AN211345

Software Migration Guide for Macronix MX25UM OctaFlash Family to Cypress HyperFlash™ Family

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Associated Part Family: S26KL-S, S26KS-S
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AN211345 provides guidelines for software migration from the Macronix MX25UM OctaFlash family to the Cypress S26KL/S26KS HyperFlash family. It describes the similarities and differences in the configuration of address spaces and command codes to facilitate the conversion.

Contents

1 Introduction

This application note provides guidelines for software migration from the Macronix MX25UM OctaFlash family to the Cypress S26KL/S26KS HyperFlash family.

The Cypress S26KL/S26KS HyperFlash family and the Macronix MX25UM OctaFlash family have very similar pin configurations but completely different command sets. The S26KL/S26KS HyperFlash family adopts the command set of traditional Parallel NOR (PNOR) Flash Memory devices such as the Cypress S29GL-S family. The HyperBus® controller integrated in the host system translates software accesses to the HyperBus signal protocol. This makes the electrical signaling and bus protocol differences between HyperBus and PNOR transparent to the software. As a result, users can use traditional PNOR software such as the Cypress Low Level Driver for NOR flash which contains the full support for the S26KL/S26KS command set.

The Cypress S26KL/S26KS HyperFlash family can also replace the Macronix MX25UM OctaFlash Family with the software migration guidelines provided in this application note. This application note maps software features like address spaces, data protection, and command sets for accessing the flash memory array or registers. In terms of the hardware interface, Cypress HyperFlash supports the following features while the Macronix OctaFlash doesn't.

- **Hybrid Burst:** A new type of burst mode that can combine one wrapped burst followed by a linear bust.[1]
- **INT# Output:** This output is used to indicate to the host system that an event has occurred within HyperFlash.
- **RSTO# Output:** This output is used to indicate when a Power-On-Reset (POR) is occurring within the HyperFlash device.

Details of these features and any other topics relevant to the hardware interface such as signaling, timing, and bus protocol are out of the scope of this document. See corresponding datasheet sections for these details.

[1] Supported by the 256-Mb and 128-Mb parts only. Not supported by the 512-Mb part.

2 Address Space Maps

The S26KL/S26KS HyperFlash family has a set of address spaces as follows:

Address Space	Description	OctaFlash Equivalent
Flash Memory Array	The main nonvolatile memory array used for data storage.	Flash Memory Array
ID/CFI	Factory-programmed memory array used for Cypress device characteristics information	Serial Flash Discoverable Parameter (SFDP)
Secure Silicon Region (SSR)	The 1024-byte one-time programmable (OTP) nonvolatile memory area used for Cypress factory-programmed and customer-programmable permanent data.	Secured OTP
Persistent Protection Bits (PPB)	The nonvolatile memory array with one bit for each sector. When programmed, each bit protects the related sector from erasure and programming.	Solid Protection Bits (SPB)
PPB Lock Bit	The volatile register bit used to enable or disable programming and erase of the PPB bits.	SPB Lock Down Bit (SPBLKDN), but it is one-time-programmable
Password	The OTP nonvolatile array used to store a 64-bit password used to enable changing the state of the PPB Lock Bit when using Password Mode Sector Protection.	Not supported
Dynamic Protection Bits (DYB)	The volatile array with one bit for each sector. When set, each bit protects the related sector from erasure and programming.	Dynamic Protection Bits (DPB)
Status or Peripheral Registers	The register that is used to hold the status of the Embedded Algorithm and read/write of other registers.	Status Register

To access each address space, the S26KL/S26KS HyperFlash family provides a methodology called “Address Space Overlay” (ASO). ASO requires explicit address space switching by issuing ASO entry/exit commands before/after accessing each address space except Flash Memory Array and Status or Peripheral Registers address space. Each ASO replaces (overlays) either the sector selected by the command that enters the ASO or the entire flash device address range, depending on the ASO entry command.

The MX25UM OctaFlash only uses the ASO methodology for its secured OTP address space.

2.1 Flash Memory Array

The S26KL/S26KS HyperFlash family has a uniform sector architecture with a sector size of 256 KB. A user configuration option is available to overlay the first sector or last sector with eight 4-KB Parameter Sectors. The existence and location of the Parameter Sectors can be changed by writing to Non-Volatile Configuration Register (NVCR) or Volatile Configuration Register (VCR).

The MX25UM OctaFlash family also has a uniform architecture with 4-KB sectors and 64-KB blocks, which each contain 16 consecutive sectors. Table 1 shows the sector architecture comparison of the MX25UM51245G OctaFlash and the S26KL512S/S26KS512S HyperFlash family.

Table 1. Sector Architecture Comparison of MX25UM51245G and S26KL512S/S26KS512S

Address Range	OctaFlash MX25UM		S26KL/S26KS		
	Sector	Block	xVCR[9.8] = 00	xVCR[9.8] = 01	xVCR[9.8] = 10
0000000h – 0000FFFh	0	0	Param-Sector 0	Sector 0	Sector 0
0001000h – 0001FFFh	1		Param-Sector 1		
0002000h – 0002FFFh	2		Param-Sector 2		
0003000h – 0003FFFh	3		Param-Sector 3		
0004000h – 0004FFFh	4		Param-Sector 4		
0005000h – 0005FFFh	5		Param-Sector 5		
0006000h – 0006FFFh	6		Param-Sector 6		

Address Range	OctaFlash MX25UM		S26KL/S26KS		
	Sector	Block	xVCR[9.8] = 00	xVCR[9.8] = 01	xVCR[9.8] = 10
0007000h – 0007FFFh	7		Param-Sector 7		
…	…				
000F000h – 000FFFFh	15				
0010000h – 0010FFFh	16				
…	…	1			
001F000h – 001FFFFh	31				
0020000h – 0020FFFh	32		Sector 0		
…	…	2			
002F000h – 002FFFFh	47				
0030000h – 0030FFFh	48				
…	…	3			
003F000h – 003FFFFh	63				
0040000h – 0040FFFh	64				
…	…	4			
004F000h – 004FFFFh	79				
0050000h – 0050FFFh	80				
…	…	5			
005F000h – 005FFFFh	95				
0060000h – 0060FFFh	96		Sector 1	Sector 1	Sector 1
…	…	6			
006F000h – 006FFFFh	111				
0070000h – 0070FFFh	112				
…	…	7			
007F000h – 007FFFFh	127				
…	…	…	…	…	…
3F80000h – 3F80FFFh	16256				
…	…	1016			
3F8F000h – 3F8FFFFh	16271				
3F90000h – 3F90FFFh	16272				
…	…	1017			
3F9F000h – 3F9FFFFh	16287				
3FA0000h – 3FA0FFFh	16288		Sector 254	Sector 254	Sector 254
…	…	1018			
3FAF000h – 3FAFFFFh	16303				
3FB0000h – 3FB0FFFh	16304				
…	…	1019			
3FBF000h – 3FBFFFFh	16319				

Address Range	OctaFlash MX25UM		S26KL/S26KS		
	Sector	Block	xVCR[9.8] = 00	xVCR[9.8] = 01	xVCR[9.8] = 10
3FC0000h – 3FC0FFFh	16320	1020	Sector 255	Sector 255	Sector 255
…	…				
3FCF000h – 3FCFFFFh	16335				
3FD0000h – 3FD0FFFh	16336	1021			
…	…				
3FDF000h – 3FDFFFFh	16351				
3FE0000h – 3FE0FFFh	16352	1022			
…	…				
3FEF000h – 3FEFFFFh	16367				
3FF0000h – 3FF0FFFh	16368	1023			
…	…				
3FF8000h – 3FF8FFFh	16366			Param-Sector 0	
3FF9000h – 3FF9FFFh	16377			Param-Sector 1	
3FFA000h – 3FFAFFFh	16378			Param-Sector 2	
3FFB000h – 3FFBFFFh	16379			Param-Sector 3	
3FFC000h – 3FFCFFFh	16380			Param-Sector 4	
3FFD000h – 3FFDFFFh	16381			Param-Sector 5	
3FFE000h – 3FFEFFFh	16382			Param-Sector 6	
3FFF000h – 3FFFFFFh	16383			Param-Sector 7	

2.2 Device ID and CFI (ID-CFI)

The S26KL/S26KS HyperFlash family has two methods to identify the type of flash memory: Device Identification (ID) and Common Flash Interface (CFI).

The Device Identification (ID), traditionally referred to as Autoselect, contains the JEDEC manufacturer ID, device ID, and some configuration and protection status information from the flash memory. The host system can use the ID to select the appropriate driver software for the specific flash device.

The Common Flash Interface (CFI) contains an extendable table of standard information describing the organization and operation of the flash memory. This permits the use of a general driver software that can accommodate multiple memory devices. The driver software adjusts the driver behavior based on the information in the CFI table.

The ID and CFI command sequences and command codes are different (see the Command Codes in Table 5 on page 10), but they are combined into a single address space and appear in a single overlay. Accessing either the ID or the CFI will display the combined ID-CFI address map. The ID-CFI address map appears within, and overlays the Flash Memory Array data of the sector selected by the address used in the ID-CFI enter command. While the ID-CFI ASO is entered, the content of all other sectors is undefined.

The MX25UM OctaFlash has a Serial Flash Discoverable Parameter (SFDP), a set of parameter tables that contain device characteristics that are used for identification. The SFDP can be adjusted by the system software to accommodate multiple memory devices, similar to the S26KL/S26KS HyperFlash CFI.

Table 2 on page 5 lists the ID address map for the S26KL/S26KS HyperFlash Family. For details of the ID and CFI field definitions, see the datasheets.

Table 2. ID Address Map of S26KL/S26KS HyperFlash Family

Word Address	Data	Description
(SA[2]) + 0000h	0001h	Manufacture ID
(SA) + 0001h	007Eh	Device ID
(SA) + 0002h to 000Bh	Reserved	RFU
(SA) + 000Ch	0005h	Lower Software Bits
(SA) + 000Dh	Reserved	Upper Software Bits
(SA) + 000Eh	0070h = 512 Mb @ 1.8 V 006Fh = 512 Mb @ 3.0 V 0072h = 256 Mb @ 1.8 V 0071h = 256 Mb @ 3.0 V 0074h = 128 Mb @ 1.8 V 0073h = 128 Mb @ 3.0 V	Device ID
(SA) + 000Fh	0000h	Device ID

3 Data Protection

3.1 Secure Silicon Region (SSR)

The Cypress S26KL/S26KS HyperFlash family and the Macronix MX25UM OctaFlash family both have a 1024-byte one-time-programmable (OTP) address space, referred to as the “Secure Silicon Region (SSR)” by Cypress HyperFlash and the “Secured OTP” by Macronix OctaFlash. This memory space is used to provide additional system security by holding a unique device serial number that can be set by the factory or system user. The HyperFlash SSR provides a larger user-programmable address space than the OctaFlash Secured OTP as well as individually lockable regions.

3.1.1 OctaFlash SSR

The OctaFlash secured OTP region’s lowest 512 address bytes are available for the user to program ; the highest 512 address bytes are Macronix factory-programmed. The OTP region is programmed or read by first entering the secured OTP mode with the Enter Security OTP command. Normal procedures are used for programming or reading, and then the secured OTP mode is exited with the Exit Security OTP command (see Table 11 on page 16 for a list of commands). The user-programmable secured OTP address space is locked by writing the WRSCUR (write security register) command to set the user lock-down bit1 as “1”. The factory-programmable secured OTP address space is locked in the factory in the security register bit0. Once the OTP is locked by the factory or user, the corresponding address range cannot be reprogrammed.

Table 3. OctaFlash Secured OTP Address Map

Address Range	Contents
xxx000 - xxx1FF	Available for User Programming
xxx200 - xxx3FF	Programmed by Macronix

[2] *SA = Address of the sector selected or being overlaid.*

3.1.2 HyperFlash SSR

The HyperFlash 1024-byte SSR is divided into 32 individually lockable, 32-byte aligned and length regions. The lowest 16 address bytes are Cypress factory-programmed. The next four higher bytes are SSR Lock Bytes, where each bit in an SSR Lock Byte corresponds to an SSR region. The user can program the SSR Lock Bytes to lock the corresponding SSR regions individually to prevent further programming (see the datasheet for more details). The next higher 12 bytes of the lowest address region are Reserved for Future Use (RFU). These bits can be programmed by the user, but future Cypress devices may use these as SSR Lock bits to protect a larger SSR space. The remaining regions are available for the user to program additional permanent data. The SSR region is programmed or read by entering the SSR ASO with the SSR Entry command, programming or reading through the normal procedures, and then exiting with the SSR Exit command (see Table 11 on page 16). The SSR Freeze (xVCR10) configuration register bit can be set to “0” to protect the entire SSR memory by preventing further programming. The SSR Freeze command provides the same functionality as the OctaFlash WRSCUR command.

Table 4. HyperFlash Secured Silicon Region (SSR) Address Map

Region	Byte Address Range (Hex)	Contents	Initial Delivery State
Region 0	0	Least Significant Byte of Cypress-Programmed Random Number	Cypress-Programmed Random Number
	…	…	
	000F	Most Significant Byte of Cypress-Programmed Random Number	
	0010-0013	Region Locking Bits Byte 10 [bit 0] locks region 0 from programming when = 0 … Byte 13 [bit 7] locks region 31 from programming when = 0	All Bytes = FF
	0014 - 001F	Reserved for Future Use (RFU)	All Bytes = FF
Region 1	0020 - 003F	Available for User Programming	All Bytes = FF
Region 2	0040 - 005F	Available for User Programming	All Bytes = FF
…	…	Available for User Programming	All Bytes = FF
Region 31	03E0 - 003FF	Available for User Programming	All Bytes = FF

3.2 Block Lock Protection

The MX25UM OctaFlash supports the Block Lock Protection feature that allows the user to protect memory areas by writing BP0-BP3 bits in the Status Register. The S26KL/S26KS HyperFlash family does not support the Block Lock Protection; use the Advanced Sector Protection features instead.

3.3 Advanced Sector Protection (ASP)

The S26KL/S26KS HyperFlash family supports the Advanced Sector Protection (ASP) feature that allows sectors to be individually protected by the corresponding volatile protection bits (DYB bits) or nonvolatile protection bits (PPB bits). The HyperFlash DYB and PPB bits are assigned to each sector throughout the entire memory; when either a DYB or PPB bit is 0, the corresponding sector is protected from program and erase operations.

The MX25UM OctaFlash supports a similar protection feature that is compatible with ASP (DPB as volatile protection bits and SPB as nonvolatile protection bits). The MX25UM OctaFlash DPB bits are also assigned to each sector, but the SPB bits are assigned to each sector in only the bottom and top 64 KB of the memory and to each 64-KB block in the remaining memory. The sector or block is protected when either of the DPB or SPB bits is 1. The MX25UM OctaFlash also supports the Gang Lock/Unlock feature that can protect/unprotect the whole Flash Memory Array.

HyperFlash has a PPB Lock Bit to protect the PPB bits, which provides the same functionality as the OctaFlash SPB Lock Down Bit (SPBLKDN). The OctaFlash SPBLKDN bit is in the OTP Lock Register, so once it is locked as 0, all SPB bits are permanently locked from program and erase operations. The HyperFlash PPB Lock Bit is not in an OTP region, so has greater flexibility and added features. The PPB Lock Bit can be managed by Persistent Protection or Password Protection:

- **Persistent Protection** sets the PPB Lock Bit to 1 during POR or Hardware Reset to unprotect the PPB bits. A command can clear the PPB lock bit to 0 to protect the PPB bits. There is no Persistent Protection command to set the PPB Lock Bit back to 1, so it will stay at 0 until the next Power-Off or Hardware Reset.
- **Password Protection** clears the PPB Lock Bit to 0 during POR or Hardware Reset, locking the PPB bits. A 64-bit password can be permanently programmed and hidden. A command can be used to provide a password for comparison with the hidden password. If the passwords match, the PPB Lock bit is set to 1 to unprotect the PPB bits. A command can be used to clear the PPB Lock Bit to 0.

The selection of Persistent Protection or Password Protection is made in the OTP ASP Configuration Register, so is a permanent selection. The features and register set of the S26KL/KS HyperFlash ASP can be read by the Sector Address (SA) Protection Status Read command. The returned data from SA Protection Status Read command indicates whether the target sector is protected in bits 0 to 3.

- **Bit 0:** Indicates whether the sector is protected (0 = protected, 1 = unprotected)
- **Bit 1:** Protected using the sector's DYB bit (0 = protected, 1 = unprotected)
- **Bit 2:** Protected using the sector's PPB bit (0 = protected, 1 = unprotected)

4 Read Flash Memory Array

The Flash Memory Array is the primary and default address space that is selected during Power-On, after a Hardware Reset, or after a Command Reset. The typical HyperBus controller integrated in the host system maps the HyperFlash memory array within the system memory area. Reading from the address where the HyperFlash is mapped returns data from the HyperFlash. In general, the software doesn't need to consider the HyperBus signal protocol, but the HyperBus controller must be set to either a wrapped or linear burst type for every read transaction. The length of a wrapped burst can be configured via NVCR or VCR. AN99195 describes burst configuration and read performance optimization.

The MX25UM OctaFlash family has different Read commands based on the bus width and addressing mode. It also has the Set Burst Length command that allows configuring both burst type and length. See Table 6 on page 11 and Table 9 on page 14 for the command comparison.

5 Program Flash Memory Array

The S26KL/S26KS HyperFlash family supports two methods of programming: Word or Write Buffer Programming. Write Buffer Programming allows up to a buffer size of 512 B to be programmed in one operation. Word programming is used to program a single word to the Flash Memory Array. Use of Write Buffer Programming is recommended because it is more efficient and faster than Word Programming.

The MX25UM OctaFlash family is programmed on a 256-B-page basis with the Page Program operation, similar to the S26KL/S26KS HyperFlash Write Buffer Programming.

Code 1 shows an example C code for initiating Write Buffer Programming. See Table 9 for command comparison.

Code 1. Write Buffer Programming Example

```
UINT16 *src = source_of_data;              /* address of source data */
UINT16 *dst = destination_of_data;         /* flash destination address */
UINT16 wc = words_to_program -1;           /* word count (minus 1) */
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)sector_address ) = 0x0025;    /* write buffer load command */
*( (UINT16 *)sector_address ) = wc;        /* write word count (minus 1) */
for (i=0;i<=wc;i++)
{
       *dst++ = *src++;
}
       *( (UINT16 *)sector_address ) = 0x0029;    /* write confirm command */
```

6 Erase Flash Memory Array

The S26KL/S26KS HyperFlash family supports Sector Erase on 256-KB sectors and Chip Erase, while the MX25UM OctaFlash memory supports Sector Erase on 4-KB sectors, Block Erase on 64-KB blocks, and Chip Erase. HyperFlash does not have a dedicated command for erasing 4-KB Parameter Sectors; the Sector Erase command sequence can be used to target the appropriate Parameter Sector addresses.

Code 2 shows an example C code for initiating HyperFlash Sector Erase. See Table 10 on page 15 for command comparison.

Code 2. Sector Erase Example

```
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)base_addr + 0x555 ) = 0x0080; /* write setup command */
*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write additional unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write additional unlock cycle 2 */
*( (UINT16 *)sector_address ) = 0x0030;    /* write sector erase command */
```

6.1 Blank Check

The S26KL/S26KS HyperFlash family supports a Blank Check command that can be used to confirm whether the selected Flash Memory Array sector is fully erased. No similar command is supported in the MX25UM OctaFlash family. The Blank Check command can replace the traditional procedure of reading each Flash Memory Array bit to verify that they are all 1s.

See Table 10 on page 15 for command comparison.

6.2 Evaluate Erase Status

The S26KL/S26KS HyperFlash family supports the Evaluate Erase Status (EES) command that can be used to detect erase operations that failed due to loss of power, reset, or failure during an erase operation. No similar command is supported in the MX25UM OctaFlash family.

See Table 10 on page 15 for command comparison.

7 Status Register

The S26KL/S26KS HyperFlash family has a single, read-only 16-bit Status Register (SR), while the MX25UM OctaFlash family has a Status Register and a Security Register. See the corresponding datasheet sections for all register bit assignments and detailed descriptions of the bits. The HyperFlash Status Register and the OctaFlash Security Registers both contain bits dedicated to Program Suspend, Program Status, Erase Suspend, and Erase Status.

The HyperFlash Status Register has the following additional dedicated bits:

Dedicated Bit	Function	OctaFlash Equivalent
Sector Erase Status	Indicates whether the most recent sector erase command was successful.	Not supported
Sector Locked Status	Indicates whether a sector is locked by the lock bits in the Advanced Sector Protection region.	Not supported
Write Buffer Abort	Indicates an error in the Write Buffer Program command sequence.	Not supported
Device Ready	Indicates whether the device is busy with an Embedded Algorithm.	Write in Progress bit in the Status Register

The OctaFlash Security Register and Status Register have the following additional dedicated bits:

Dedicated Bit	Function	HyperFlash Equivalent
Write Protection Selection	Indicates whether the device is under Block Lock mode or Advanced Sector Protection mode.	Not supported; use the Advanced Sector Protection mode instead
OTP Indicator	Indicates whether the factory-programmed ID address space in the OTP region has been programmed.	Uses a random, factory-programmed ID number programmed into the lowest 16 address bytes
Lock-Down Secured OTP	Locks the entire Secured OTP region once this bit is programmed.	Not supported; use the SSR Freeze bit located in the configuration register instead
Write in Progress bit	Indicates whether the device is busy with a write command.	Not supported; use the Device Ready bit instead
Write Enable Latch bit	Must be set before any instruction which changes the device content.	Not required
Block Protect bits	For Block Protection mode.	Not supported; use the Advanced Sector Protection mode instead

See Table 5 on page 10 for command comparison.

8 Software Reset

The S26KL/S26KS HyperFlash Software Reset command can be used to exit any ASO and clear any error bits in the Status Register (SR). Software Reset commands are ignored during programming or erase operations. This differs from the OctaFlash Software Reset command, which will still execute during program or erase operations and can cause data loss.

See Table 14 on page 19 for command comparison.

9 Deep Power-Down

The S26KL/S26KS HyperFlash family supports Deep Power-Down (DPD). In the DPD mode, current consumption is driven to the lowest level. DPD is entered using the DPD Entry command sequence. Exiting the DPD mode is accomplished with the assertion of CS# during any read or write transaction or Hardware Reset. There is no dedicated command to exit the DPD.

The MX25UM OctaFlash family also supports Deep Power-down (DP) and a command for entering DP. Exiting the DP is accomplished by issuing a Release from Deep Power-down (RDP), Read Electronic Signature (RES), or Software Reset command.

See Table 5 on Page 11 for command comparison.

10 Command Summary

Tables 5 to 12 compare the command sets of S26KL/S26KS HyperFlash and MX25UM OctaFlash. MX25UM can be operated in Serial Peripheral Interface (SPI) mode or Octa Peripheral Interface (OPI) mode; the command sets for both interface modes are shown.

Table 5. Command Set Map (ID/CFI, Status Register, and Deep Power-Down)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Read ID/CFI					
ID (Autoselect) Entry	555	AA	Read SFDP Mode	RDSFDP (5A A5)	RDSFDP (5A)
	2AA	55			
	(SA[3])555	90			
CFI Enter	(SA)55	98			
ID-CFI Read	(SA)RA[4]	RD[5]			
Reset / ASO Exit	XXX[6]	F0 or FF			
-	-	-	Read Identification	RDID (9F 60)	RDID (9F)
Status Register Access					
Status Register Read	555	70	Status Register Read	RDSR (05 FA)	RDSR (05)
	XXX	RD	Security Register Read	RDSCUR (2B D4)	RDSCUR (2B)
Status Register Clear	555	71	-	-	-
-	-	-	Status Register Write	WRSR (01 FE)[7]	WRSR (01)
-	-	-	Security Register Write	WRSCUR (2F D0)	WRSCUR (2F)
Deep Power-Down					
Enter Deep Power-Down	555	AA	Deep Power-down	DP (B9 46)	DP (B9)
	2AA	55			
	XXX	B9			
-	-	-	Release from Deep Power-down	RDP (AB 54)	RDP (AB)

[3] SA = Address of the sector selected or being overlaid.

[4] *RA = Address of the memory to be read*

[5] *RD = Data read from address*

[6] *X = Don't care.*

[7] *WRSR and WRCR (OPI) have the same 2-byte command IDs but the last address cycle is different*

Table 6. Command Set Map (Configuration Register)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Configuration Register Access					
Load Volatile Configuration Register	555	AA	-	-	-
	2AA	55			
	555	38			
	XXX[8]	VCR[9]			
Read Volatile Configuration Register	555	AA	-	-	-
	2AA	55			
	555	C7			
	XXX	RD[10] VCR			
Program Nonvolatile Configuration Register	555	AA	Write Configuration Register Write Configuration Register 2 Set Burst Length	WRCR (01 FE)[11] WRCR2 (72 8D) SBL (C0 3F)	WRSR (01) WRCR2 (72) SBL (C0)
	2AA	55			
	555	39			
	XXX	NVCR[12]			
Erase Nonvolatile Configuration Register	555	AA	-	-	-
	2AA	55			
	555	C8			
Read Nonvolatile Configuration Register	555	AA	Read Configuration Register Read Configuration Register 2	RDCR (15 EA) RDCR2 (71 8E)	RDCR (15) RDCR2 (71)
	2AA	55			
	555	C6			
	XXX	RD NVCR			

[8] *X = Don't care*

[9] *VCR = Volatile Configuration Register*

[10] *RD = Data read from address*

[11] *WRSR and WRCR (OPI) have the same 2-byte command IDs but the last address cycle is different*

[12] *NVCR = Non-Volatile Configuration Register*

Table 7. Command Set Map (Miscellaneous Register Access)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Miscellaneous Register Access					
Program Power-On Reset Timer Register	555	AA	-	-	-
	2AA	55			
	555	34			
Read Power-On Reset Timer	555	AA	-	-	-
	2AA	55			
	555	3C			
	XXX[13]	RD[14]			
Load Interrupt Configuration Register	555	AA	-	-	-
	2AA	55			
	555	36			
	XXX	ICR[15]			
Read Interrupt Configuration Register	555	AA	-	-	-
	2AA	55			
	555	C4			
	XXX	RD			
Load Interrupt Status Register	555	AA	-	-	-
	2AA	55			
	555	37			
	XXX	ISR[16]			
Read Interrupt Status Register	555	AA	-	-	-
	2AA	55			
	555	C5			
	XXX[17]	RD[18]			

[13] *X = Don't care*

[14] *RD = Data read from address*

[15] *ICR = Interrupt Configuration Register*

[16] *ISR = Interrupt Status Register*

[17] *X = Don't care*

[18] *RD = Data read from address*

Table 8. Command Set Map (Miscellaneous Register Access)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Miscellaneous Register Access (Continued)					
-	-	-	Write Disable	WRDI (04 FB)	WRDI (04)
-	-	-	Write Enable	WREN (06 F9)	WREN (06)
-	-	-	Read Fast Boot Register	RDFBR (16 E9)	RDFBR (16)
-	-	-	Write Fast Boot Register	WRFBR (17 E8)	WRFBR (17)
-	-	-	Erase Fast Boot Register	ESFBR (18 E7)	ESFBR (18)
-	-	-	Write Protect Selection	WPSEL (68 97)	WPSEL (68)

Table 9. Command Set Map (Read and Program Flash Memory Array)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Read Flash Memory Array					
Read	RA[19]	RD[20]	Read	8READ (EC 13) DTRD (EE 11)	READ3B (03) READ4B (13)
			Fast Read	-	FAST_READ3B (0B) FAST_READ4B (0C)
Program Flash Memory Array					
Word Program	555	AA	-	-	-
	2AA	55			
	555	A0			
	PA[21]	PD[22]			
Write Buffer Program	555	AA	Page Program	PP (12 ED)	PP3B (02) PP4B (12)
	2AA	55			
	SA[23]	25			
	SA	WC[24]			
	WBLx[25]	PDx[26]			
	SA	29			
Write-to-Buffer-Abort Reset	555	AA	-	-	-
	2AA	55			
	555	F0			
Program Suspend	XXX[27]	51	Program Suspend	PGM Suspend (B0 4F)	PGM Suspend (B0)
Program Resume	XXX	50	Program Resume	PGM Resume (30 CF)	PGM Resume (30)

[19] *RA = Address of the memory to be read*

[20] *RD = Data read from address*

[21] *PA = Address of the memory location to be programmed*

[22] *PD = Data to be programmed*

[23] *SA = Address of the sector selected or being overlaid*

[24] *WC = Word Count is the number of words to be loaded into write buffer minus 1*

[25] *WBLx = The address of the data to be programmed. The address must be within a same 512-byte write buffer.*

[26] *PDx = Data to be programmed at address WBLx*

[27] *X = Don't care*

Table 10. Command Set Map (Erase Flash Memory Array)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Erase Flash Memory Array					
Chip Erase	555	AA	Chip Erase	CE (60 C7 or 9F 38)	CE (60 or C7)
	2AA	55			
	555	80			
	555	AA			
	2AA	55			
	555	10			
Sector Erase	555	AA	Sector Erase Block Erase	SE (21 DE) BE (DC 23)	SE3B (20) SE4B (21) BE3B (D8) BE4B (DC)
	2AA	55			
	555	80			
	555	AA			
	2AA	55			
	SA[28]	30			
Erase Suspend	XXX[29]	B0	Erase Suspend	ERS Suspend (B0 4F)	ERS Suspend (B0)
Erase Resume	XXX	30	Erase Resume	ERS Resume (30 CF)	ERS Resume (30)
Blank Check	(SA)555	33	-	-	-
Evaluate Erase Status	(SA)555	D0	-	-	-

[28] *SA = Address of the sector selected or being overlaid.*

[29] *X = Don't care.*

Table 11. Command Set Map (Secure Silicon Region)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
Secure Silicon Region					
SSR Entry	555	AA	OTP Entry	ENSO (B1 4E)	ENSO (B1)
	2AA	55			
	(SA[30])555	88			
Read	RA[31]	(SA)RD[32]	Read	8READ (EC 13) DTRD (EE 11)	READ3B (03) READ4B (13)
			Fast Read	-	FAST_READ3B (0B) FAST_READ4B (0C)
Word Program	555	AA	-	-	-
	2AA	55			
	555	A0			
	PA[33]	PD[34]			
Write Buffer Program	555	AA	Page Program	PP (12 ED)	PP3B (02) PP4B (12)
	2AA	55			
	SA	25			
	SA	WC[35]			
	WBLx[36]	PDx[37]			
	SA	29			
Write-to-Buffer-Abort Reset	555	AA	-	-	-
	2AA	55			
	555	F0			
SSR Exit	555	AA	OTP Exit	EXSO (C1 3E)	EXSO (C1)
	2AA	55			
	555	90			
	XXX[38]	00			
Reset / ASO Exit	XXX	F0	-	-	-

[30] *SA = Address of the sector selected or being overlaid.*

[31] *RA = Address of the memory to be read*

[32] *RD = Data read from address*

[33] *PA = Address of the memory location to be programmed*

[34] *PD = Data to be programmed*

[35] *WC = Word Count is the number of words to be loaded into write buffer minus 1*

[36] *WBLx = The address of the data to be programmed. The address must be within a same 512-byte write buffer.*

[37] *PDx = Data to be programmed at address WBLx*

[38] *X = Don't care.*

Table 12. Command Set Map (ASP Configuration Register Access and Password)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
ASP Configuration Register Access					
ASP Register Entry	555	AA	-	-	-
	2AA	55			
	555	40			
Program	XXX[39]	A0	Write Protect Selection	WPSEL (68 97)	WPSEL (68)
	XXX	PD[40]			
ASPR Read	0	RD[41]	-	-	-
ASPR ASO Exit	XXX	90	-	-	-
	XXX	0			
Reset / ASO Exit	XXX	F0	-	-	-
Password					
Password ASO Entry	555	AA	-	-	-
	2AA	55			
	555	60			
Program	XXX	A0	-	-	-
	PWAx[42]	PWDx[43]			
Read	PWAx	PWDx	-	-	-
Unlock	0	25	-	-	-
	0	3			
	PWAx	PWDx			
	0	29			
Command Set Exit	XXX	90	-	-	-
	XXX	0			
Reset / ASO Exit	XXX	F0	-	-	-

[39] *X = Don't care.*

[40] *PD = Data to be programmed.*

[41] *RD = Data read from address*

[42] *PWAx = Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h*

[43] *PWDx = Password data word0, word1, word2, and word3*

Table 13. Command Set Map (PPB and PPB Lock)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
PPB					
PPB Entry	555	AA	-	-	-
	2AA	55			
	555	C0			
PPB Program	XXX[44]	A0	SPB Program	WRSPB (E3 1C)	WRSPB (E3)
	SA[45]	0			
All PPB Erase	XXX	80	All SPB Erase	ESSPB (E4 1B)	ESSPB (E4)
	0	30			
PPB Read	SA	RD[46]	SPB Read	RDSPB (E2 1D)	RDSPB (E2)
SA Protection Status	XXX	60	-	-	-
	SA	RD			
Command Set Exit	XXX	90	-	-	-
	XXX	0			
Reset / ASO Exit	XXX	F0	-	-	-
PPB Lock					
PPB Lock Entry	555	AA	-	-	-
	2AA	55			
	555	50			
PPB Lock Bit Clear	XXX	A0	-	-	-
	XXX	0			
PPB Lock Status	XXX	RD	Lock Register Read	RDLR (2D D2)	RDLR (2D)
-	-	-	Lock Register Write	WRLR (2C D3)	WRLR (2C)
Command Set Exit	XXX	90	-	-	-
	XXX	0			
Reset / ASO Exit	XXX	F0	-	-	-

[44] *X = Don't care*

[45] *SA = Address of the sector selected or being overlaid.*

[46] *RD = Data read from address*

Table 14. Command Set Map (DYB and Reset)

S26KL/S26KS			MX25UM		
Command Description	**Addr**	**Data**	**Command Description**	**OPI Mode Command Name (Code)**	**SPI Mode Command Name (Code)**
DYB					
DYB ASO Entry	555	AA	-	-	-
	2AA	55			
	555	E0			
DYB Set	XXX[47]	A0	DPB Write	WRDPB (E1 1E)	WRDPB (E1)
	SA[48]	0			
DYB Clear	XXX	A0	-	-	-
	SA	1			
DYB Status Read	SA	RD[49]	DPB Read	RDDPB (E0 1F)	RDDPB (E0)
SA Protection Status	XXX	60	-	-	-
	SA	RD			
Command Set Exit	XXX	90	-	-	-
	XXX	0			
Reset / ASO Exit	XXX	F0	-	-	-
	-	-	Gang Block Lock	GBLK (7E 81)	GBLK (7E)
			Gang Block Unlock	GBULK (98 67)	GBULK (98)
Reset					
Reset / ASO Exit	XXX	F0	-	-	-
-	-	-	No Operation	NOP (00 FF)	NOP (00)
-	-	-	Reset Enable	RSTN (66 99)	RSTN (66)
-	-	-	Reset Memory	RST (99 66)	RST (99)

11 Summary

The Cypress S26KL/S26KS HyperFlash family adopts the command set of traditional Parallel NOR (PNOR) Flash Memory devices such as the Cypress S29GL-S family. The typical HyperBus controller integrated in the host system translates the software accesses to the HyperBus signal protocol. Therefore, the S26KL/S26KS HyperFlash family is fully compatible with PNOR Flash Memory devices in terms of software. Although the command set is completely different, the S26KL/S26KS HyperFlash family has similar functions to the Macronix MX25UM OctaFlash Family. Users can transition from the Macronix MX25UM OctaFlash to the S26KL/S26KS HyperFlash with these software migration guidelines.

[47] *X = Don't care*

[48] *SA = Address of the sector selected or being overlaid.*

[49] *RD = Data read from address*

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**	5186789	TKUW	03/24/2016	New application note.
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