AN203277

FM 32-Bit Microcontroller Family Hardware Design Considerations

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Associated Part Family: All FM0+, FM3 and FM4 parts

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AN203277 reviews several topics for designing a hardware system with FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal and other pin connections, and programming and debugging interfaces.

Contents

1 Introduction

The FM0+, FM3, and FM4 families of MCUs provide power and flexibility for complex applications, beyond what traditional MCUs offer. However, this power and flexibility raises new considerations when designing an FM device into a printed circuit board (PCB) design.

These considerations include proper connections for device power, reset, crystal, programming, and other pins.

Good board layout techniques are also important, especially for precision analog applications.

This application note provides information on each of these topics so that you can successfully design FM devices into your PCB and hardware environment.

This application note is for hardware design engineers and PCB layout engineers who have some previous experience with 32-bit MCU circuit board design, but may not have direct knowledge of the FM family design requirements.

It is assumed that the reader has a basic understanding of PCB layout tools and how to use them to implement the design suggestions given here.

This document does not go into specific PCB design tools or how tool design rules are configured.

2 Package Selection

One of the first decisions you must make for your design is which package to use. Several considerations drive this decision, including number of I/O pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses.

The FM device families have a very large selection of devices to help match your exact needs in any situation with an efficient and cost-effective solution. Packaging solutions range from the ultra-small Wafer Scale Packages to high pin count Ball Grid Array packages. Easier to layout on lower layer counts and lower cost PCBs are the Leaded Quad Flat Pack (LQFP). LQFP packaging options range from 48 pin devices to 216 pin devices.

Following are some package selection criteria:

LQFP

- Easier to route signals due to large pitch and the open area below the part
- Less mechanical rigidity for more protection against vibration and mechanical stress
- Disadvantages are larger package and lower thermal conduction (θ_{JA}).

48-QFN and 64-QFN

- QFN packages are smaller
- Better thermal conduction due to center thermal pad
- Disadvantages are:
  - More difficult to route signals due to the center pad
  - Possibility of mechanical stress on the device inducing electrical / mechanical performance changes. Center pad solder paste and solder mask must be designed taking these factors into account.

For more information, see AN72845, Design Guidelines for QFN Packaged Devices.

BGA and PBGA

- Small-scale packages offering high pin counts in larger lead pitches, which significantly reduce the manufacturing complexities for high I/O devices. BGA packages are used in applications requiring:
- Faster circuitry speed because the terminations are much shorter and therefore less inductive and resistive
- Better heat dissipation
- Conventional surface mount technology (SMT) production technologies such as stencil printing and component mounting can be used
- Robust reflow processing, due to higher pitch (1.27 mm, 0.050”, typical), better lead rigidity, and self-alignment characteristics. Self-alignment during reflow is very beneficial and opens the process window considerably.
- Disadvantage: X-ray needed for solder joint inspection

CSP and WLCSP

- Are true die-scale packages and offer the smallest footprint for each I/O pin count of any standard package. They are used in applications with:
  - Very small PCB size
  - Flexible printed circuits (FPC)
- However, the manufacturing process is more complex and requires specialized knowledge. For more information see:
  - AN69061, Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages.
  - AN89611, PSoC 3 and PSoC 5LP Getting Started with Chip Scale Packages

3 Power System

The FM power system is based on separate supplies and returns for analog, digital, backup, USB, and Ethernet, as Table 1 shows.

Table 1. Power Domains

Power Domain	Associated Power and Return Pins
Analog	AV_{CC}, AV_{RH}, AV_{RL}, AV_{SS}
Digital	V_{CC} , V_{SS}
Backup Battery	V_{BAT}, V_{SS}
USB	$USBV_{CC}$, V_{SS}
Ethernet	$ETHV_{CC}$, V_{SS}

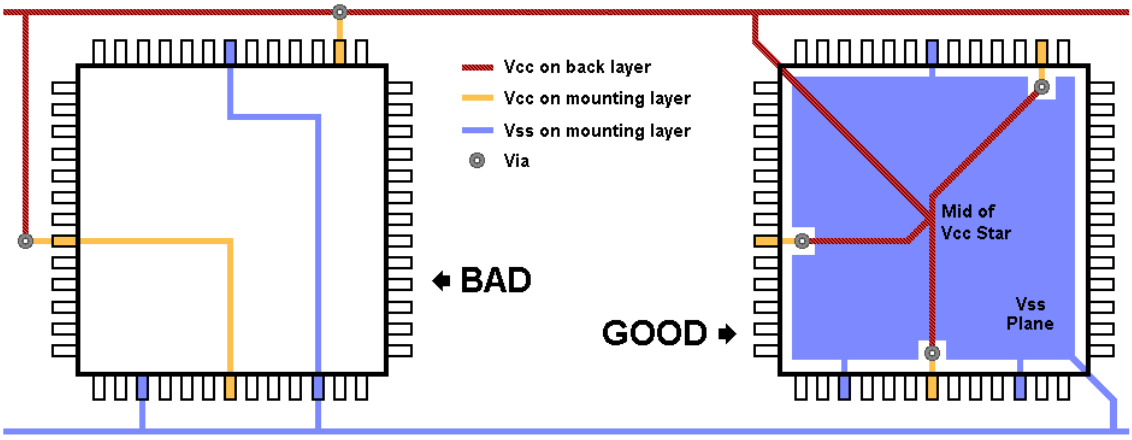
3.1 Digital Power Connections

The power supply must be from 2.7 V to 5.5 V for normal usage, depending on the selected FM series. Refer to the datasheet for maximum and minimum power supply voltages. For USB functionality, provide 3.3 V to $USBV_{CC}$.

If the USB data pins (USDMn, USDPn) are used only as digital I/O ports. $USBV_{CC}$ must be connected to V_{CC}, Failure to connect $USBV_{CC}$ to V_{CC} causes the GPIO function of the USB pins to operate incorrectly.

Note that if V_{CC} is routed to several pins; these pins must be connected together on the PCB. The PCB trace between the V_{CC} pins should be as short as possible; ideally, it should be run underneath the device directly between the pins. For QFN packages with center pads, the trace can be run through vias to another PCB layer. Figure 1 shows this.

Figure 1. PCB Trace Between VCC Pins



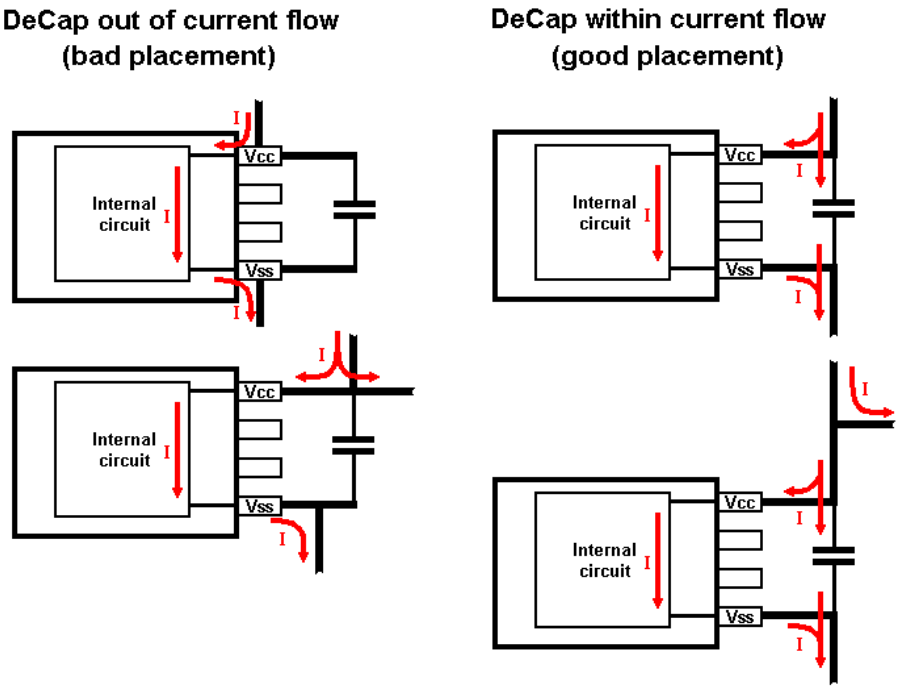
Cypress FM MCU and PSoC development kit schematics and board Gerber files provide good examples of how to incorporate FM MCUs into board schematics. For more information, see Related Documents.

To reduce power supply noise throughout the device, each V_{CC} pin should be connected to a ceramic decoupling capacitor. The PCB trace between the pin and the capacitor should be as short and wide as possible – for more information see Appendix A. One or more 10-µF bulk decoupling capacitors should also be placed on each board assembly.

Note: It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias is a significant percentage of the rated working voltage.

Decoupling capacitors (DeCaps) for power supply must be placed within the “current flow”. Otherwise, inductance and resistive effects negate having the capacitors. Figure 2 shows this.

Figure 2. Examples of DeCap Placement



If possible, all decoupling capacitors should be placed on the same mounting side as the MCU. Cypress recommends 10 nF (~100 MHz resonance) to 100 nF (~10 MHz resonance) depending on the application.

Figure 3 shows the recommended routing and placement for single-sided metal layer. (Note that in all following illustrations, the mounting metal layer is drawn in black and the back side metal layer in gray).

Figure 3. Routing and Placement for Single-Sided Metal Layer

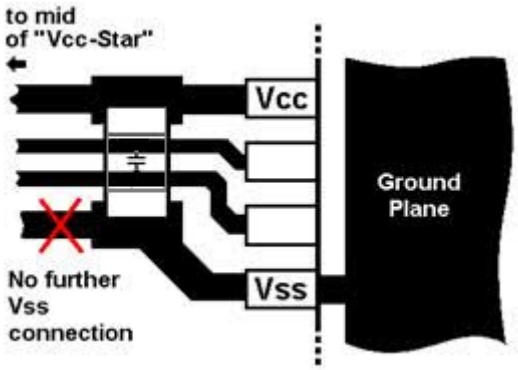


Figure 4 shows the recommended routing and placement for double-sided metal layers. Note that despite the capacitor being placed on the opposite side from the MCU, this solution is preferred over other solutions as the via to the ground plane and the via connecting to the V_{CC} pin minimize inductance.

Figure 4. Routing and Placement for Double-Sided Metal Layer

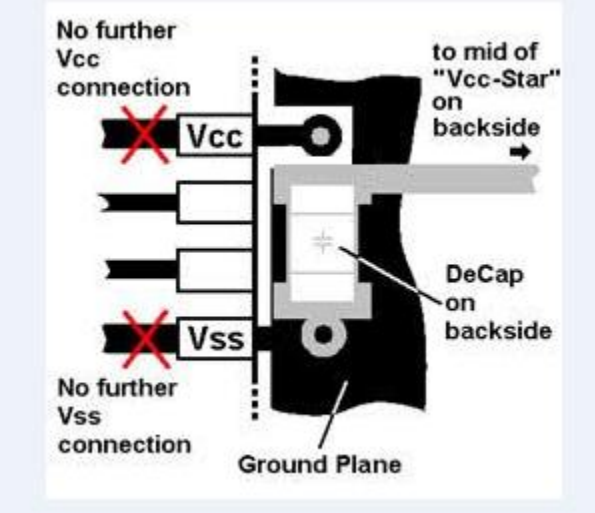
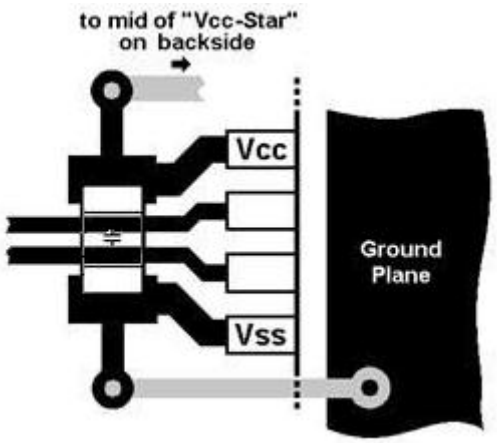


Figure 5 shows the recommended placement and routing if mounting on both sides is not possible.

Figure 5. Placement and Routing if Mounting on Only One Side



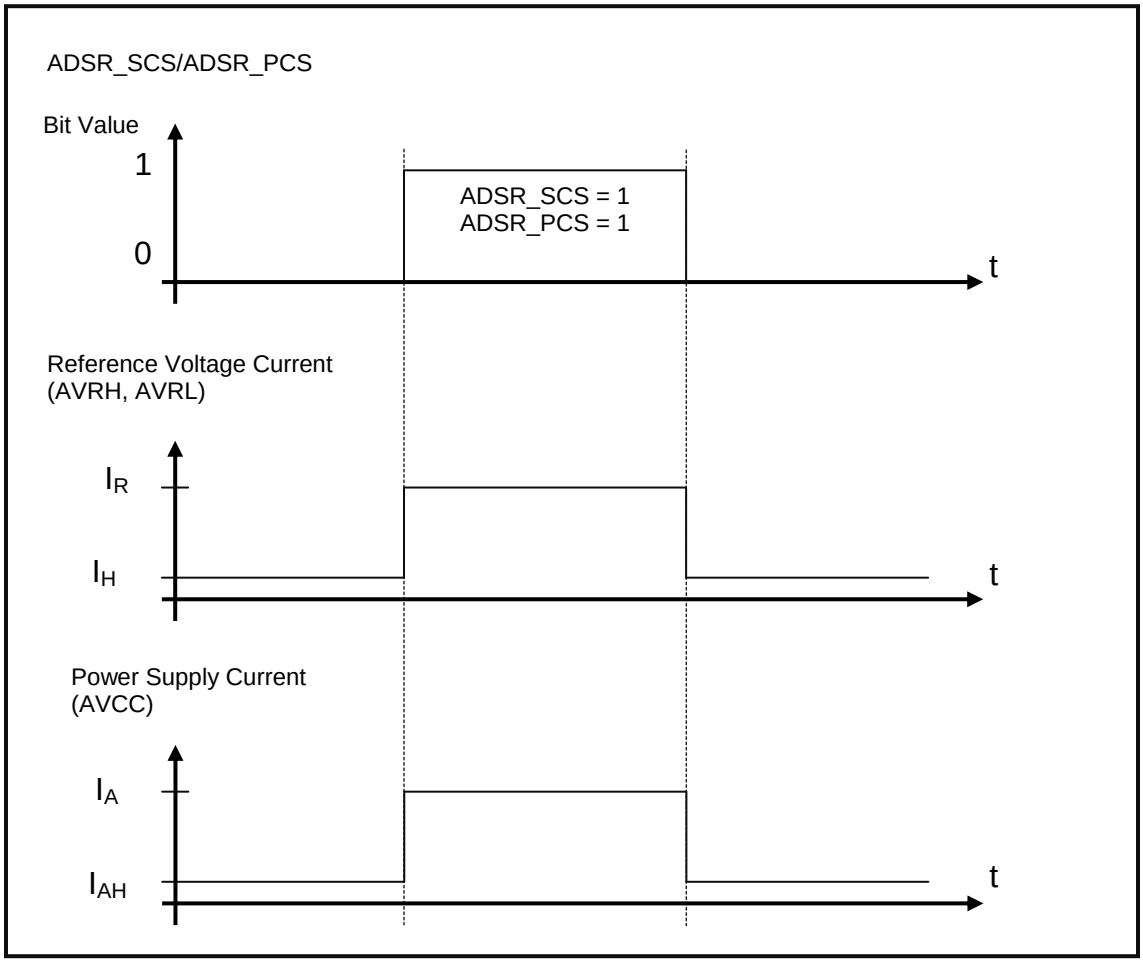
4 Analog Power Connections

The analog system voltage, applied to AV_{CC} relative to AV_{SS}, can be up to 5.5 V (absolute maximum), and must be greater than or equal to all other applied power voltages. That is, the voltage applied to the other V_{CC} power pins, relative to V_{SS}, must be ≤ AV_{CC}.

4.1 Analog Power Consumption Considerations

The power consumption (I_R, I_A) of the ADC increases when a conversion is in progress. While the ADC is halted, only leakage current (I_{RH}, I_{AH}) flows. Figure 6 shows this behavior.

Figure 6. Analog Power Consumption Considerations



Refer to the MCU's datasheet for the actual currents.

4.3 Analog Noise Consideration

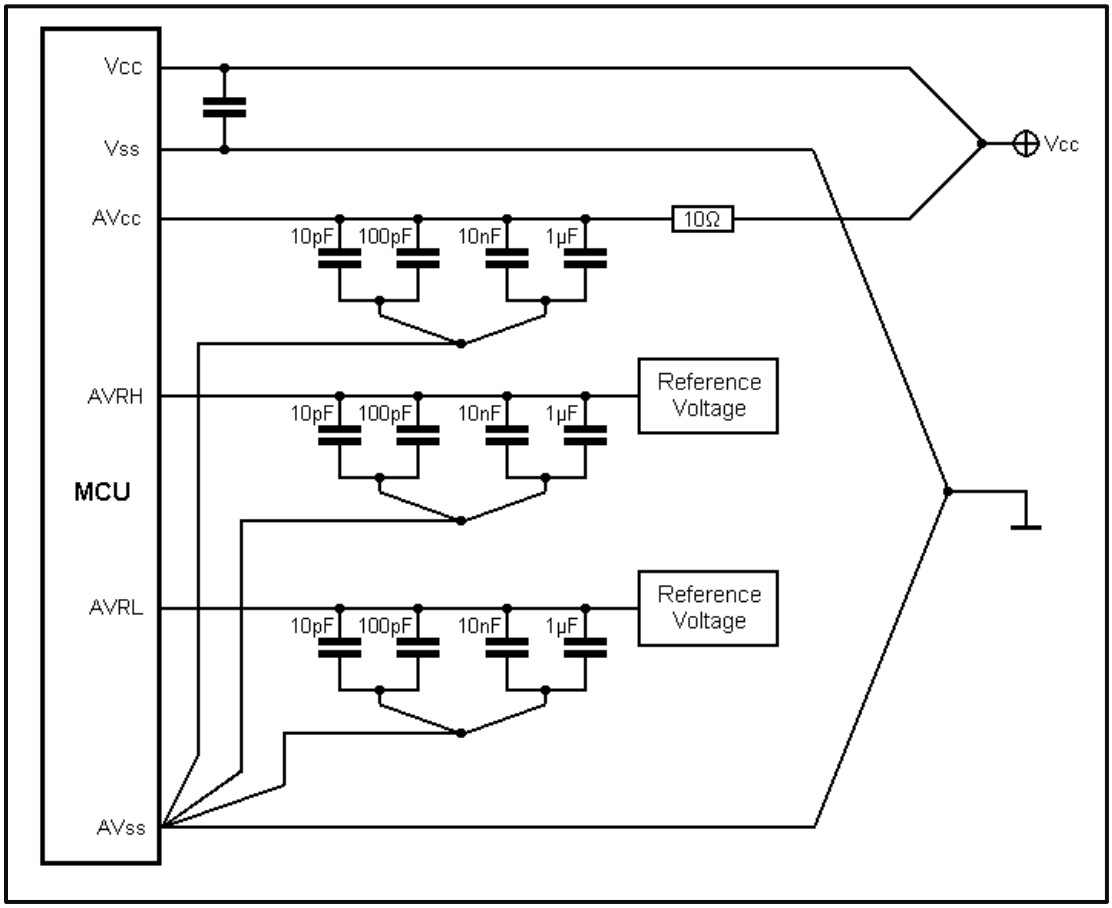
Cypress FM microcontrollers have an embedded 12-bit successive approximation register ADC. Due to the high resolution, the digital bit stream from the ADC output is sensitive to environment noise. For example, 1 LSB corresponds to only 1.221 mV for V_{REF} = 5 V. Hence, the noise introduced from external circuits must be considered and should be reduced to the minimum possible.

The reference voltage V_{REF}, which is equal to AV_{RH} - AV_{VL}, is connected to the weighted capacitor array and the resistor array of the ADC. The noise coupled to AV_{RH} is not rejected by the ADC. This noise is added to V_{REF} directly, introducing an error with a ratio of V_{Noise}/V_{REF}. For example, to keep the error caused by this kind of noise below 0.1 LSB, the noise level of V_{REF} must be kept within 0.122 mV.

To minimize noise error, connect the AV_{RH} and AV_{RL} pins with low impedance routing. In practice, often a simple low-pass RC filter is used for noise reduction. In this case, the reference voltage supply current (see datasheet) must be taken into account when calculating the filter resistor, to minimize the voltage drop while converting. Normally two capacitors in parallel are recommended: one filtering low frequency noise, the other one filtering high frequency noise ((10 nF – 1 µF) || (10 pF – 100 pF)). In most cases, this configuration suppresses the noise efficiently. If very high frequency noise appears in the environment, an additional noise filter such as a dedicated π mode RC filter might be useful.

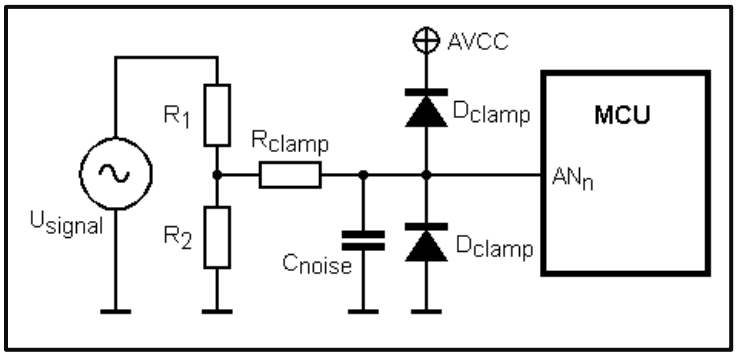
The analog power path AV_{CC} supplies the internal voltage comparator and the analog switches of the ADC, while the V_{CC} path supplies all the digital parts in the microcontroller. Internal parasitic capacitors may couple noise from AV_{CC} to the internal voltage comparator of the ADC. AV_{CC} should not be connected directly to V_{CC} - a filter should be used. For more efficient noise filtering, the same configuration as for AV_{RH} is recommended.

Figure 7. Analog Noise Consideration



4.4 Analog Inputs and Related External Circuits

Figure 8. Analog Inputs and Related External Circuits



To protect the analog pins from suffering from an over-voltage, a “clamping resistor” is usually added to the input pins. The minimum value of the resistor can be chosen as

$$R_{clamp} = U_{overvoltage}/I_{clamp},$$

Where, I_{clamp} is the specified maximum clamp current in the data sheet.

For some applications, a large clamp resistor is sometimes unacceptable. As a compromise, external clamping diodes with low leakage current may be added between the input pin and the AV_{CC} pin and the AV_{SS} pin. These clamping diodes should be rated to clamp the voltage at currents greater than the internal ESD diodes.

In some cases, the analog input voltage is biased with a voltage supply higher than the maximum allowed voltage for the microcontroller. For example, in automotive applications, sensors may be biased with the car battery, which exhibits a voltage of 12 V/24 V. A resistor divider is commonly used to reduce the sensor voltage signal seen on the pin down to a value that is equal to or smaller than AV_{CC} and V_{CC}.

The ratio between R_1 and R_2 should satisfy the following constraint:

$$\frac{R_1}{R_2} \geq \frac{U_{Signal}}{AV_{CC}} - 1$$

Another factor that influences the values of R_1, R_2, and R_{clamp} is related to current consumption budget and input signal noise suppression. The second factor is discussed here in more detail. The signal from the sensors may be noisy. The noise, which has a time constant smaller than the sampling time $T_{sampling}$, is transparent to the ADC, resulting in distorted output. In this case, an additional dedicated bypass capacitor together with the clamping resistor and resistor divider, works as a low pass filter. A larger capacitor lowers the AC impedance and is more effective at shunting away the noise signal. Generally, the time constant of this low pass filter ($R_{clamp} + R_1 \parallel R_2$) x C_{noise} should be chosen to be considerably larger than the sampling time (5 to 10 times larger as a rule of thumb).

However, this time constant should be also considerably smaller than the time constant of the analog input signal. Then, the analog pin is able to follow the dynamic changes of the input voltage, which the ADC is being used to track. These, along with the values of R_1/R_2 or R_{clamp}, must be considered when choosing the capacitor value to avoid rolling off any high frequency signal components of interest.

4.5 Analog Input Leakage Current Consideration

All analog input pins by design have a small leakage current, whose value ranges from 3 υA to 1 υA, depending on temperature. The leakage current, which flows through the external resistor, introduces an undesired voltage drop. This error voltage is a function of the external resistor and the leakage current itself. The following example shows a value of the resistor with this factor taken into consideration. For the case of using a resistor divider to reduce the error due to leakage current, the size of $R_1 \parallel R_2 + R_{clamp}$ should not be too large and should be according to the following equation:

$$R_1 \parallel R_2 + R_{clamp} \leq \frac{U_{LSB}}{I_{leakage}}$$

Note:
$U_{LSB} = U_{REF} / 4096$

To keep the error smaller than one LSB for a leakage of 3 μA, the size of $R_1 \parallel R_2 + R_{clamp}$ should be smaller than 400 Ω. As the leakage current drops down to 1 μA, the value of R1 || R2 + R_{clamp} can be chosen as large as 1.2 kΩ. This is considering V_{REF} of 5 V.

The leakage current consists of two parts: one is due to the leakage current of the input ESD structure. Another leakage current appears only as the multiplexer is switched on during sampling time; its contribution is usually considerably larger than the one created from the ESD structure. The second leakage current can be regarded as a noise during the sampling time by the bypass capacitor, which is commonly used to filter the noise from the sensor input. If this capacitor is large enough, it can absorb most of the second leakage current during the sampling time, eliminating its contribution to the error voltage.

Figure 9. Sources of Analog Leakage Offset Currents

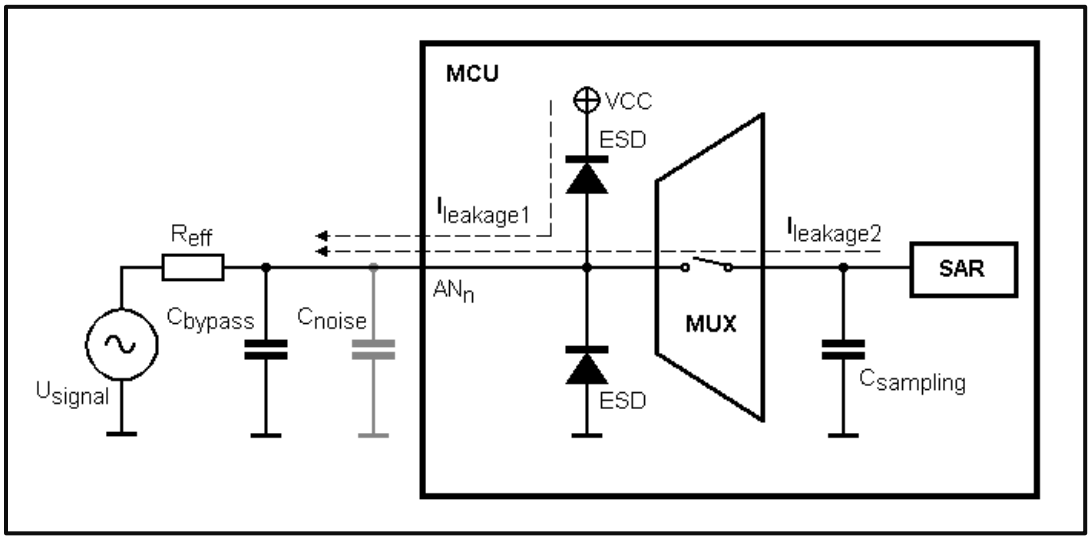
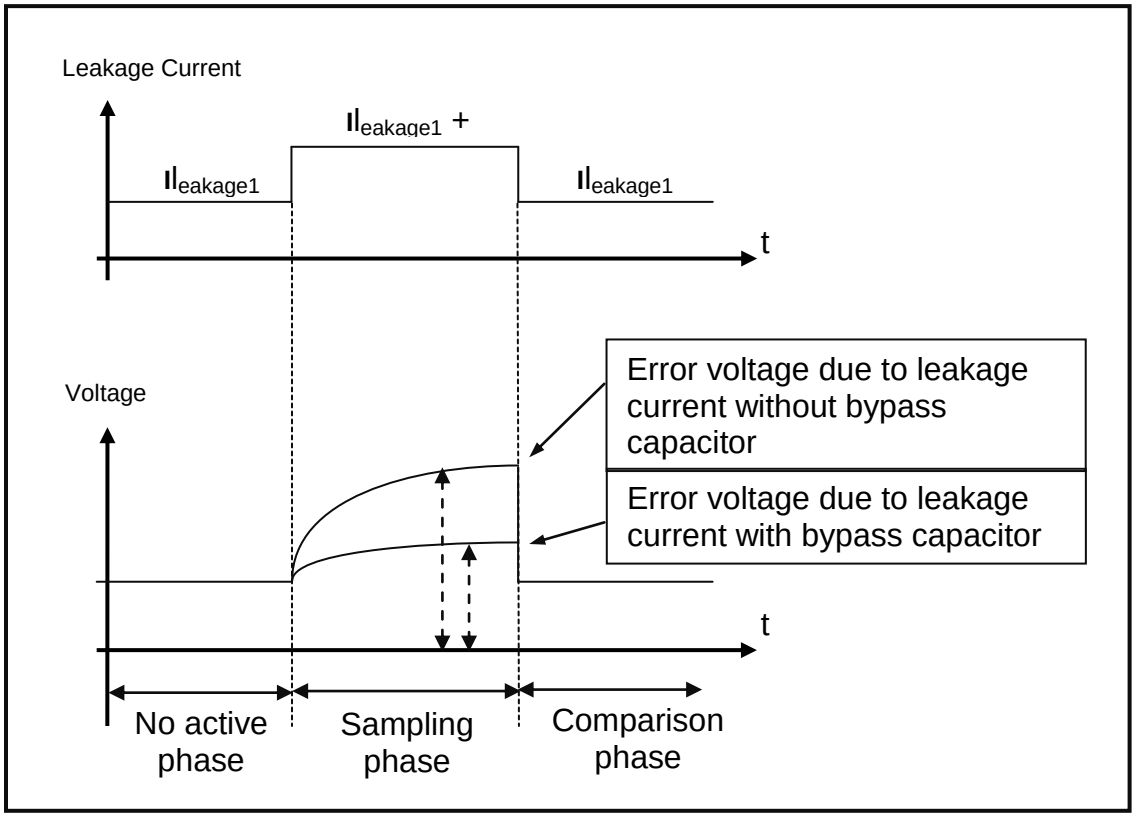


Figure 10. Error Voltage in the Sampling Phase



To show the effect of the bypass capacitor on reducing the leakage current error, we take a sampling time of 5 μs and a leakage current of 3 μA as an example. If we want to keep the voltage drop due to the second leakage current smaller than 0.5 LSB, the minimum size of the bypass capacitor should be chosen as:

$$C = \frac{3\mu A \times 5\mu s}{4.99mV / 2} \approx 6nF$$

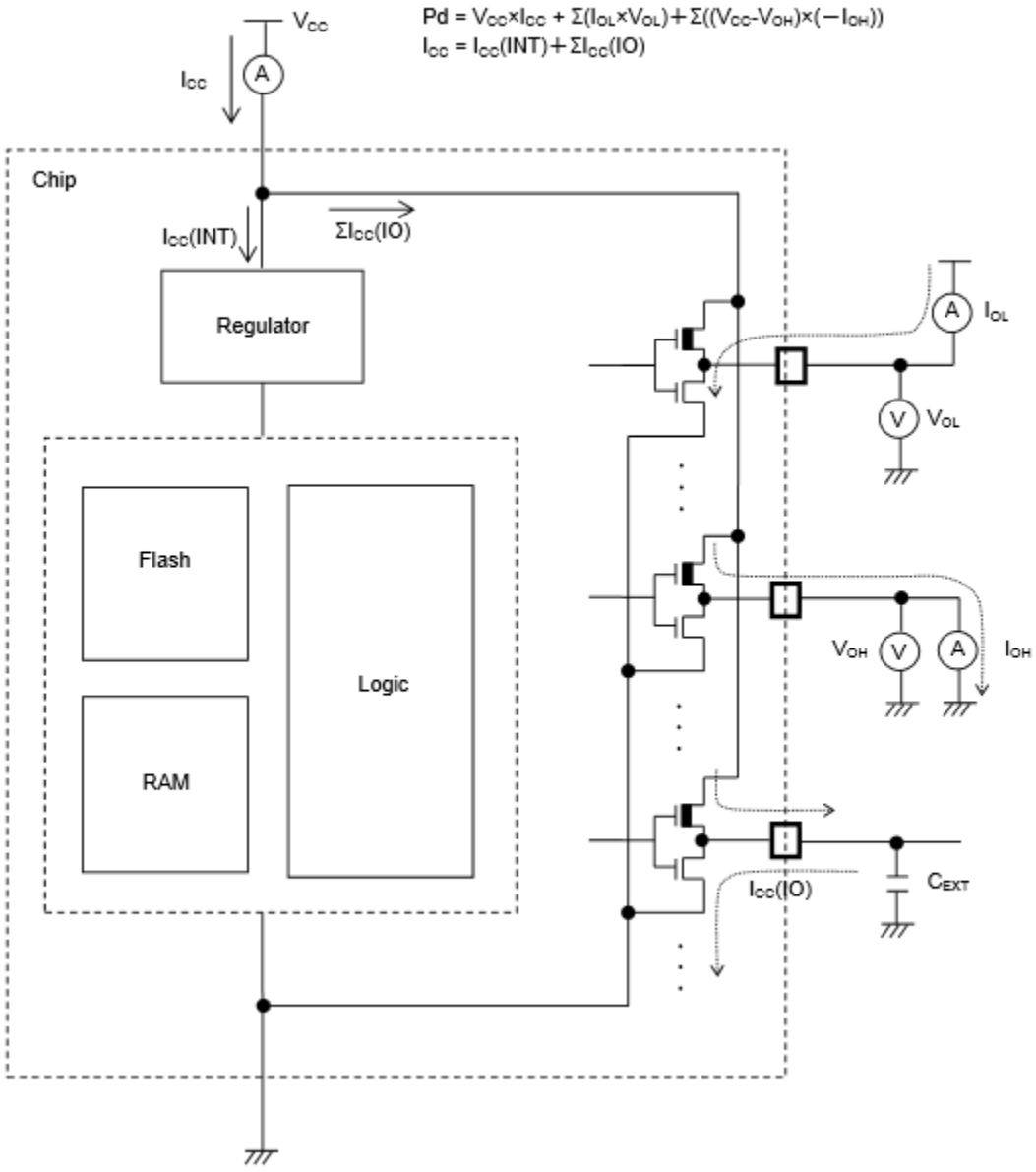
4.6 Total Chip Power Considerations

Each IO pin driver has a drive capability based mainly on the functionality assigned to the given port. For most pins/ports this is a fixed value; for some it is programmable. The maximum value of the drive current is 4 mA, 8 mA, 10 mA, 12 mA, or 20 mA. The current depends on the major function associated with each pin group. See GPIO and Non-Power Pins for more detail of individual pin currents.

It is important to know that the total combined drive of all pins cannot exceed 100 mA average over a 100 ms period. Peak currents of up to 200 mA total are permissible as long the duration is less than 100 ms.

In addition to the power sourced from and sunk into the pins, the operating current of the peripherals internal to the device must be considered. Many of the high performance FM4 devices with a large number of internal peripherals can consume more than 250 mA of internal peripheral current. Data for each peripheral is listed in the datasheet. A good estimate of the total operating current can be calculated from adding these peripheral currents. Figure 11 shows the total power of an MCU implementation (Pd). It is based on the sum of the currents of all the internal peripherals (from data sheets) I_{CC} (INT) and the sum of all I/O currents I_{CC} (IO) calculated from circuit design components driven by the I/O pins.

Figure 11. Sources of MCU Total Power.



4.7 Thermal Considerations

Once an indication of the MCU total power requirement is known, it is very important to understand if the system design can properly dissipate this power into the ambient air efficiently enough to require no further action or if significant heat sinking and PCB design choices might be required. The Cypress FM family MCUs cover a wide range of products from devices capable of very low power to MCUs with very fast complex logic requiring higher power needs. Under certain conditions, MCUs may dissipate more than 1 Watt of power including the core, peripheral, and I/O currents. With a lot of power in a device, you must consider steps necessary to keep it from overheating. Before a design is finalized, a complete thermal review should be done. Items such as the amount of airflow through the system, nearby heat sources, and PCB construction should be reviewed. The examples given below are first steps to determine whether your preliminary design objectives can be met.

For a first order approximation, first check the datasheet for the thermal resistance from junction to ambient (θ_{JA}), for the package that you intend to use. θ_{JA} is expressed in units of °C/watt. For example, the θ_{JA} for an LQFP 120-pin FM4 is 38°C/watt. For the same device in an LQFP 120-pin package with an exposed pad on the bottom side correctly mounted, the θ_{JA} is reduced to18°C/watt, allowing a much higher total device power usage or a higher ambient operating temperature.

The maximum temperature difference between the device junction and the ambient air surrounding the device is θ_{JA} times the maximum power, or as in the first case above 38°C/watt x 1.0 watt = 38°C. Because the specified maximum operating junction temperature of the device is 125°C, the maximum allowable ambient air temperature is 125 – 38 = 87°C. If you use the exposed pad version of package, which has a lower thermal resistance θ_{JA} of 18°C/watt if implemented with proper PCB to pad design, then the maximum allowable ambient air temperature is 125 – 18 = 107°C. This allows a 20°C increase in ambient operating temperature or the possibility to drive more power from the device I/O or core.

Each datasheet for a device series contains a table showing package thermal resistance and maximum permissible power. This allows you to quickly see the amount of power that can practically be consumed by a device in a given package. The table also gives recommended minimal PCB construction. Most FM MCUs can be mounted to simple single or double layer printed circuited boards. For other devices, the table recommends at least a four layer construction, where the inner plane layers help dissipate heat.

Note: The datasheet specifications for θ_{JA} are typical. You should design your product such that the ambient air temperature is much less than the allowable maximum.

Note: With the above calculation, if the θ_{JA} or the power dissipated is high, the maximum allowable ambient air temperature could theoretically approach the 125°C junction temperature limit. However, the product's commercial-range ambient air temperature limit of 85°C or the industrial-range ambient air temperature limit of 105°C still applies. In the examples above, the first example would be unacceptable for operating a consumer grade (85°C) device. In the second example, a consumer grade or industrial grade device would be well suited depending on the choice of operating conditions of the final product.

Many FM MCU devices are offered in PBGA and QFN packages. Due to the small size reducing the available surface area for thermal conduction, these packages must be thoroughly reviewed for power applications. For more information and examples of higher order thermal review, see AN72845, Design Guidelines for QFN Packaged Devices.

4.8 Power Ramp-up Considerations

Turn power on/off in the sequence shown below or at the same time. If not using the A/D converter and D/A converter, connect AV_{CC}= V_{CC} and AV_{SS}= V_{SS}.

Turning on: $V_{BAT} \rightarrow V_{CC} \rightarrow USBV_{CC}$

$V_{BAT} \rightarrow V_{CC} \rightarrow ETHV_{CC}$

$V_{CC} \rightarrow AV_{CC} \rightarrow AV_{RH}$

Turning off: $USBV_{CC} \rightarrow V_{CC} \rightarrow V_{BAT}$

$ETHV_{CC} \rightarrow V_{CC} \rightarrow V_{BAT}$

$AV_{RH} \rightarrow AV_{CC} \rightarrow V_{CC}$

The voltages at the V_{CC} pins must be less than or equal to that on AV_{CC}.

When powering up the device, the maximum ramp rate for any V_{CC} pin is 0.1 V/µs.

5 GPIO and Non-Power Pins

The I/O pins of the FM MCU family are made of I/O pin drivers of different types. The type of pin driver and a reference schematic of the driver and the current capability of each are all described in the datasheet in “I/O Circuit Type” for a particular device. These circuit types can then be related to the actual device pins in “Pin Descriptions” in the datasheet.

While almost any pin can be used as a general-purpose I/O, note that the current drive for pins is allocated per the major peripheral function of the pin. For example, the current drive on the NAND flash interface is 3x greater than the standard I/O drive. If a system had a very long run CSIO (SPI) link and no need of the NAND interface, you could use the multifunction serial (MFS) block associated with the pins of the NAND flash interface for the CSIO. See Table 2.

Table 2. Pin Function and Associated Pin Current

Pin Function	Associated Pin Current
GPIO	4 mA
SD Card	8 mA
UART	8 mA
Hi Current MFS I^2C/SPI	8 mA
Remaining MFS modules	4 mA
USB	~20 mA
NAND	12 mA
Ethernet	8 mA
Quad SPI	4 mA / 10 mA selectable.
External Bus Ctln / Clk	8 mA

For more information on all pin types, see the datasheet for your device.

Table 3 shows the remaining MCU critical pins and gives short information about how to connect them.

Table 3. Remaining MCU Critical Pins and their Connections

Pin Name	Function
V_{CC}	Main supply for I/O buffer and MCU core.
V_{SS}	Main supply for I/O buffer and MCU core.
C	External 4uF to 10 µF ceramic capacitor (dielectric X7R) as smoothing capacitor for internal 1.2 V regulator output, used for supply of the MCU core. Refer to the datasheet for selection of capacitance value.
AV_{CC}	Power supply for the A/D converter.
AV_{SS}	Power supply for the A/D converter.
AV_{VRH}	Reference voltage input for the A/D converter.
$USBV_{CC}$	Power supply for internal USB host/function. Use voltage according to datasheet and purpose of supplied pins (USB or GPIO).
$ETHV_{CC}$	Power supply for internal Ethernet MAC. Use voltage according datasheet and purpose of supplied pins (Ethernet or GPIO).
X0, X0A	Oscillator input. If not used, it shall be connected with pull-up or pull-down resistor or set to digital output (see the datasheet).

Pin Name	Function
X1, X1A	Oscillator output. The crystal and bypass capacitor must be connected via shortest distance with X1/X1A pin. If not used, it shall be open.

5.1 C Pin Decoupling

The C pin is connected to the internal 1.2 V supply for the MCU core. Proper filtering and decoupling of this pin is critical for a working design. The decoupling capacitor must be placed very near to the C pin.

Figure 12 shows the recommended routing and placement for single sided metal layer. (Note that in all following illustrations, the mounting metal layer is drawn in black and the back side metal layer in gray).

Figure 12. C Pin Routing and Placement for Single Sided Metal Layer Circuit Board

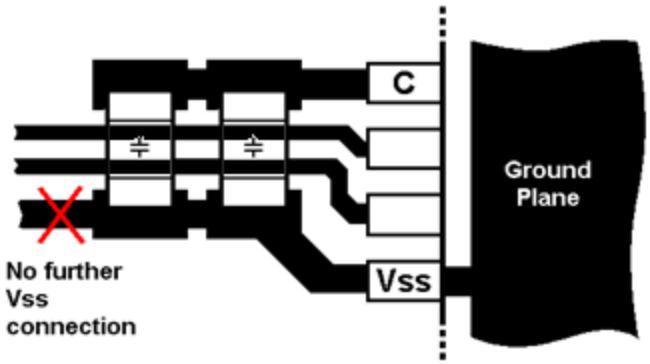
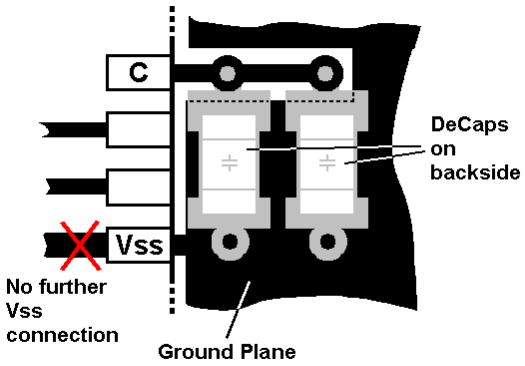


Figure 13 shows the recommended routing and placement for double sided metal layer. Note that despite the capacitor being placed on the opposite side from the MCU, this solution is preferred as the via to the ground plane and the via connecting to the C pin minimize inductance over other solutions.

Figure 13. C Pin Routing and Placement for Double Sided Metal Layer Circuit Board



5.2 Quartz Crystal Placement and Signal Routing

The crystal must be placed as near as possible to the MCU. Therefore the oscillator capacitors must be placed “behind” the crystal. Figure 14 shows the recommended placement and signal routing for a single metal layer circuit board.

Figure 14. Quartz Crystal Placement and Signal Routing for Single Metal Layer Circuit Board

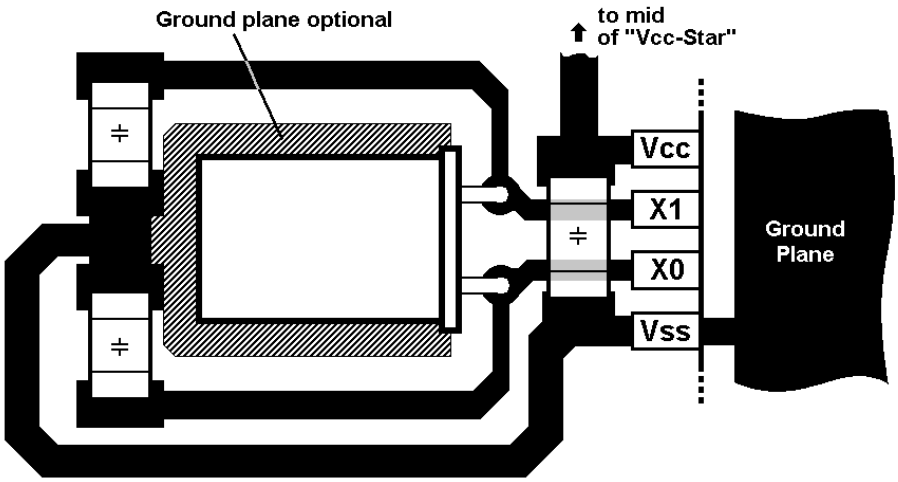
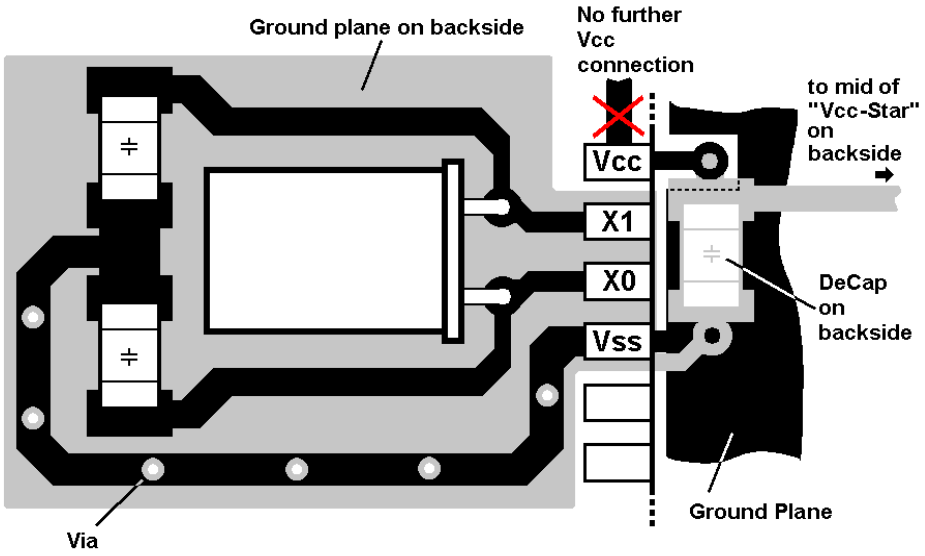


Figure 15 shows the quartz recommended placement and signal routing for a double sided metal layer layout.

Figure 15. Quartz Crystal Placement and Signal Routing for Double Metal Layer Circuit Board



5.3 Device Reset

To reset the FM MCU, apply a low-level pulse to the INITX pin. This can be via a switch or external reset controller. A capacitor must be connected between Vss and the INITX pin for debouncing the switch and for EMI protection. Use a capacitor of not more than 1 nF. This capacity covers the most common frequency protection in a wide range. Higher capacities and the high input impedance of the INITX pin may cause latch-up effects with high currents being released from the capacitor through the INITX pin by the Reset SW. If a high value must be used, limit any current rush with a series resistor.

Note that reset is not a low power condition. The MCU must be released from reset and commanded into low power modes. Reset should not be used as a method of power gating the device. While the I/O pins are generally in high impedance mode, the internal peripherals may be actively clocked and waiting for the rising edge of INITX to initialize.

5.4 I/O Pins and Device Reset

The I/O pins are always in one of three states relative to device reset:

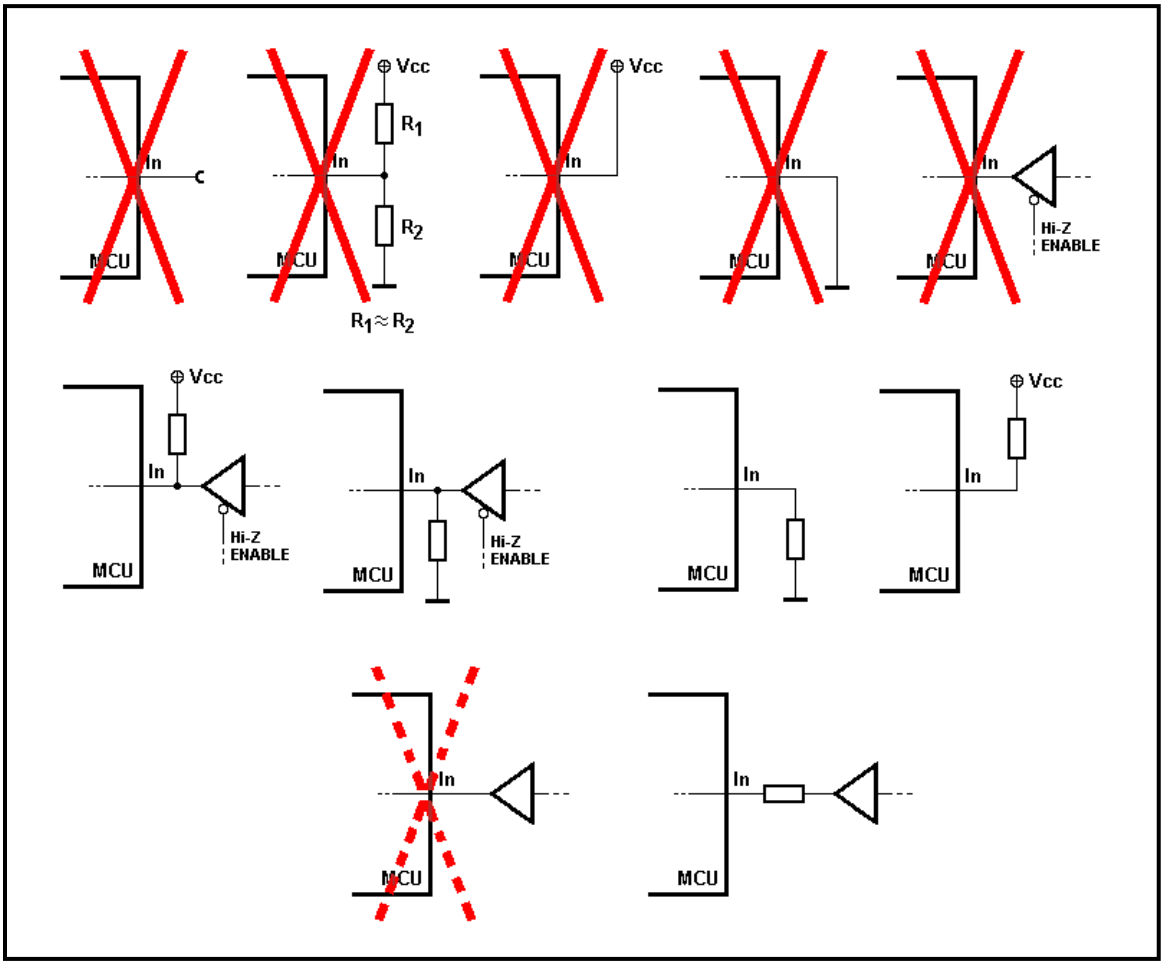
1. While reset is active, all I/O pins are in the high-impedance analog state.
2. When the MCU comes out of reset, the state for each I/O port is set to high-impedance analog (the default), pull-up, or pull-down.
3. The final state for each I/O pin is determined by user software. Care in software coding should be taken to ensure there are no floating inputs or contending outputs in any condition.

6 Port Input / Unused Pins / Latch-up

Do not leave digital I/O pins unconnected while they are switched to input. If they are unconnected while being switched to input, those pins can enter a so-called *floating state*. This can cause a high I_{CC} current, which is adverse to low power modes. Also, damage to the MCU can occur. Use the internal pull-up resistors in this case. If not, use external pull-up or pull-down resistors to define the input-level. Figure 16 shows every possible way to connect I/O to a MCU GPIO pin. While you are designing, match your GPIO case to this figure and verify that it is a proper connection.

Never connect a resistor divider with similar resistance values as shown in the second example of the figure below. Be very careful in connecting the output of an external device to the MCU (see example below with dotted cross) make absolutely sure that you understand the power up, reset and, run conditions that this MCU pin may exhibit. For good design practice, you should consider using the next example over and adding a small series resistor to protect the system if the MCU and the external device ever have their outputs driven at the same time.

Figure 16. Connecting Digital I/O Pins



Be careful connecting input pins to other devices that can go into High-Z states. Always use internal pull-up or external pull-up or pull-down resistors in this situation.

Outputs from external digital circuits should always be connected via a serial resistor to an MCU input pin to prevent latch-up effects caused by under- or overshoots.

Choose debouncing and decoupling capacitors that are as physically small as practical. This reduces the inductance of the capacitor and the interconnect.

All pins are set to input after their power-on default if they do not share an analog port. Analog ports have the digital I/O functionality disabled after reset. They may be left open, but for ESD protection, they should be terminated with a pull-up or pull-down resistor if not used.

Note:

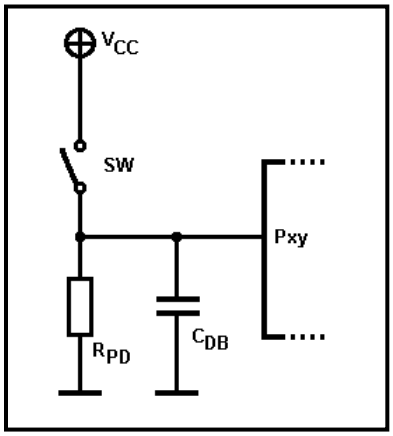
Do not connect any input ports directly to V_{CC} or V_{SS} (GND) if PCB routing and power supply can carry noise. Use pull-up or pull-down resistors (2 kΩ … 4 kΩ).

7 EMC, ESD Protection, Latch-up Consideration

Be careful with external switches to V_{CC} or ground together with debouncing capacitors connected to port pins.

A typical configuration is shown in Figure 17.

Figure 17. External Switch Configuration

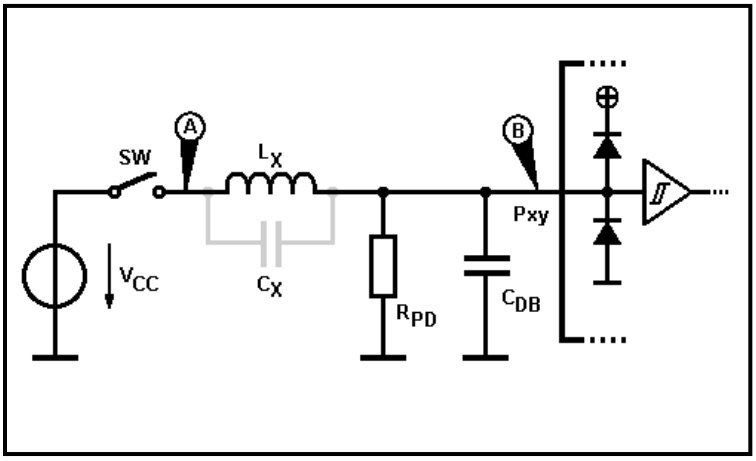


R_{PD} is a pull-down resistor and C_{BD} is a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed, the input changes to “1”.

From the physical aspect, you must consider that the switch is often placed some distance from the MCU by cable, wire, or circuit path. The longer the circuit path is, the higher is its inductivity L_X (and capacity C_X).

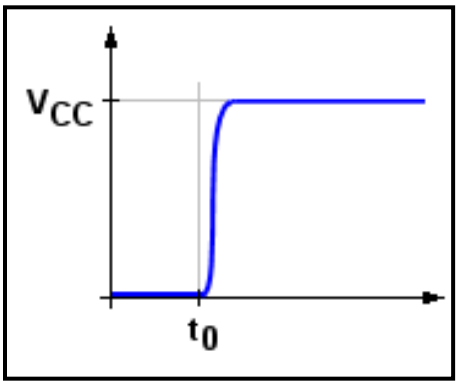
An equivalent circuit diagram is shown in Figure 18.

Figure 18. Equivalent Circuit Diagram



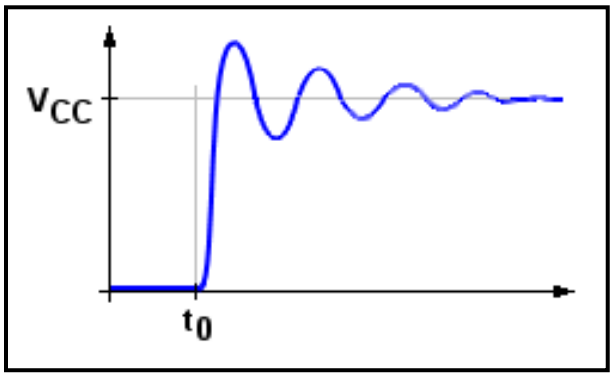
By closing the switch SW at time t_0, the voltage can be measured at point (A) in the above circuit as shown in Figure 19.

Figure 19. Measuring Voltage at Point (A)



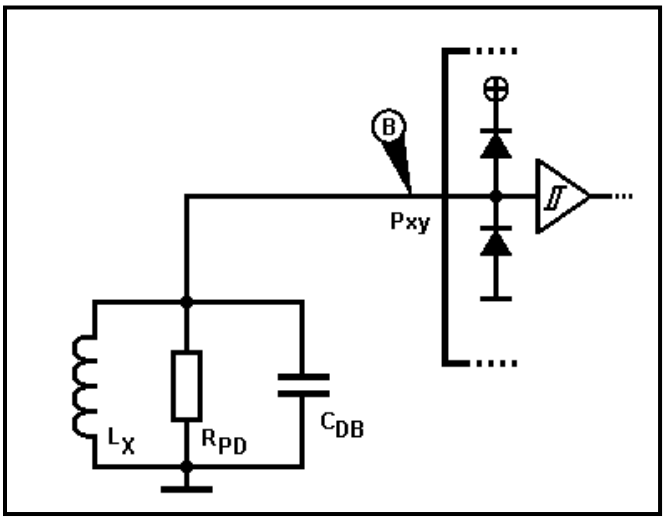
But at the port pin Pxy on point (B) in the above circuit the voltage can be measured as shown in Figure 20.

Figure 20. Measuring Voltage at Point (B)



By closing the switch SW, (as in Figure 21) the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debouncing capacity C_X, and the damping R_{PD} of the pull-down resistor, assuming the power supply to be ideal (no internal resistance).

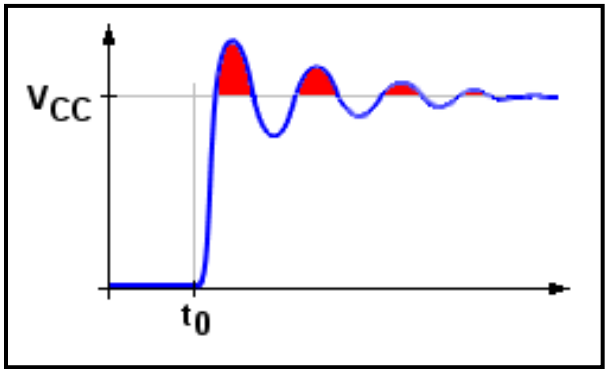
Figure 21. Circuit after Closing Switch SW



Because R_{PD} is often chosen high (> 50 kOhms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in Figure 22.

Figure 22. Voltage Overshoots on the Port Pin



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to V_{CC} becomes conductive. Opening the switch causes a similar result. In this case there are undershoots on the port pin.

The frequency of the oscillation can be calculated by:

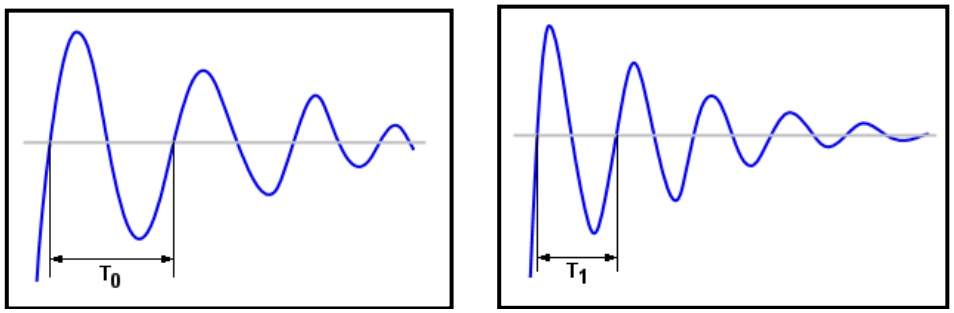
$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}}$$

The inductivity L_X is the unknown value and depends on the PCB, its routing, and the wire lengths.

There are two countermeasures to prevent latch-up.

One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the overall energy of the overshoots is smaller. See Figure 23.

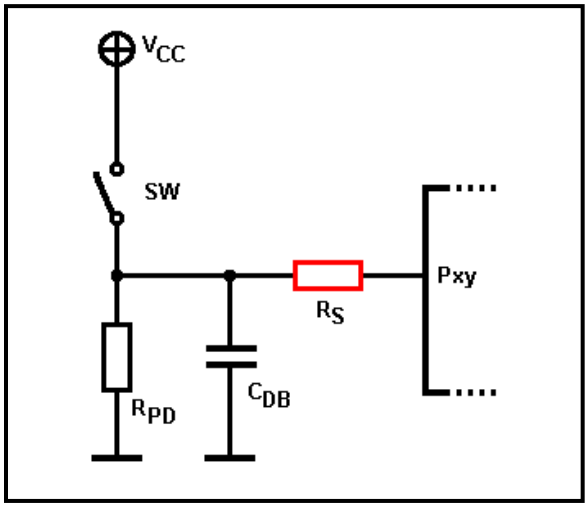
Figure 23. Decreasing the Capacity of the Debouncing Capacitor



This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee that the latch-up condition is eliminated.

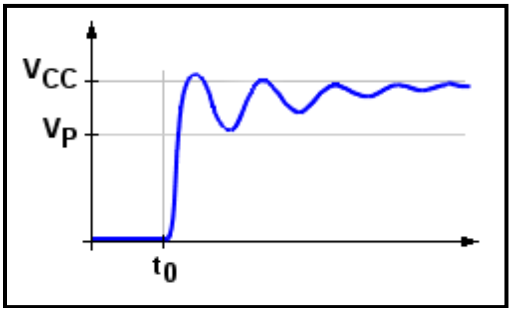
A better solution is to use a series resistor at the port pin, as Figure 24 shows.

Figure 24. Using a Resistor at the Port Pin



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the positive CMOS level. See Figure 25.

Figure 25. Effect of the Series Resistor R_S



Good design practice is to protect I/O pins, and consequently the device itself, from electrostatic discharge (ESD) by putting on the PCB a 50 Ω to 100 Ω resistor in series with any I/O pin that is routed off the PCB – for example to a button or a connector.

For more information on electromagnetic compatibility (EMC) and ESD considerations, see AN80994, PSoC EMC Best Practices, and Appendix A.

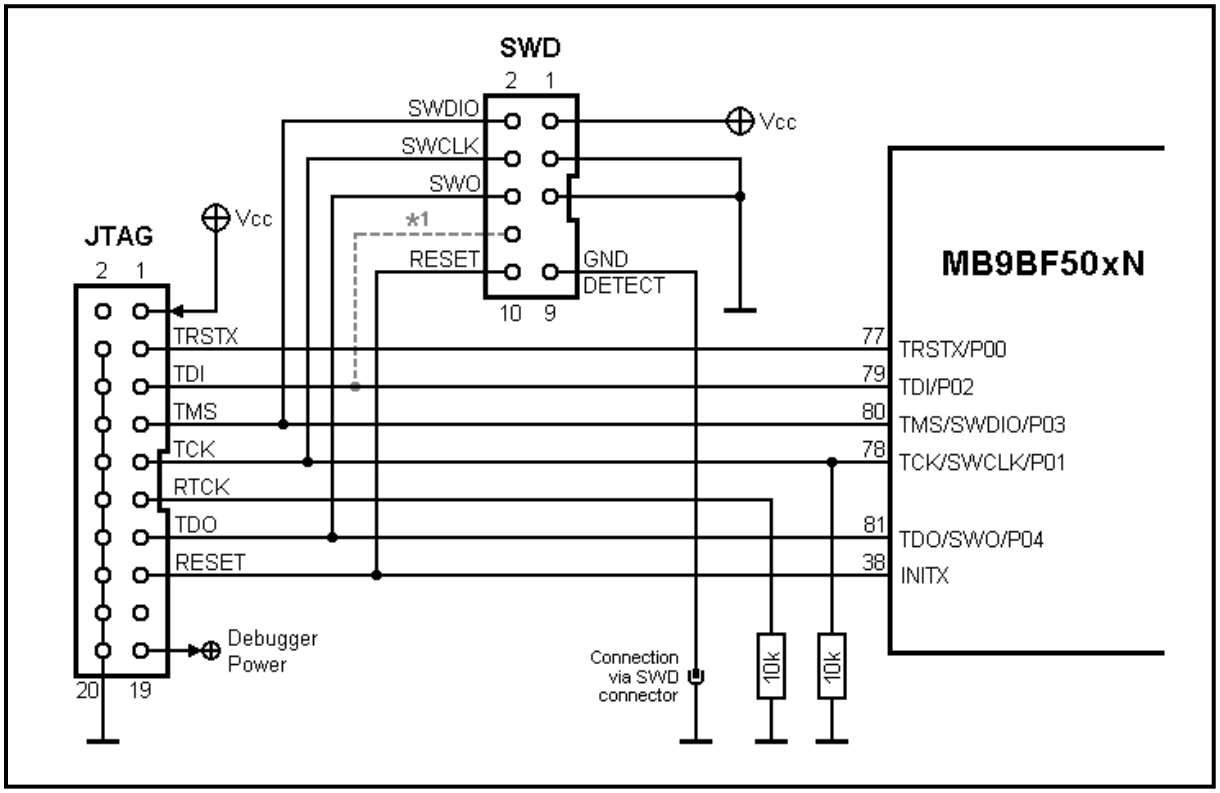
8 Programming and Debug

All of the FM families of MCUs support both the Joint Test Action Group (JTAG) and serial wire debug (SWD) interfaces for device flash programming and debugging. In addition, the FM3 and FM4 family of devices supports an extended Traceport capability available to enhance the debugger capability by adding trace capability.

8.1 JTAG/SWD Connections

The FM MCU family supports JTAG debugging for full JTAG and SWD. Figure 26 shows the connection for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM derivatives and their JTAG/SWD pin locations. If supported by your debugging system, the external debugger can optionally supply power to the system in test from the Debugger Power output on pin 19 of the JTAG connector.

Figure 26. JTAG/SWD Connection

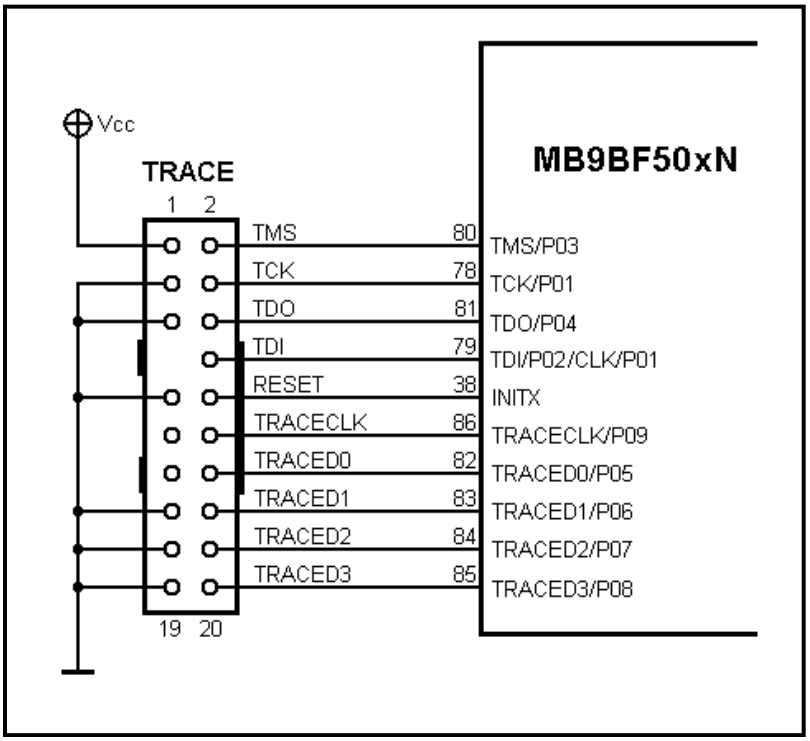


*1 Only needed if SWD connector should also provide JTAG lines

8.2 Traceport Connections

Besides the JTAG/SWD ports, the FM3/FM4 MCU families also support debug via Traceport. Figure 27 shows the connections for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM derivatives and their Traceport pin locations.

Figure 27. FM3/FM4 Debug Trace Port Connection



Unlike the event trace provided by the SWD and JTAG, the Traceport lets you know what your application was doing before it received an interrupt, what it is doing while the ISR is executing, and what happens after it leaves the interrupt. It tells you where the application has been and exactly how it got there. In short, it gives you full insight to your application's behavior in real-time without being intrusive.

9 Minimum System

There are components required to guarantee that an FM MCU device always is recoverable in a user system. There are conditions under which the part is NOT reprogrammable via debug mode. Setting the flash security bit, poor software programming, wrong PLL settings, or other factors might keep an MCU from booting into user operating mode and make it incapable of off chip programming.

To help you avoid locking up a system so that it is no longer usable, Cypress provides a small boot ROM on every FM device. This ROM is activated by pulling the MD0 pin to a high state. Port 6 bit 0 (P60) is used to select between serial and USB recovery mode.

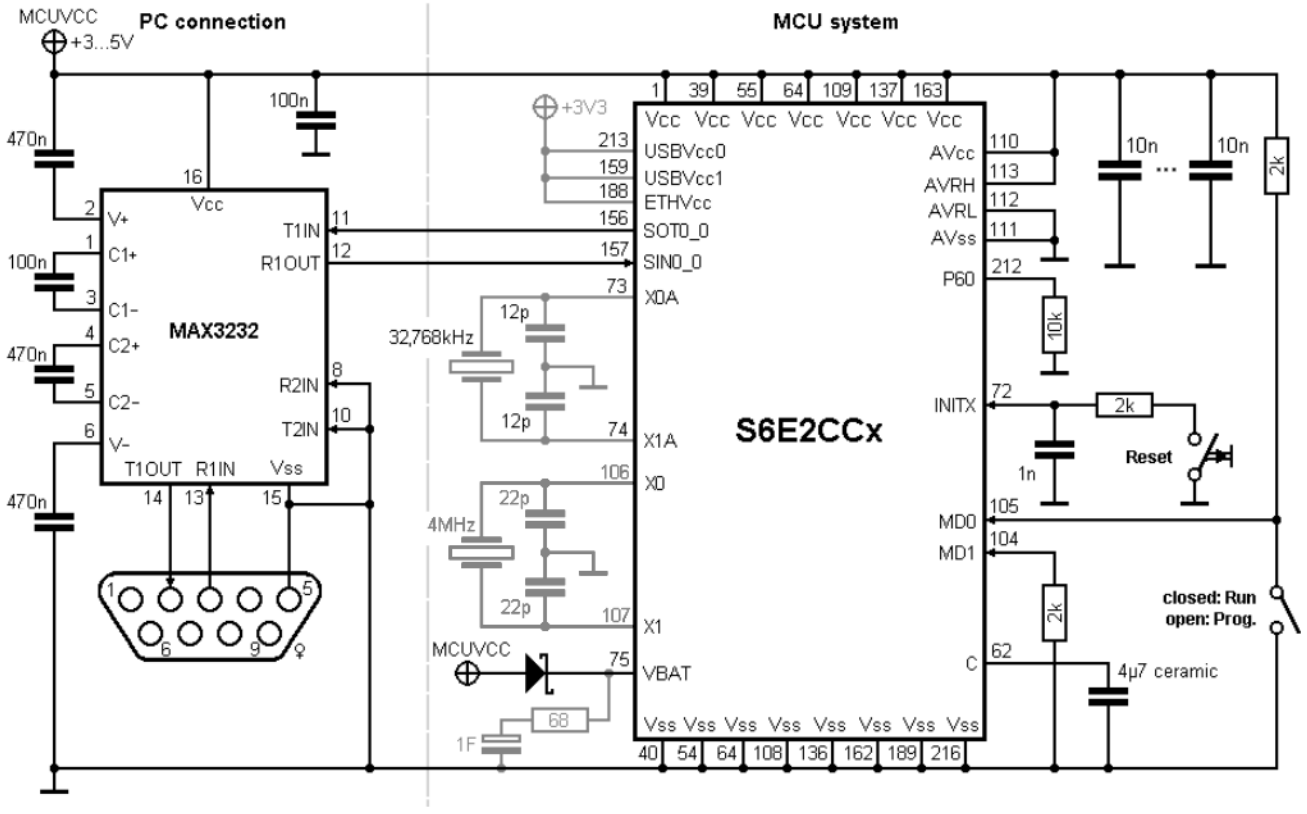
Figure 28 and Figure 29 show the configuration of these two methods of recovery and the components required to implement each method. Components shown in the two figures below are coded as Black = required and Gray = optional but suggested. The choice of implementation is completely up to you. You might not need an RS-232 interface; in this case you could remove the RS-232 driver device and implement a 5 volt serial-to-USB cable to connect and recover the system.

If needed, this mode of operation can also be used for production programming of the device. Be aware that proprietary software is needed to recover and program the device. The “MCU Flash programmer” software and “USB Direct Programmer” software are available on our website.

9.1 Schematic (Serial Programming)

Figure 28 is a schematic of a minimum hardware system that uses the UART asynchronous channel for flash programming. Note that for other MCU families, a different interconnects to the serial driver is required. Please see device data sheet.

Figure 28. RS232 Programming



9.2 Serial Interface

The PC connection section is needed only if there are no 3...5 V external serial data lines for programming. The MAX3232 is a standard level shifter, which converts the 3...5 V levels of the MCU to ±12 V RS232V24 levels, and vice versa.

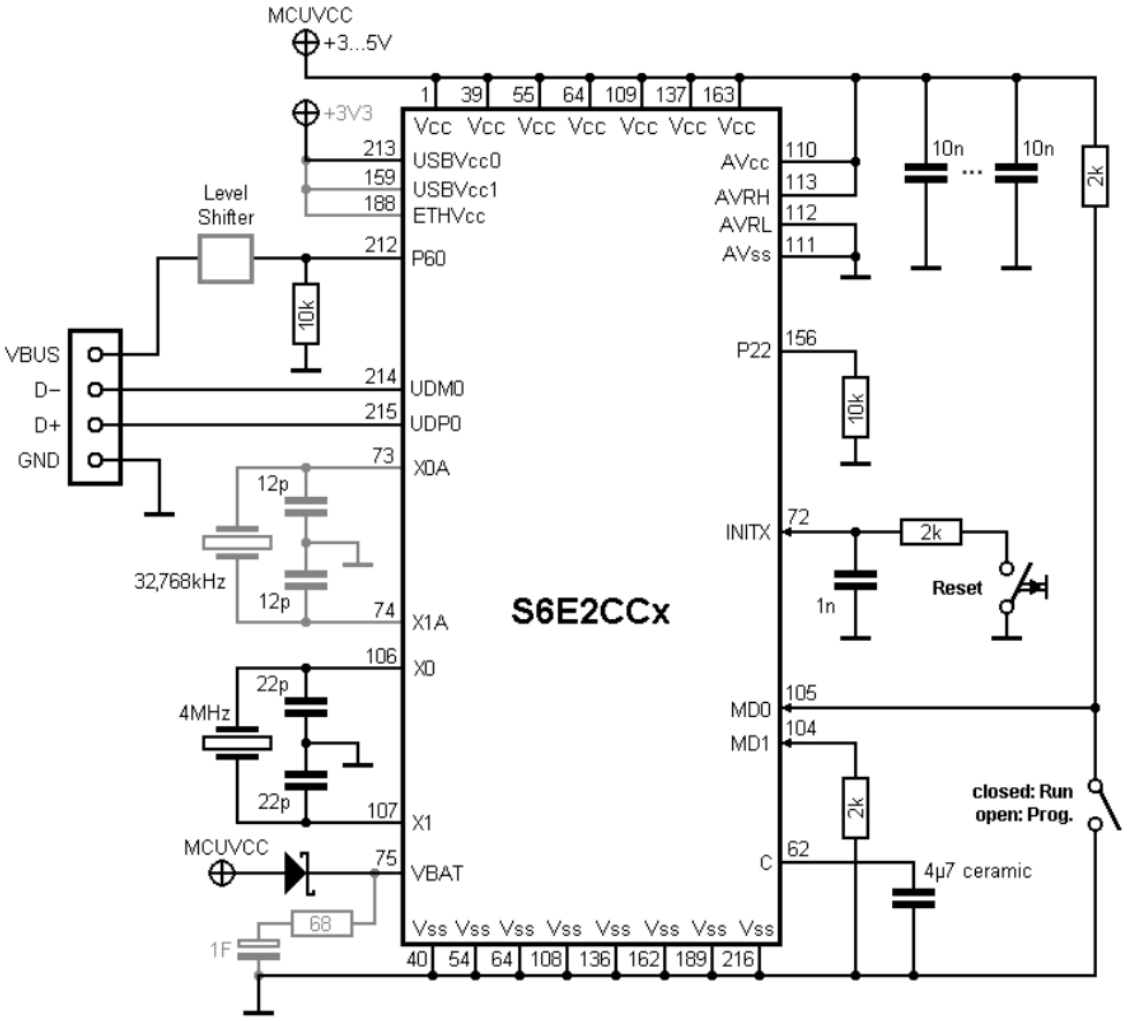
Consider that the internal charge pumps of the level shifter can produce noise on the +3…5 V line, which can influence the ADC, if AV_{CC} and AV_{RH} are directly (unfiltered) connected to it.

Consider that the logic level at port P60 determines UART or USB programming. If the port is not used in your application and USB programming is not needed, it can also be connected directly to GND (considering good EMI routing). Do not switch this port to output mode in this case.

9.3 Schematic (USB Programming)

Figure 29 is a schematic of a minimum hardware system that uses the USB function for flash programming (if USB is available on the MCU). Note that for other MCU families, a different interconnect to the serial driver is required. Please see device data sheet.

Figure 29. USB Programming



10 USB Interface

The MCU can be supplied either by external power or by V_{BUS} connection to the USB host. In any case, for $USBV_{CC}$ +3.3 V is needed. Use a 3.3 V regulator for $USBV_{CC}$, if V_{BUS} is used for powering the MCU.

Consider that the internal charge pumps of the level shifter can produce noise on the +3…5 V line, which can influence the ADC, if AV_{CC} and AVRH are directly (unfiltered) connected to it.

Note: Cypress kit schematics provide good examples of how to incorporate MCUs into board schematics. For more information, see Related Documents.

11 Summary

Many of the hardware considerations given in this application note are similar to those for other MCU devices. However, the power and flexibility of FM families raise additional topics, such as selecting the best pins for the application and using opportunities to simplify and optimize PCB routing.

This application note has provided information on each of these topics, so that you can successfully design Cypress MCU devices into a PCB and hardware environment.

Use the checklist in Appendix B – Schematic Checklist to check your hardware design.

12 Related Documents

The following application notes are a good source for more detailed information:

- AN57821 – PSoC 3 and PSoC 5LP Mixed Signal Circuit Board Layout Considerations
- AN72845 – Design Guidelines for QFN Packaged Devices
- AN89611 – PSoC 3 and PSoC 5LP Getting Started with Chip Scale Packages
- AN69061 – Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages
- AN88619 – PSoC 4 Hardware Design Considerations

Cypress development kit schematics are good examples of how to incorporate MCUs into board schematics. It may be helpful to review the following Cypress kit schematics:

- FM0-64L-S6E1C3 FM0+ S1E1C –Series Starter Kit.
- FM4-176L-S6E2GM FM4 S6E2GM Pioneer Kit.

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A Appendix A – PCB Layout Tips and I/O Pin Selection

When you create a schematic with an FM Family device, you should select which pins go to which functions in the following order:

1. **Power pins:** How many different or separate voltages are required for digital, analog, and USB power? The analog converter supply pins (AV_{CC}, AV_{SS}, AV_{RH}) should be connected even if the ADC of the MCU is not used to avoid latch-up conditions on the analog pins even if they are switched to digital input. See Power System for details.
2. **Crystal and clock generation:** You must plan for these high impedance (crystal) and or high frequency clock traces at the very beginning of your design. Your layout needs to accommodate keepouts and keepaway for these signals.
3. **C pin:** A 1..10 µF ceramic capacitor (dielectric X7R, for example 4.7 µF) must be connected near the C pin of the MCU. Otherwise, the MCU may not operate correctly or may be damaged in worst case.
4. **Mode Pins:** The mode pins signal the MCU operation mode after reset. They should be pulled-up with 2 kΩ resistors. If the PCB routing protects against ESD and EMI influence, the mode pins can be connected directly to V_{CC} and V_{SS} (GND) depending on needed logic level – see Programming and Debug for details.
5. **Fixed pins:** Will you need the following features:
   - Device reset? All FM devices require the INITX pin to, at a minimum, have an RC filter on the pin See Device Reset.
   - Flash programming or debug, using JTAG or SWD? If not, some of the pins can be used as GPIOs – see Programming and Debug for details. Remember to always allow for boot mode recovery of a device in the system.
   - MHz or 32 kHz crystal oscillator? If not, the pins can generally be used as GPIOs – see GPIO and Non-Power Pins for details.
   - Analog features, ADC inputs, DAC outputs, external voltage reference? If not, the pins can be used as GPIOs – see Analog Noise Consideration for details.
   - USB? If not, the USBIO pins can be used as limited GPIOs – see USB Interface. They can also be used for flash programming and debug – see Programming and Debug for details.
   - Wake from low power modes, reduced power, sleep, deep sleep? Use of special wakeup pins may be required to support exiting from some modes.
   - External bus interface? External bus interfaces often operate at high speeds and require impedance matched traces to function at full speed reliably. Short, direct routes are required. Connections should all be equal in length.
   - High speed or Quad CSIO (SPI) interface? These interfaces are both fast and have drive control selection capability. These require impedance matched traces to function at full speed reliably. Short direct routes are required. Connections should all be equal in length.
   - Ethernet? The Mii or RMii Ethernet interface should be as short and direct to the magnetics and connector as possible. Connections should all be equal in length. Physical isolation of this part of the circuitry helps reduce interface to and from this section.
6. **GPIO pins and digital function pins:** All remaining pins can be used for digital I/O functions, and can be assigned to simplify or optimize your PCB layout.
7. **NC or unused pins:** Do not leave input pins open. If not possible, switch pin to output. See I/O Pins and Device Reset.for how to proceed with unused (not connected) pins.
8. **(DNU) pins:** Any device pin marked “do not use” (DNU) must be left unconnected and floating.

   Note: Cypress FM Family and PSoC Family kit schematics provide good examples of how to incorporate PSoC into board schematics. For more information, see Related Documents.

There are many classic techniques for designing PCBs for low noise and electromagnetic compatibility (EMC). Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the V_{CC} and V_{SS} supplies. This gives good decoupling and shielding effects. Provide separate fills on these layers for AV_{CC}, $V_{CC,}$ AV_{SS}, and V_{SS}.

  To reduce cost, a 2-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all V_{SS} and V_{DD}.

- **Ground and Power Supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using 2-layer or single-layer PCBs.

  The power supply should be near to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of electromagnetic interference (EMI).

- **Decoupling:** The standard decoupler for external power is a 100 µF capacitor. Supplementary 0.1 µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device, to reduce high frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve EMC performance. Decoupling can be both capacitive and inductive.

- **Component Position:** You should separate the different circuits on the PCB according to their EMI contribution. This helps reduce cross-coupling on the PCB. For example, separate noisy high current circuits, low voltage circuits, and digital components.

- **Signal Routing:** Check the routing of the following signal types to improve EMC performance:
  - Noisy signals, for example signals with fast edge times
  - Sensitive and high impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To increase EMC performance, keep the trace lengths as short as possible, and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route traces near or parallel to other noisy and sensitive traces.

  For more information, several references are available:

- The Circuit Designer's Companion, Second Edition, (EDN Series for Design Engineers) by Tim Williams
- PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science), by Bruce R. Archambeault and James Drewniak
- Printed Circuits Handbook (McGraw Hill Handbooks), by Darwin Edwards, Clyde F. Coombs, Jr.,
- EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple, by Mark I. Montrose
- Signal Integrity Issues and Printed Circuit Board Design, by Douglas Brooks
- Cypress AN80994, PSoC 3, PSoC 4, and PSoC 5LP EMC Best Practices
- Application Note: *Board Level Assembly and Reliability Considerations for QFN Type Packages* – Amkor Technology, September 2008 http://www.amkor.com/go/packaging/all-packages/microleadframeandreg

B Appendix B – Schematic Checklist

Each item in the following checklist should be confirmed (C) or noted as not applicable (NA). For example, if you choose a single power domain for your system, you can mark all the items related to multiple power domains as NA.

Catalog	Item	C / NA	Remark
Power	Is the voltage at the AV_{CC} pin always greater than or equal to the voltage at any of the V_{CC} pins?		
	If there are multiple power domains on the PCB, have the V_{CC} pins been assigned accordingly?		
	Are the correct capacitors connected to each AV_{CC} and V_{CC} pin? Do the capacitors have appropriate working voltage and DC bias specifications?		
	Are the power voltage ramp-up speeds limited?		
	Are the total I/O currents less than the current limit?		
	Does your package selection have the correct thermal resistance for your anticipated total chip power?		
I/O Pins	Have your pin selections been optimized for your PCB / application? See I/O Pins and Device Reset.		
	Are all device pins marked “do not use” (DNU) left unconnected and floating?		
	Are all unused I/O pins left floating and software programmed to outputs driving a low signal?		
	Have series resistors been added to all pins being routed off the PCB, for ESD protection?		
Reset	Is the reset pin (INITX) connection in accordance with Device Reset?		
Programming and Debugging	Are the JTAG or SWD pin connections in accordance with Programming and Debug?		
Oscillators	Are the crystals and external components connected correctly?		
Analog Connections	Are bypass capacitors connected to the correct pins?		
	Are analog power connections isolated from digital power?		
	Is a single point used for gathering all analog ground returns?		
PCB	Does your PCB layout implement the techniques suggested in Appendix A – PCB Layout Tips and I/O Pin Selection?		

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**	5057349	JPWI	02/09/2016	New Application Note
*A	5530542	JETT	11/23/2016	Fix a broken link; minor edits and update to latest templates
*B	5715437	AESATMP9	04/27/2017	Updated logo and copyright.

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