

This Customer Design Review Supplement is provided to prevent problems that may arise in the system development of MB90920 series. A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items. We will recommend this Customer Design Review Supplement used to be filed as a review results.

Item	Check	Reason for checking	Result	Remark	Update
CAN	HP-FAQ	Do you know that a reception error cannot lead to a bus-off status?	Yes / No		2008/1/10
CAN	HP-FAQ	For standard ID processing at reception of CAN data, is filtering processing implemented for IDs other than the target IDs?	Yes / No		2008/1/10
CAN	HP-FAQ	Is the error status judged only with the error counter?	Yes / No		2008/1/10
CAN	HP-FAQ	Do you know that when the reception error count reads REC of 128 or more and a normal reception occurs, the REC is changed to the value between 119 and 127.	Yes / No		2008/1/10
CAN	HP-FAQ	Do you know that a glitch can be output to the CAN TX pin?	Yes / No		2008/1/10
CAN	HP-FAQ	Is a high-precision oscillator used to execute high-speed CAN data communications?	Yes / No		2008/1/10
CAN	HALT bit clear timing	Before clearing HALT bit, is it confirmed that the value of HALT bit is "1"?	Yes / No		2008/1/10
CAN	Implementation of RMW instruction to CSR	Do you know that the implementation of RMW instruction to CSR is restricted by the manual?	Yes / No		2008/1/10
CAN	Processing for DLC of 9 and higher	Is the software fail-safe in anticipation of a DLC of 9 and higher for DLC judgment at data reception?	Yes / No		2008/1/10
CAN	IDR	Is the message buffer (BVAL) enabled without setting ID in "ID"?	Yes / No		2008/1/10
CAN	CAN baud rate	Are settings made considering the conditions of all segments for determining the CAN baud rate?	Yes / No	Confirm whether the following conditions in the manual are met: TSEG1 >= 2TQ, TSEG1 >= RSJW, TSEG2 >= 2TQ, TSEG2 >= RSJW	2008/1/10
CAN	Reception interruption processing	Confirm that RC is completely cleared in all message buffers in the reception interruption routine of CAN.	Yes / No		2008/1/10
CPU	Watchdog	Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings and the intermittent operation mode considered?)	Yes / No		2008/1/10
CPU	Watchdog	When using the built-in watchdog timer during sub-clock operation, is the watchdog clock resource set so that the clock timer is used (WDCS=0)?	Yes / No		2008/1/10
CPU	External reset IC	When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered?	Yes / No	Confirm the guaranteed operation voltage range in the data sheet.	2008/1/10
CPU	External reset	Does the reset range meet the Spansion's standard?	Yes / No		2008/1/10
CPU	Power-on reset	Is the standard on electrical characteristics concerning power-on reset being met?	Yes / No	Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input).	2008/1/10

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CPU	Reset cause bits	When using the watchdog timer control (WDT0) register's reset cause bits, is the WDT0 register read once by using the program default setting, followed by the clearing of the reset cause bits?	The default values of all reset cause bits are undefined. Accordingly, in order to clear all reset cause bits, ensure that the WDT0 register is read once before using it.	Yes / No	Applied only when reset cause bits are used.	2008/1/10
CPU	Main(PLL) → Sub → Main(PLL)*	In CPU status transitions, during status transition of Main or PLL → Sub → Main or PLL, is it verified, prior to transition to another status, that the CPU is transferred to statuses set by using the MCM and SCM bits?	Between the "0" write (Sub) and the "1" write (Main) to SCS, "1" write can be ignored within one sub clock cycle. When switching SCS, modify SCS only after verifying that transition to the status expected in SCM occurs.	Yes / No	Refer to the explanation of the SCM bit in the manual.	2008/1/10
CPU	Switching of the internal clock operation mode	When switching the internal clock operation mode (PLL, main, sub), is the operation mode switched to another mode?	If, when switching the internal clock operation mode (PLL, main, sub), the operation mode is switched to another mode, problems may arise when switching the mode (Behavior such as attempting to transition to the PLL mode during main clock oscillation stabilization wait time in transition from sub-clock oscillation to main clock oscillation is prohibited).	Yes / No	See the explanation of the MCS and SCM bits in the manual.	2008/1/10
CPU	Sub clock oscillation stabilization wait	Has the state transition from the main mode to the sub clock mode taken place while the sub clock oscillation is still unstable?	The sub clock needs longer oscillation stabilization time than the main clock does. Thus, before the state transition to the sub clock mode takes place, oscillation of the sub clock needs to stabilize.	Yes / No	Only when the sub clock is used	2008/1/10
CPU	Main clock oscillation stabilization wait	Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator?	CPU may be run before oscillation has stabilized.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2008/1/10
CPU	Transition to standby mode	Do you know the notes to be followed at transition to standby mode?	For transition to standby mode, to access the low power consumption mode control register, add the following commands. MOV LPMCR,#xxh ;standby mode transition com. NOP NOP JMP S+3 ;jump to next com. For details, see the hardware manual. (See the chapter on low power consumption mode.)	Yes / No	Applied only when standby mode is used.	2008/1/10
CPU	Time-base timer	Is the time-base timer interrupt prohibited during transition from the main mode to the PLL mode or from the main mode to the sub mode?	Since the time-base timer is used as a counter of the oscillation stabilization wait time and PLL clock stabilization wait time, the counter is automatically cleared in the following state transitions: - Transition from the main clock mode to the PLL clock mode - Transition to the sub clock mode - Transition to the stop mode When the time-base timer interrupt is not prohibited during state transition from the main mode to the PLL mode or from the main mode to the sub-clock mode, an unintended time-base timer interrupt may occur.	Yes / No		2008/1/10
Peripheral	A/D converter	Is analog impedance the analog impedance described in the datasheet or less. When the analog impedance is higher, it is required to set the sample hold time longer or install an external capacitor of approximate 0.1 uF.	When the analog impedance is higher, the sampling time of analog data may become shorter than required time.	Yes / No	Only when A/D converter is used.	2008/1/10
Peripheral	A/D converter	Is voltages of AVR and AVCC are sufficiently stable?	To separate power supplies of analog system and digital system, a reactance device may be mounted in AVR and AVCC. In this case, it is recommended to configure the circuit by adding a capacitor of some micro F so that sufficient power is supplied at A/D start.	Yes / No	Only when A/D converter is used.	2008/1/10
Peripheral	A/D converter	Is analog sampling time sufficiently long?	When analog input impedance is larger, a glitch may occur at analog input pin. The glitch is determine by the analog impedance and time constant of internal capacitance. When sample hold time is shorter, sample hold value may be affected by the glitch. Because the influence of the glitch is different between FLASH product and MASK product, it is recommended to set a sufficient sample hold time when the analog input impedance is larger.	Yes / No	Only when the analog input impedance used is larger than the analog input impedance recommended by the Data Sheet.	2008/1/10
Peripheral	A/D converter	Are the completion and start of A/D conversion implemented at the same time?	When the completion and start of A/D conversion are implemented at the same time, the later operation, the start of the A/D conversion, may be ignored.	Yes / No	Only when A/D conversion is started during A/D conversion performed.	2008/1/10
Peripheral	A/D converter	Is the analog input enable register(ADER) set to port input mode, when A/D converter is used?	When the port input mode is set with the ADER and A/D input (voltage of medium potential) is implemented, through current flows in CMOS input circuit of I/O port and the current consumption is increased.	Yes / No	Only when A/D converter is used.	2008/1/10

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Peripheral	A/D converter	When enabling the ADTG input, is the corresponding bit of the port direction register set to "0" (initial value)?	To enable the ATDG input, set the corresponding bit of the port direction register to 0 (initial value).	Yes / No	Only when the A/D trigger input (ADTG) is used	2008/1/10
Peripheral	Interrupt	Is the interrupt vector processing of an exceptional interrupt performed?	Runaway may be caused when an undefined instruction is executed due, for example, to runaway.	Yes / No	When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended.	2008/1/10
Peripheral	Interrupt	Is processing of an unused interrupt vector performed?	Runaway may be caused when an unused interrupt occurs due, for example, to runaway.	Yes / No	When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended	2008/1/10
Peripheral	I/O port	Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output?	Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports.	Yes / No		2008/1/10
Peripheral	I/O port	When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register?	Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first.	Yes / No		2008/1/10
Peripheral	Flash	Do you know that FLASH memory cannot be read while writing to/deleting (chip deletion/sector deletion) FLASH memory?	While writing to/deleting (chip deletion/sector deletion) FLASH memory, no interrupt vector on FLASH memory cannot be read, either. Thus, remember that no interrupt processing can be performed while writing/deleting.	Yes / No	Only when FLASH memory is written by the user	2008/1/10
Peripheral	Flash	When users are allowed to write to FLASH memory in user programming mode, is the hardware sequence flag used to control writing to FLASH memory?	Since the FMCS register cannot be used to check for write/delete errors, it is recommended to use the hardware sequence flag to control writing to/deleting FLASH memory.	Yes / No	Only when FLASH memory is written to by the user	2008/1/10
Peripheral	Flash	Do you use Flash memory with Flash security in mind?	The Flash microcomputer of this product contains a Flash security circuit. When the protected data of "01H" is written to the specified address, no data can be written to flash memory without deleting the whole chip memory.	Yes / No	For details, see the chapter of Flash memory of the hardware manual.	2008/1/10
Others	General	Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Spansion? When any of them does not satisfy the standards, is any special guarantee considered and supported?	When not used within the guarantee range, no product guarantee can be provided.	Yes / No	Check the guaranteed operation range in the data sheet.	2008/1/10
Others	General	When a special guarantee is considered, is a notification form returned to the Sales Dept. after affixing a "confirmation stamp (No problem, Problem found) in the reply)" on the notification form?	If a special guarantee is provided, test changes may be needed. Thus, make sure to return the notification form before ROM release.	Yes / No	Since it may take up to several months to deal with test changes, they may not be dealt with when the notification form is returned just before ROM release.	2008/1/10
Noise reduction measures and others	Oscillation	Is oscillation matching data of mass-produced products obtained?	Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2008/1/10
Noise reduction measures and others	Mode(MOD) pin	Is the same level for processing of the MOD pin ensured even while executing instructions?	The level of the MOD pin may be read incorrectly (When a high-impedance resistor is used for treating the MOD pin, the MOD pin level may not be ensured due to noise).	Yes / No	When external noise tends to propagate to the MOD pin, it is recommended to take countermeasures against static electricity such as connecting a capacitor to the mode pin.	2008/1/10
Noise reduction measures and others	Mode(MD) pin	Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect?	The level of the MOD pin may be read incorrectly due to power supply deviation and noise.	Yes / No		2008/1/10
Noise reduction measures and others	Oscillation	When using a crystal oscillator, is an appropriate dumping resistor inserted?	To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2008/1/10
Noise reduction measures and others	Oscillation	Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude?	When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase.	Yes / No	When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise.	2008/1/10

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Noise reduction measures and others	Oscillation	Is the oscillator arranged as close to the chip as possible?	Yes / No	It is recommended to arrange the oscillator as close to the chip as possible?	2008/1/10
Noise reduction measures and others	Vcc, GND	Is consideration given to making Vcc and GND as strong as possible?	Yes / No	To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened).	2008/1/10
Peripheral	Unused pin treatment	Is any unused pin pulled up or pulled down by the resistor of 2 kΩ or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened?	Yes / No		2008/1/10
Noise reduction measures and others	Capacitor	Is the optimum capacitor connected near the chips as a capacitor for reducing noise?	Yes / No		2008/1/10
Noise reduction measures and others	C pin	The capacitance of the smoothing capacitor connected to Vcc is larger than that of the capacitor connected to C pin?	Yes / No		2008/1/10
Noise reduction measures and others	Software	Is the setting made in which Start.asm is linked at first at the development with C language?	Yes / No	Only for the use of Start.asm of Softune.	2008/1/10
Noise reduction measures and others	ESD, latch-up, noise	Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances?	Yes / No	Since it is possible to submit measurement results of Spansion as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them.	2008/1/10
Noise reduction measures and others	Connection of reactance	Is reactance connected directly with power supply?	Yes / No	If reactance is put directly in the power supply of chip, it is necessary to connect capacitor between chip power supply and reactance.	2008/1/10
Noise reduction measures and others	Memory map	Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation?	Yes / No		2008/1/10
Noise reduction measures and others	Bit manipulation instruction	Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register?(Is not RMW instruction executed for the register including write only bit?)	Yes / No	Read-modify-write related instruction is indicated in the instruction list by * in RMW.	2008/1/10
Noise reduction measures and others	Stack usage	Is the maximum usage of stack confirmed?	Yes / No	It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack (Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage).	2008/1/10
Noise reduction measures and others	Operation mode of tools	Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation?	Yes / No		2008/1/10
CPU	PLL -> Sub Run -> PLL	For direct transition to PLL mode following the release of main clock stop status, is the oscillation stabilization wait time of the main clock set longer than the PLL clock wait time?	Yes / No		2015/3/9
CPU	Stop mode	Do you know it is prohibition to transit directly to the stop mode from the PLL mode without passing through the main mode?	Yes / No	Please refer to Customer Information CI703-00001.	2015/3/9