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CAN	HP-FAQ	Do you know that a reception error cannot lead to a bus-off status?	For a software that is developed assuming that reception errors lead to "bus-off" status, however, processing based on such assumption is invalidated.	Yes / No		2007/11/27
CAN	HP-FAQ	For standard ID processing at reception of CAN data, is filtering processing implemented for IDs other than the target IDs?	For non-target IDs (difference between extended format and standard format), other ID data could be included. Example: For some ID data to be processed, the data cannot be received in the processing routine of the target ID.	Yes / No		2007/11/27
CAN	HP-FAQ	In the reception processing routine, is the data processed by using the reception overrun register (ROVRR) instead of invalidating the target message buffer (BVALR)?	"Hit and Away" can occur.	Yes / No		2007/11/27
CAN	HP-FAQ	Is the error status judged only with the error counter?	There are cases where the error status value and the error counter value do not match after the error counter exceeds a count of 256.	Yes / No		2007/11/27
CAN	HP-FAQ	Do you know that when the reception error count reads REC of 128 or more and a normal reception occurs, the REC is changed to the value between 119 and 127.	There is a need to exercise caution with software that relies on the reception error count.	Yes / No		2007/11/27
CAN	HP-FAQ	Do you know that a glitch can be output to the CAN TX pin?	In terms of system operations, this does not bring about any adverse effects. However, you need to know this as information for system inspection purposes.	Yes / No		2007/11/27
CAN	HP-FAQ	Is a high-precision oscillator used to execute high-speed CAN data communications?	As the tolerance of an oscillator depends on the CAN baud rate, normal communication cannot be made when the oscillator's error is larger than the tolerance.	Yes / No		2007/11/27
CAN	Hit and Away	Is the control of message buffer prohibited processing (BVALR) for the relevant buffer during message reception or while securing message transmission permission?	A "Hit and Away" bypass can occur.	Yes / No		2007/11/27
CAN	HALT bit clear timing	Before clearing HALT bit, is it confirmed that the value of HALT bit is "1"?	When HALT bit is cleared at the timing when the value of HALT bit is changing from "0" to "1," the unconformity of internal operation may be caused.	Yes / No		2007/11/27
CAN	Implementation of RMW instruction to CSR	Do you know that the implementation of RMW instruction to CSR is restricted by the manual?	Because the implementation of RMW instruction to CSR is restricted, the development of a software without RMW instruction implementation is recommended.	Yes / No		2007/11/27
CAN	Processing for DLC of 9 and higher	Is the software fail-safe in anticipation of a DLC of 9 and higher for DLC judgment at data reception?	The CAN standard stipulates DLC of 8 and less. However there is no specification for transmission at DLC of 9 and higher. Accordingly, to avoid problems for transmission of DLC of 9 and higher, we recommend considering the fail-safe approach in developing a software.	Yes / No		2007/11/27
CAN	IDR	Is the message buffer (BVAL) enabled without setting ID in "ID"?	Because the intial value of IDR setting ID is unstable, when the target image buffer is eabled without setting the value, the data of undefined ID may be recieved	Yes / No		2007/11/27
CAN	CAN baud rate	Are settings made considering the conditions of all segments for determining the CAN baud rate?	Normal CAN sending and reception cannot occur.	Yes / No	Confirm whether the following conditions in the manual are met: TSEG1 >= 2TQ, TSEG1 >= RSJW, TSEG2 >= 2TQ, TSEG2 >= RSJW	2007/11/27
CAN	Acceptance mask register switching	Is the acceptance mask register changed while HALT is "0" ?	Unless the acceptance mask register is changed after setting HALT to "1" and invalidating the message buffer, "Hit and Away" can occur.	Yes / No		2007/11/27
CAN	Reception interruption processing	Confirm that RC is completly cleared in alll message buffers in the reception interruption routine of CAN.	It is recommended that the software development is implemented so that the interrupt flag (CR) of an image buffer that is indicated not to be received in the reception interrupt routine of CAN is also cleared considering a fall-safe.	Yes / No		2007/11/27
CPU	uDMAC	When using the uDMAC, is CAN operation stopped?	Normal uDMAC sending cannot occur.	Yes / No	Refer to "uDMAC Bus error".	2007/11/27
CPU	Watchdog	Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings and the intermittent operation mode considered?)	When the watchdog reset interval is not sufficient, whether a program is proceeding normally cannot be detected.	Yes / No		2007/11/27
CPU	Watchdog	When using the built-in watchdog timer during sub-clock operation, is the watchdog clock resource set so that the clock timer is used (WDCS=0)?	When using the built-in watchdog timer during sub-clock operation, if the time-base timer is set as the watchdog clock resource (WDCS=1), no watchdog may be generated during sub-clock operation.	Yes / No		2007/11/27

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CPU	External reset IC	When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered?	When no reset within the guaranteed operation voltages is entered, a malfunction may occur.	Yes / No	Confirm the guaranteed operation voltage range in the data sheet.	2007/11/27
CPU	External reset	Does the reset range meet the Fujitsu's standard?	When the reset range does not meet the Fujitsu's standard, recovery cannot be implemented.	Yes / No		2007/11/27
CPU	Power-on reset	Is the standard on electrical characteristics concerning power-on reset being met?	Powering on without meeting the power-on reset standard may result in the execution of commands by CPU without the power-on reset implemented normally.	Yes / No	Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input).	2007/11/27
CPU	Reset cause bits	When using the watchdog timer control (WDTC) register's reset cause bits, is the WDTC register read once by using the program default setting, followed by the clearing of the reset cause bits?	The default values of all reset cause bits are undefined. Accordingly, in order to clear all reset cause bits, ensure that the WDTC register is read once before using it.	Yes / No	Applied only when reset cause bits are used.	2007/11/27
CPU	Main(PLL) -> Sub -> Main(PLL)*	In CPU status transitions, during status transition of Main or PLL -> Sub -> Main or PLL, is it verified, prior to transition to another status, that the CPU is transferred to statuses set by using the MCM and SCM bits?	Between the "0" write (Sub) and the "1" write (Main) to SCS, "1" write can be ignored within one sub clock cycle. When switching SCS, modify SCS only after verifying that transition to the status expected in SCM occurs.	Yes / No	Refer to the explanation of the SCM bit in the manual.	2007/11/27
CPU	PLL -> Sub(Stop) -> PLL	For direct transition to PLL mode following the release of main clock stop status, is the oscillation stabilization wait time of the main clock set longer than the PLL clock wait time?	When transition to PLL mode recurs after transition from PLL mode to sub RUN (or STOP) status, the oscillation stabilization wait time of the main clock should be set longer than the PLL clock wait time.	Yes / No		2007/11/27
CPU	Switching of the internal clock operation mode	When switching the internal clock operation mode (PLL, main, sub), is the operation mode switched to another mode?	If, when switching the internal clock operation mode (PLL, main, sub), the operation mode is switched to another mode, problems may arise when switching the mode (Behavior such as attempting to transition to the PLL mode during main clock oscillation stabilization wait time in transition from sub-clock oscillation to main clock oscillation is prohibited).	Yes / No	See the explanation of the MCS and SCM bits in the manual.	2007/11/27
CPU	Subclock oscillation stabilization wait	Has the state transition from the main mode to the subclock mode taken place while the subclock oscillation is still unstable?	The subclock needs longer oscillation stabilization time than the main clock does. Thus, before the state transition to the subclock mode takes place, oscillation of the subclock needs to stabilize.	Yes / No	Only when the subclock is used	2007/11/27
CPU	PLL->Main	In software development, is attention given to the timing of the changes in the CPU's operation speed during the status transition of Main -> PLL -> Main -> PLL when such processing speed does change? (Is consideration given to the need to wait for eight cycles between MCS "1" write and "0" write?)	Within the eight cycles between MCS "1" write (Main) and "0" write (PLL), "0" write can be ignored.	Yes / No	Refer to the explanation of the MSC bit in the manual.	2007/11/27
CPU	Main clock oscillation stabilization wait	Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator?	CPU may be run before oscillation has stabilized.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
CPU	Transition to standby mode	Do you know the notes to be followed at transition to standby mode?	For transition to standby mode, to access the low power consumption mode control register, add the following commands. MOV LPMCR,#xxh ;standby mode transition com. NOP NOP JMP S+3 ;jump to next com. For details, see the hardware manual. (See the chapter on low power consumption mode.)	Yes / No	Applied only when standby mode is used.	2007/11/27
CPU	Time-base timer	Is the time-base timer interrupt prohibited during transition from the main mode to the PLL mode or from the main mode to the submode?	Since the time-base timer is used as a counter of the oscillation stabilization wait time and PLL clock stabilization wait time, the counter is automatically cleared in the following state transitions: - Transition from the main clock mode to the PLL clock mode - Transition to the subclock mode - Transition to the stop mode When the time-base timer interrupt is not prohibited during state transition from the main mode to the PLL mode or from the main mode to the sub-clock mode, an unintended time-base timer interrupt may occur.	Yes / No		2007/11/27
Peripheral	A/D converter	Is analog impedance the analog impedance described in the datasheet or less. When the analog impedance is higher, it is required to set the sample hold time longer or install an external capacitor of approximate 0.1 uF.	When the analog impedance is higher, the sampling time of analog data may become shorter than required time.	Yes / No	Only when A/D converter is used.	2007/11/27
Peripheral	A/D converter	Is voltages of AVR and AVCC are sufficiently stable?	To separate power supplies of analog system and digital system, a reactance device may be mounted in AVR and AVCC. In this case, it is reconmmended to configure the circuit by adding a capacitor of some micro F so that sufficient power is supplied at A/D start.	Yes / No	Only when A/D converter is used.	2007/11/27

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Peripheral	A/D converter	Is analog sampling time sufficiently long?	When anolog input impedance is larger, a glitch may occur at analog input pin.. The glitch is determine by the analog impedance and time constant of internal capacitance. When sample hold time is shorter, sample hold value may be affected by the glitch. Because the influence of the glitch is different beteween FLASH product and MASK product, it is recommmended to set a sufficient sample hold time when the analog input impedance is larger.	Yes / No	Only when the analog input impedance used is larger than the analog input impedance recommended by th Data Sheet.	2007/11/27
Peripheral	A/D converter	Are the completion and start of A/D conversion implemented at the same time?	When the comletion and start of A/D conversion are implemented at the same time, the later operation, the start of the A/D conversion, may be ignored.	Yes / No	Only when A/D conversion is started during A/D conversion performed.	2007/11/27
Peripheral	A/D converter	Is the analog input enable register(ADER) set to port input mode, when A/D converter is used?	When the port input mode is set with the ADER and A/D input (voltage of medium potential) is implemented, through current flows in CMOS input circuit of I/O port and the current consumption is increased.	Yes / No	Only when A/D converter is used.	2007/11/27
Peripheral	A/D converter	When the consecutive ADC operation is paused by the data protection function, is the interrupt is cleared?	Normal A/D operation cannot occur.	Yes / No	Refer to "ADC Interrupt error".	2007/11/27
Peripheral	A/D converter	When enabling the ADTG input, is bit 5 of the port 2 direction register (DDR2:000012H) set to "0" (initial value)?	Note that, in contrast to the MB90340 series, ADTG of the MB90350 series is assigned to P25. To enable the ATDG input, set bit5 of the port2 direction register (DDR2:000012H) to 0 (initial value).	Yes / No	Only when the A/D trigger input (ADTG) is used	2007/11/27
Peripheral	Interrupt	Is the interrupt vector processing of an exceptional interrupt performed?	Runaway may be caused when an undefined instruction is executed due, for example, to runaway.	Yes / No	When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended.	2007/11/27
Peripheral	Interrupt	Is processing of an unused interrupt vector performed?	Runaway may be caused when an unused interrupt occurs due, for example, to runaway.	Yes / No	When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended	2007/11/27
Peripheral	External address output register	When using in external bus mode, has "1" been written to bit6 and bit7 of HARC?	When using in external bus mode, the address A22 and A23 pins do not exist. Thus, be sure to write "1" to bit 6 and bit 7 of HARC at the start of user programs after the reset sequence.	Yes / No	There is no need to confirm this item when the software for the MB90340 series is not used for software development of the MB90350 series.	2007/11/27
Peripheral	I/O port	Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output?	Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports.	Yes / No		2007/11/27
Peripheral	I/O port	When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register?	Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first.	Yes / No		2007/11/27
Peripheral	Port direction register setting	When the software for the MB90340 series is used for software development of the MB90350 series, is any register that is not available in the MB90350 series accessed?	When DDR of P26, P27, P70 to P77, P80 to P87, P90 to P97, and PA0 to PA1 that are not available in the MB90350 series is set for output, tools may not work normally. Thus, set the target DDR for input (=0).	Yes / No	There is no need to confirm this item when the software for the MB90340 series is not used for software development of the MB90350 series.	2007/11/27
Peripheral	I2C	When using the I2C bus, are the dual-purpose pins P44, P45 used by setting them for input (DDR=0)?	When RMW instruction is executed on the same series (P44 to P45) as the dual-pin (P44/SDA0, P45/SCL0) with the I2C bus and the dual-purpose pin is set for output, PDR44, 45 may change due to execution of the RMW instruction. When the I2C bus is prohibited in this state, the changed value of PDR44, 45 is output to a port.	Yes / No	Only when I2C is used	2007/11/27
Peripheral	I2C	Is INT bit cleared at the end of the interrupt routine processing?	SCL pin = LOW output in a state of "INT bit = 1" and making the SCL pin open when INT bit is cleared are specified. Therefore, it is necessary to perform I2C data processing in a state of "INT bit = 1" (SCL pin = LOW) and to clear INT bit (open SCL pin) when it becomes ready for sending or receiving the next piece of data.	Yes / No		2007/11/27
Peripheral	I2C	Is AL bit confirmed after setting the master mode (writing "1" to MSS bit)?	If the master mode is set ("1" is written to MSS bit) when the SCL pin or SDA pin is in "LOW" state, it becomes impossible to generate a start condition and output the SCL clock so that no transfer end interrupt (INT bit) occurs. Thus, after setting the master mode (writing "1" to MSS bit), wait for the 3 bit data transfer time and then check AL bit for this state (It takes the 3 bit transfer time after setting MSSbit = "1" for a change of AL bit).	Yes / No	Only when I2C is used	2007/11/27

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Peripheral	I2C	Is any general call address sent in multimaster mode?	Since this product prohibits the kind of use in which general call addresses are sent and then lost in arbitration, it is recommended not to send any general call address in multi master mode.	Yes / No	Only when I2C is used	2007/11/27
Peripheral	Flash	Do you know that FLASH memory cannot be read while writing to/deleting (chip deletion/sector deletion) FLASH memory?	While writing to/deleting (chip deletion/sector deletion) FLASH memory, no interrupt vector on FLASH memory cannot be read, either. Thus, remember that no interrupt processing can be performed while writing/deleting.	Yes / No	Only when FLASH memory is written by the user	2007/11/27
Peripheral	Flash	When users are allowed to write to FLASH memory in user programming mode, is the hardware sequence flag used to control writing to FLASH memory?	Since the FMCS register cannot be used to check for write/delete errors, it is recommended to use the hardware sequence flag to control writing to/deleting FLASH memory.	Yes / No	Only when FLASH memory is written to by the user	2007/11/27
Others	General	Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Fujitsu? When any of them does not satisfy the standards, is any special guarantee considered and supported?	When not used within the guarantee range, no product guarantee can be provided.	Yes / No	Check the guaranteed operation range in the data sheet.	2007/11/27
Others	General	When a special guarantee is considered, is a notification form returned to the Sales Dept. after affixing a "confirmation stamp ((No problem, Problem found) in the reply)" on the notification form?	If a special guarantee is provided, test changes may be needed. Thus, make sure to return the notification form before ROM release.	Yes / No	Since it may take up to several months to deal with test changes, they may not be dealt with when the notification form is returned just before ROM release.	2007/11/27
Noise reduction measures and others	Oscillation	Is oscillation matching data of mass-produced products obtained?	Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
Noise reduction measures and others	Mode(MOD) pin	Is the same level for processing of the MOD pin ensured even while executing instructions?	The level of the MOD pin may be read incorrectly (When a high-impedance resistor is used for treating the MOD pin, the MOD pin level may not be ensured due to noise).	Yes / No	When external noise tends to propagate to the MOD pin, it is recommended to take countermeasures against static electricity such as connecting a capacitor to the mode pin.	2007/11/27
Noise reduction measures and others	Mode(MD) pin	Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect?	The level of the MOD pin may be read incorrectly due to power supply deviation and noise.	Yes / No		2007/11/27
Noise reduction measures and others	Oscillation	When using a crystal oscillator, is an appropriate dumping resistor inserted?	To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
Noise reduction measures and others	Oscillation	Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude?	When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase.	Yes / No	When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise.	2007/11/27
Noise reduction measures and others	Oscillation	Is the oscillator arranged as close to the chip as possible?	CPU runaway due to external noise may be presumed.	Yes / No	It is recommended to arrange the oscillator as close to the chip as possible?	2007/11/27
Noise reduction measures and others	Vcc, GND	Is consideration given to making Vcc and GND as strong as possible?	Problems of unnecessary radiation noise and CPU runaway due to external noise may be presumed.	Yes / No	To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened).	2007/11/27
Peripheral	Unused pin treatment	Is any unused pin pulled up or pulled down by the resistor of 2 kΩ or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened?	When an unused pin is treated without a resistor and the port level opposite to the processing level is output due to CPU runaway, problems such as latch-up may arise.	Yes / No		2007/11/27
Noise reduction measures and others	Capacitor	Is the optimum capacitor connected near the chips as a capacitor for reducing noise?	The capacitor connected to reduce noise may not work with reactance components of interconnect (Measures that take noise components into account are needed).	Yes / No		2007/11/27
Noise reduction measures and others	C pin	The capacitance of the smoothing capacitor connected to Vcc is larger than that of the capacitor connected to C pin?	When the capacitance of the smoothing capacitor is smaller, the internal regulator may become unstable.	Yes / No		2007/11/27

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Noise reduction measures and others	Software	Is the setting made in which Start.asm is linked at first at the development with C language?	In Start.asm of Softune, the link is generated automatically at the begining of the address where RAM is cleared. Therefore, when Start.asm is used, it is necessary to set the order of the link at first because the address information becomes wrong if it is not set.	Yes / No	Only for the use of Start.asm of Softune.	2007/11/27
Noise reduction measures and others	ESD, latch-up, noise	Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances?	Since the resistances against ESD, latch-up, and noise of Flash products and those of mask products are different, it is recommended to use mass-produced products to evaluate ESD and latch-up resistance.	Yes / No	Since it is possible to submit measurement results of Fujitsu as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them.	2007/11/27
Noise reduction measures and others	Connection of reactance	Is reactance connected directly with power supply?	The characteristic of internal requlator might not be obtained by the reactance element.	Yes / No	If reactance is put directly in the power supply of chip , it is necessary to conect capacitor between chip power supply and reactance.	2007/11/27
Noise reduction measures and others	Memory map	Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation?	The built-in memory amount of the EVA chip for evaluation and that of the Flash and mask chip are different. Therefore, the actual chips may not work even if normal operation is confirmed by using a tool.	Yes / No		2007/11/27
Noise reduction measures and others	Bit manipulation instruction	Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register?(Is not RMW instruction executed for the register including write only bit?)	The instruction may not be executed normally, resulting in unintended data being written.Since, when a read-modify-write related instruction (such as SETB) is used on a register with write-only bits, the read value of the write-only bit is undefined, problems may be caused (When safety use of the read-modify-write instructions is described in the manual for a register, no problem will be caused).	Yes / No	Read-modify-write related instruction is indicated in the instruction list by * in RMW.	2007/11/27
Noise reduction measures and others	Stack usage	Is the maximum usage of stack confirmed?	Incorrect estimation of the stack usage could lead to RAM damage.	Yes / No	It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack (Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage).	2007/11/27
Noise reduction measures and others	Operation mode of tools	Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation?	The native mode and debug mode are available as the operation modes of tools. Since the working speed in debug mode is different from the actual working speed, it is recommended to make an evaluation after setting the native mode.	Yes / No		2007/11/27
Noise reduction measures and others	Do not use the Clock Modulation.	Don't you use the Clock-Modulationfunction?	Before CM44-10125-2E Manual deceives the Clock Modulation Function. But it is not available to use this function, which is written in Note.	Yes / No		2008/8/26