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Item		Check	Reason for checking	Result	Remark	Update
CPU	Watchdog	Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings considered?)	When the watchdog reset interval is not sufficient, whether a program is proceeding normally cannot be detected.	Yes / No		2007/11/27
CPU	External reset IC	When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered?	When no reset within the guaranteed operation voltages is entered, a malfunction may occur.	Yes / No	Confirm the guaranteed operation voltage range in the data sheet.	2007/11/27
CPU	External reset	Does the reset range meet the Fujitsu's standard?	When the reset range does not meet the Fujitsu's standard, recovery cannot be implemented.	Yes / No		2007/11/27
CPU	Power-on reset	Is the standard on electrical characteristics concerning power-on reset being met?	Powering on without meeting the power-on reset standard may result in the execution of commands by CPU without the power-on reset implemented normally.	Yes / No	Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input).	2007/11/27
CPU	Reset cause bits	When using the Reset Cause and Clock status (RCCSR/RCCSRC) register's reset cause bits, is the RCCSRC register read once by using the program default setting, followed by the clearing of the reset cause bits?	The default values of all reset cause bits are undefined. Accordingly, in order to clear all reset cause bits, ensure that the RCCSRC register is read once before using it.	Yes / No	Applied only when reset cause bits are used.	2007/11/27
CPU	Subclock oscillation stabilization wait	Has the state transition from the main mode to the subclock mode taken place while the subclock oscillation is still unstable?	The subclock needs longer oscillation stabilization time than the main clock does. Thus, before the state transition to the subclock mode takes place, oscillation of the subclock needs to stabilize.	Yes / No	Only when the subclock is used	2007/11/27
CPU	Main clock oscillation stabilization wait	Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator?	CPU may be run before oscillation has stabilized.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
Peripheral	A/D converter	Is analog impedance the analog impedance described in the datasheet or less. When the analog impedance is higher, it is required to set the sample hold time longer or install an external capacitor of approximate 0.1 uF.	When the analog impedance is higher, the sampling time of analog data may become shorter than required time.	Yes / No	Only when A/D converter is used.	2007/11/27
Peripheral	A/D converter	Is voltages of AVR and AVCC are sufficiently stable?	To separate power supplies of analog system and digital system, a reactance device may be mounted in AVR and AVCC. In this case, it is reconmmended to configure the circuit by adding a capacitor of some micro F so that sufficient power is supplied at A/D start.	Yes / No	Only when A/D converter is used.	2007/11/27
Peripheral	A/D converter	Is analog sampling time sufficiently long?	When anolog input impedance is larger, a glitch may occur at analog input pin.. The glitch is determine by the analog impedance and time constant of internal capacitance. When sample hold time is shorter, sample hold value may be affected by the glitch. Because the influence of the glitch is different beteween FLASH product and MASK product, it is recommmended to set a sufficient sample hold time when the analog input impedance is larger.	Yes / No	Only when the analog input impedance used is larger than the analog input impedance recommended by th Data Sheet.	2007/11/27
Peripheral	A/D converter	Are the completion and start of A/D conversion implemented at the same time?	When the comletion and start of A/D conversion are implemented at the same time, the later operation, the start of the A/D conversion, may be ignored.	Yes / No	Only when A/D conversion is started during A/D conversion performed.	2007/11/27
Peripheral	A/D converter	Is the analog input enable register(ADER) set to port input mode, when A/D converter is used?	When the port input mode is set with the ADER and A/D input (voltage of medium potential) is implemented, through current flows in CMOS input circuit of I/O port and the current consumption is increased.	Yes / No	Only when A/D converter is used.	2007/11/27
Peripheral	A/D converter	When the consecutive ADC operation is paused by the data protection function, is the interrupt is cleared?	Normal A/D operation cannot occur.	Yes / No	Refer to "ADC Interrupt error".	2007/11/27
Peripheral	Interrupt	Is the interrupt vector processing of an exceptional interrupt performed?	Runaway may be caused when an undefined instruction is executed due, for example, to runaway.	Yes / No	When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended.	2007/11/27
Peripheral	Interrupt	Is processing of an unused interrupt vector performed?	Runaway may be caused when an unused interrupt occurs due, for example, to runaway.	Yes / No	When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended	2007/11/27
Peripheral	I/O port	Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output?	Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports.	Yes / No		2007/11/27

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Peripheral	I/O port	When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register?	Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first.	Yes / No		2007/11/27
Peripheral	Flash	Do you know that FLASH memory cannot be read while writing to/deleting (chip deletion/sector deletion) FLASH memory?	While writing to/deleting (chip deletion/sector deletion) FLASH memory, no interrupt vector on FLASH memory cannot be read, either. Thus, remember that no interrupt processing can be performed while writing/deleting.	Yes / No	Only when FLASH memory is written by the user	2007/11/27
Peripheral	Flash	When users are allowed to write to FLASH memory in user programming mode, is the hardware sequence flag used to control writing to FLASH memory?	Since the FMCS register cannot be used to check for write/delete errors, it is recommended to use the hardware sequence flag to control writing to/deleting FLASH memory.	Yes / No	Only when FLASH memory is written to by the user	2007/11/27
Others	General	Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Fujitsu? When any of them does not satisfy the standards, is any special guarantee considered and supported?	When not used within the guarantee range, no product guarantee can be provided.	Yes / No	Check the guaranteed operation range in the data sheet.	2007/11/27
Others	General	When a special guarantee is considered, is a notification form returned to the Sales Dept. after affixing a "confirmation stamp ((No problem, Problem found) in the reply)" on the notification form?	If a special guarantee is provided, test changes may be needed. Thus, make sure to return the notification form before ROM release.	Yes / No	Since it may take up to several months to deal with test changes, they may not be dealt with when the notification form is returned just before ROM release.	2007/11/27
Noise reduction measures and others	Oscillation	Is oscillation matching data of mass-produced products obtained?	Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
Noise reduction measures and others	Mode(MD) pin	Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect?	The level of the MOD pin may be read incorrectly due to power supply deviation and noise.	Yes / No		2007/11/27
Noise reduction measures and others	Oscillation	When using a crystal oscillator, is an appropriate dumping resistor inserted?	To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.	2007/11/27
Noise reduction measures and others	Oscillation	Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude?	When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase.	Yes / No	When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise.	2007/11/27
Noise reduction measures and others	Oscillation	Is the oscillator arranged as close to the chip as possible?	CPU runaway due to external noise may be presumed.	Yes / No	It is recommended to arrange the oscillator as close to the chip as possible?	2007/11/27
Noise reduction measures and others	Vcc, GND	Is consideration given to making Vcc and GND as strong as possible?	Problems of unnecessary radiation noise and CPU runaway due to external noise may be presumed.	Yes / No	To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened).	2007/11/27
Peripheral	Unused pin treatment	Is any unused pin pulled up or pulled down by the resistor of 2 kΩ or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened?	When an unused pin is treated without a resistor and the port level opposite to the processing level is output due to CPU runaway, problems such as latch-up may arise.	Yes / No		2007/11/27
Noise reduction measures and others	Capacitor	Is the optimum capacitor connected near the chips as a capacitor for reducing noise?	The capacitor connected to reduce noise may not work with reactance components of interconnect (Measures that take noise components into account are needed).	Yes / No		2007/11/27
Noise reduction measures and others	C pin	The capacitance of the smoothing capacitor connected to Vcc is larger than that of the capacitor connected to C pin?	When the capacitance of the smoothing capacitor is smaller, the internal regulator may become unstable.	Yes / No		2007/11/27
Noise reduction measures and others	Software	Is the setting made in which Start.asm is linked at first at the development with C language?	In Start.asm of Softune, the link is generated automatically at the begining of the address where RAM is cleared. Therefore, when Start.asm is used, it is necessary to set the order of the link at first because the address information becomes wrong if it is not set.	Yes / No	Only for the use of Start.asm of Softune.	2007/11/27

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Noise reduction measures and others	ESD, latch-up, noise	Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances?	Since the resistances against ESD, latch-up, and noise of Flash products and those of mask products are different, it is recommended to use mass-produced products to evaluate ESD and latch-up resistance.	Yes / No	Since it is possible to submit measurement results of Fujitsu as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them.	2007/11/27
Noise reduction measures and others	Connection of reactance	Is reactance connected directly with power supply?	The characteristic of internal requlator might not be obtained by the reactance element.	Yes / No	If reactance is put directly in the power supply of chip , it is necessary to conect capacitor between chip power supply and reactance.	2007/11/27
Noise reduction measures and others	Memory map	Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation?	The built-in memory amount of the EVA chip for evaluation and that of the Flash and mask chip are different. Therefore, the actual chips may not work even if normal operation is confirmed by using a tool.	Yes / No		2007/11/27
Noise reduction measures and others	Bit manipulation instruction	Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register?(Is not RMW instruction executed for the register including write only bit?)	The instruction may not be executed normally, resulting in unintended data being written.Since, when a read-modify-write related instruction (such as SETB) is used on a register with write-only bits, the read value of the write-only bit is undefined, problems may be caused (When safety use of the read-modify-write instructions is described in the manual for a register, no problem will be caused).	Yes / No	Read-modify-write related instruction is indicated in the instruction list by * in RMW.	2007/11/27
Noise reduction measures and others	Stack usage	Is the maximum usage of stack confirmed?	Incorrect estimation of the stack usage could lead to RAM damage.	Yes / No	It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack(Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage).	2007/11/27
Noise reduction measures and others	Operation mode of tools	Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation?	The native mode and debug mode are available as the operation modes of tools. Since the working speed in debug mode is different from the actual working speed, it is recommended to make an evaluation after setting the native mode.	Yes / No		2007/11/27
CPU	SCEQ.SCWEQ	Don't you use SCEQ and SCWEQ instructions with the assembly language?	SCEQ/SCWEQ instructions does not work reliable together with interrupts. Please do not use SCEQ/SCWEQ instructions or do not allow interrupts during the use of SCEQ/SCWEQ instructions.	Yes / No	There is no problem in case of using only the C language.	2010/8/10
CPU	String instruction and WBTC,WBTS	Don't you use string instructions(MOVS, MOVSD, SCEQ, SCEQD, FILS, MOVSW, MOVSWD,SCWEQ, SCWEQD, FILSW) or WBTC,WBTS with the assembly language?	It may show different behavior when interrupt is disabled less than 4 CPU clock cycles before string instructions(MOVS, MOVSD, SCEQ, SCEQD, FILS, MOVSW, MOVSWD,SCWEQ, SCWEQD, FILSW) or WBTC,WBTS. Please implement the program not to use these instruction, or please ensure more than 4 CPU clock cycles in case of disabling interrupt before these instructions.	Yes / No	There is no problem in case of using only the C language.	2010/8/10
CPU	MOVS/I,MOVSW/I	Don't you use MOVS/I,MOVSW/I when the source and destination areas are overlapping with the assembly language?	If the source and destination areas are overlapping before execution of the instructions MOVS and MOVSW, it may show different behavior with respect to the instruction execution rules. Please change AH and bank registers latest 3 instructions before MOVS/I, MOVSW/I to avoid this behavior.	Yes / No	There is no problem in case of using only the C language.	2010/8/10
Peripheral	Interrupt	Do you return from the interruption routine after dummy reading once the resource register connected with the peripheral bus1 after the interrupt cause bit of LIN-USART and RTC is cleared?	When the interrupt cause bit of LIN-USART and RTC is cleared, actually, to wait for clearing the interrupt cause bit, return from the interruption routine after dummy reading once the resource register connected with the peripheral bus1.	Yes / No		2010/8/10
Others	General	Ultimately, Do you evaluate the timing with the mass product?	MB96F346RxxB/F347xxB/F348xxB compared to other devices of the F2MC-16FX family including the EVA devices and have some different the following operations. (1)The interrupt controller and DMA controller serve all interrupts from peripherals connected to peripheral bus 1 two clock cycles of CLKB earlier on the MB96F346Rxx/F347Rxx/F348Rxx/F386RxB/F387Rx compared to other devices of the F2MC-16FX family including the EVA devices. (2)The interrupt controller and DMA controller serve CAN interrupts from CAN interfaces one clock cycle of CLKP earlier on the MB96F346Rxx/F347Rxx/F348Rxx/F386RxB/F387Rx compared to other devices of the F2MC-16FX family including the EVA devices. (3)There may be a difference in the timing for peripheral accesses on the MB96F346Rxx/F347Rxx/F348Rxx/F386RxB/F387Rx compared to other devices of the F2MC-16FX family including the EVA devices by clock setting. (4)DMA controller takes one CLKB shorter time to clear the interrupt of the peripherals compared to other devices of the F2MC-16FX family, including the EVA devices MB96V300BRB and MB96V300CRB.	Yes / No	MB96F346RxxB/F347xxB/F348xxB has some different operation for EVA device.	2010/9/15

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peripheral	Change of peripheral clock	When CLKP2 and CLKP3 are changed from previous value, do you change after dummy access(reading or writing) more than three times to peripheral registers under CLKP2 and CLKP3?	When CLKP2 and CLKP3 are changed from previous value, the change may be ignored if you don't wait more than CLKB * 6 clocks + CLKS2 * 6 clocks.	Yes / No	Only for MB96F356xxB/F326xxB/F348Hxx/F348Txx /V300B/V300C.	2010/8/10
CPU	Change of main clock stabilization time	When main clock stabilization value is changed from previous value, do you change after waiting more than CLKS1 * 6 clocks + main clock timer 6 counts?	The change may be ignored.	Yes / No	Only for MB96F356xxB/F326xxB/F348Hxx/F348Txx /V300B/V300C.	2010/8/10
CPU	Change of sub clock stabilization time	When sub clock stabilization value is changed from previous value, have you changed after waiting more than CLKS1 * 6 clocks + sub clock timer 6 counts?	The change may be ignored.	Yes / No	Only for MB96F356xxB/F326xxB/F348Hxx/F348Txx /V300B/V300C.	2010/8/10
Peripheral	Flash	Do you judge the termination of the sector erase operation by polling the DQ6flag or all 8bit data?	The sector erase completion might be misjudged if only the DQ7 flag is used to identify the termination of the sector erase operation.In case of using DQ7, start the polling of DQ7 after waiting for 160us or more with software after the command submitted.	Yes / No	Only for the using the automatic algorithm of flash memory.	2010/8/10
Peripheral	Flash	Do you disable the software, watchdog or clock stop reset when the Flash memory is in the "busy" or "time out" state?	If a Software Reset, a Watchdog Reset or a Clock Stop Reset is asserted while the Flash memory is being programmed or erased, invalid data may be read subsequently. Executing a Power reset (Power-on or Low voltage) or an External reset initializes the Flash memory state machine from any state back to the "READ" state.	Yes / No	Only for MB96F346xxB/F347xxB/F348xxB/F348Hxx /F348Txx/F386xxA/F387xxA/F386xxB/F38 7xxB while the flash memory is being programmed or erased.	2010/8/10
CPU	DMA	Do you set the different value to the DISEL register with the enabled DMA channel and the disabled DMA channel?	If the same value is set to the DISEL register with the enabled DMA channel and the disabled DMA channel, the DMA interrupt service routine is called at each data transfer and not only after the DMA has completed the transfer.	Yes / No	Only for MB96F346Rxx/F347Rxx/F348Rxx/F386Rxx /F387Rxx	2010/8/10
CPU	Watchdog	Do you know If the watchdog is not cleared within the specified interval time, then the watchdog reset assertion will not be immediate (maximum delay is one interval time).	The reset assertion however will not happen immediately after the watchdog counter has reached the interval end time. Instead there are two possibilities: 1. If the watchdog is cleared after elapsing of the specified interval time, then the reset will be asserted immediately after this watchdog clear command. 2. If the watchdog is not cleared within a second interval of the same length as the specified interval time, then the watchdog reset will be asserted at the end of this second interval time.	Yes / No	Only for MB96F346xxB/F347xxB/F348xxB/F348Hxx /F348Txx/F386xxA/F387xxA/F386xxB/F38 7xxB/V300B	2010/8/10
Peripheral	Input Capture Unit	Do you initialize the ICE01and ICE67 registers when you use the input capture unit?	When the MCU is in internal Vector Mode (MD[2:0] = 0 1 1B) and the Boot ROM is performing temporary UART scan (the UART Scan Deactivation Marker {USDM1, USDM0} is not set to the value 292D3A7BH), then the following registers do not show the correct initial value: ICE01:"xxx1x100b", ICE67:"xxx1x100b"	Yes / No	Only for MB96F346xxB/F347xxB/F348xxB/F348Hxx /F348Txx/F386xxA/F387xxA/F386xxB/F38 7xxB/384/385/F33x	2010/8/10
Others	EUROScope	Do you use the LIN-USART0/1/2/3 when you use the EUROScope?	Only the LIN-USART0/1/2/3 can be used at the EUROScope, because the registers EDSU2_TSEL and EDSU2_RSEL are not available.	Yes / No	Only for MB96F346Rxx/F347Rxx/F348Rxx/F386Rxx /F387Rxx	2010/8/10
Others	EUROScope	Is there setting '0' for bit0 WTI0 of WDTC register, if you use EUROScope?	After break, internal Watch Dog timer might be not normal operation, if bit0:WTI0 of WDTC register is '1' on use EUROScope Debugger.	Yes / No	Only for MB96F346xxB/F347xxB/F348xxB/F348Hxx /F348Txx/F386xxA/F387xxA/F386xxB/F38 7xxB/345/346/384/385	2010/8/10
Others	EUROScope	Is there setting '0' for bit3 of 0xDF0045, if you use EUROScope?	Watch Dog will reset the device because it can not stop after break, if EUROScope debugger is used as following conditon. A : Use internal Watch Dog timer B : Write '1' to bit3 of 0xDF0045	Yes / No	Only for MB96F348CSC/F348CWC/F348HSC/F348 HWC/F348TSC/F348TWC	2010/8/10
Others	EUROScope	Is there setting H'00 for DTB, if you use EUROScope?	It might be not use break fuction on EUROScope debugging, if DTB is not H'00.	Yes / No		2010/8/10
Peripheral	Clock	Does internal clock (CLKS1,2,CLKB,CLKP1,2,3) observe strictly and set the maximum value described in the data sheet?	There is a possibility of the malfunction when the upper limit of the operation guarantee frequency is exceeded.	Yes / No		2010/8/12
CAN related item	Reception error and bus-off	Do you know there is no possibility of a bus-off by the reception error?	In the software development, a countermeasure against a bus-off due to a reception error is invalid.	Yes / No		2010/10/29
CAN related item	High-speed CAN and oscillator accuracy	For a high-speed CAN data communication, is the highly accurate oscillator used?	As the allowable error of the oscillator depends on the baud rate of CAN, the large error of the oscillator may prevent the normal communication.	Yes / No		2010/10/29

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CAN related item	CAN baud rate	Do you make the settings that consider the condition of each segment to decide the CAN baud rate?	There is a possibility that the CAN transmission and reception are not executed normally.	Yes / No	Confirm whether the requirement of TSEG1 ³2TQ, TSEG1 ³ RSJW, TSEG2 ³ 2TQ, and TSEG2 ³ RSJW in the manual is met.	2010/10/29
CAN related item	IDR	Is the message buffer (BVAL) enabled without setting ID in ID?	An initial value of IDR that sets ID is indefinite. Therefore, there is a possibility of receiving the indefinite data of ID when the target message buffer is enabled though the value is not set.	Yes / No		2010/10/29
CAN related item	Regarding with DIR	Mdir bit should not be masked.	In hardware manual, it said Mdir bit should not be masked .	Yes / No	Please refer to hardware manual.	2010/10/29
CAN related item	The transmission of C_CAN	Is not the transmission of the setting of the low rank message buffer as the transmission buffer, and the low rank message buffer canceled?	At you use the message buffer of the low rank priority level as a transmission, when TXRQST is set to "0", if TXRQST is set to "1" again, the transmission might be delayed. The message might not be transmitted immediately after TXRQST is set to "1" according to timing that TXRQST is set to "0". After either of following event, the message is transmitted. − An effective message on the CAN bus flows. − The transmission request is issued to other message buffers. − The CAN bus is initialized by the INIT bit.	Yes / No	Please refer to hardware manual.	2010/10/29
CAN related item	The transmission of C_CAN	At Disable Automatic Retransmission mode(DAR bit=1), are not two or more (3 or more) messages transmitted at the same time?	Only two messages are sent, if the host requests transmission of several messages at the same time, when the Disable Automatic Retransmission mode; DAR bit is set to "1" in CAN. While the TxRqst bit of any other message buffer requested for transmission is reset, the transmission does not start. NewDat and IntPnd remain unchanged.	Yes / No	Please refer to hardware manual.	2010/10/29
CAN related item	The INIT bit of C_CAN	Is the INIT bit of the CAN control register set while transmitting the CAN data frame?	When the INIT bit of the CAN control register is set while transmitting the last bit in control field of the CAN data frame, after clearing the INIT bit, as for the data field of the frame transmitted first, the 1 bit is shifted left.	Yes / No		2010/12/1
Peripheral	LIN-USART	When the mark Level of the serial clock is set to "L", is LIN-USART used for software reset (SMR: UPCL=1) in the master mode of the synchronous mode (operation mode 2)?	High pulse of one peripheral clock is output from serial clock output (SCK). Therefore, there is a possibility to recognize that the serial clock was supplied the slave device connected with external.	Yes / No		2010/12/1
Peripheral	External bus	Is the branching or reading/writing done to a corresponding external addressing domain (CS area) immediately after the access to the external area is set to enable?	When the branching or reading/writing is done to a corresponding external addressing domain (CS area) with external bus mode register (EBM), immediately after the access to the external area is set to enable, the instruction is not correctly executed.	Yes / No		2010/12/1
CAN related item	Notes that when transmission data is set	When transmission data is set to the message object, is NEWDAT set to 1 at the same time as TXRQST ?	There is a possibility that TXRQST disappears according to timing when new transmission data is set when the message object has already started finishing transmitting. Therefore, please set the message object after setting NEWDAT in '1'.	Yes / No	Please refer to hardware manual.	2011/4/26
CAN related item	Notes of received data handling	Are only received data of the number of DLC or less adopted?	When the received data frame is stored, the message handler writes all of eight databytes in the message object. When the received data length is less than 8 byte, the byte of the remainder of the message object is overwrited in an irregular value.Please do not refer to an irregular value.	Yes / No	Please refer to hardware manual.	2011/4/26
CAN related item	About the sequence of the setting and the MSGVAL setting of the acceptance mask	After the acceptance mask of the message object is set, is MSGVAL set?	There is a possibility of receiving it by an acceptance value wrong that mask bit is not set before MSGVAL is set to '1' when the acceptance mask is made effective with UMASK on the message object.	Yes / No	It is thought that the acceptance mask value of the message object is not changed while entered to the CAN bus. Please change if you change the acceptance mask value with corresponding MSGVAL made '0'.	2011/4/26
CAN related item	About the initial value of MSGVAL	Has MSGVAL on the message object not used been cleared before C-CAN enters it to the CANbus?	Initialize MSGVAL before the microcontroller enters it to the CAN bus. There is a possibility of receiving the incorrect data when the user doesn't initialize MSGVAL and it enters it to the CAN bus.	Yes / No	Please refer to hardware manual.	2011/4/26
CAN related item	About the initial value of the message object	Is the as needed initialized and is the message object of C-CAN used?	The initial value of the register related to C-CAN after the microcontroller's reset is released is not decided.	Yes / No	Please refer to hardware manual.	2011/4/26