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| Item | | Content | Reason | Result | Remarks |
|---|---|---|---|---|---|
| CAN関連 | Reception error and bus-off | Do you know that a reception error cannot lead to a bus-off status? | For a software that is developed assuming that reception errors lead to "bus-off" status, however, processing based on such assumption is invalidated. | Yes / No | |
| | ID checking during reception of normal ID | For standard ID processing at reception of CAN data, is filtering processing implemented for IDs other than the target IDs? | For non-target IDs (difference between extended format and standard format), other ID data could be included. Example: For some ID data to be processed, the data cannot be received in the processing routine of the target ID. | Yes / No | |
| | Disable/Enable of message buffer | In the reception processing routine, is the data processed by using the reception overrun register (ROVRR) instead of invalidating the target message buffer (BVALR)? | "Hit and Away" can occur. | Yes / No | |
| | Error counter and error status | Is the error status judged only with the error counter? | There are cases where the error status value and the error counter value do not match after the error counter exceeds a count of 256. | Yes / No | |
| | Reception error counter | Do you know that when the reception error count reads REC of 128 or more and a normal reception occurs, the REC is changed to the value between 119 and 127. | There is a need to exercise caution with software that relies on the reception error count. | Yes / No | |
| | Glitch to CAN TX pin | Do you know that a glitch can be output to the CAN TX pin? | In terms of system operations, this does not bring about any adverse effects. However, you need to know this as information for system inspection purposes. | Yes / No | |
| | High-speed CAN and precision of ocillator | Is a high-precision oscillator used to execute high-speed CAN data communications? | As the tolerance of an oscillator depends on the CAN baud rate, normal communication cannot be made when the oscillator's error is larger than the tolerance. | Yes / No | |
| | Processing for DLC of 9 and higher | Is the software fail-safe in anticipation of a DLC of 9 and higher for DLC judgment at data reception? | The CAN standard stipulates DLC of 8 and less. However there is no specification for transmission at DLC of 9 and higher. Accordingly, to avoid problems for transmission of DLC of 9 and higher, we recommend considering the fail-safe approach in developing a software. | Yes / No | |
| | Hit and Away | Is the control of message buffer prohibited processing (BVALR) for the relevant buffer during message reception or while securing message transmission permission? | A "Hit and Away" bypass can occur. | Yes / No | |
| | CAN baud rate | Are settings made considering the conditions of all segments for determining the CAN baud rate? | Normal CAN sending and reception cannot occur. | Yes / No | Confirm whether the following conditions in the manual are met: TSEG1 >= 2TQ, TSEG1 >= RSJW, TSEG2 >= 2TQ, TSEG2 >= RSJW |
| | Acceptance mask register switching | Is the acceptance mask register changed while HALT is "0" ? | Unless the acceptance mask register is changed after setting HALT to "1" and invalidating the message buffer, "Hit and Away" can occur. | Yes / No | |
| | HALT bit clear timing | Before clearing HALT bit, is it confirmed that the value of HALT bit is "1"? | When HALT bit is cleared at the timing when the value of HALT bit is changing from "0" to "1," the unconformity of internal operation may be caused. | Yes / No | |
| | Implementation of RMW instruction to CSR | Do you know that the implementation of RMW instruction to CSR is restricted by the manual? | Because the implementation of RMW instruction to CSR is restricted, the development of a software without RMW instruction implementation is recommended. | Yes / No | |
| | IDR | Is the image buffer (BVAL) enabled without setting ID in "ID"? | Because the intial value of IDR setting ID is unstable, when the target image buffer is eabled without setting the value, the data of undefined ID may be recieved | Yes / No | |

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|---|---|---|---|---|---|
| | Reception interruption processing | Confirm that RC is completly cleared in alll image buffers in the reception interruption routine of CAN. | It is recommended that the software development is implemented so that the interrupt flag (CR) of an image buffer that is indicated not to be received in the reception interrupt routine of CAN is also cleared considering a fall-safe. | Yes / No | |
| CPU | Power-on reset | Is the standard on electrical characteristics concerning power-on reset being met? | Powering on without meeting the power-on reset standard may result in the execution of commands by CPU without the power-on reset implemented normally. | Yes / No | Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input). |
| | External reset | Does the reset range meet the Fujitsu's standard? | When the reset range does not meet the Fujitsu's standard, recovery cannot be implemented. | Yes / No | |
| | Hard-wired reset | In FLASH micro computer, the values of reset vector and mode data are determined with an internal circuit. (Reset vector address: FFA000H, Mode data: 00H) | Unless the start address of a program is set to be tha fixed vector address of hard-wired reset, the abnormal operation is implemeted. Note that this failue is, however, not debugged with an Evaluation(EVA) chip. | Yes / No | |
| | PLL->Main | In software development, is attention given to the timing of the changes in the CPU's operation speed during the status transition of Main -> PLL -> Main -> PLL when such processing speed does change? (Is consideration given to the need to wait for eight cycles between MCS "1" write and "0" write?) | Within the eight cycles between MCS "1" write (Main) and "0" write (PLL), "0" write can be ignored. | Yes / No | Refer to the explanation of the MSC bit in the manual. |
| | Main(PLL) -> Sub -> Main(PLL)* | In CPU status transitions, during status transition of Main or PLL -> Sub -> Main or PLL, is it verified, prior to transition to another status, that the CPU is transferred to statuses set by using the MCM and SCM bits? | Between the "0" write (Sub) and the "1" write (Main) to SCS, "1" write can be ignored within one sub clock cycle. When switching SCS, modify SCS only after verifying that transition to the status expected in SCM occurs. | Yes / No | Refer to the explanation of the SCM bit in the manual. |
| | PLL -> Sub(Stop) -> PLL | For direct transition to PLL mode following the release of main clock stop status, is the oscillation stabilization wait time of the main clock set longer than the PLL clock wait time? | When transition to PLL mode recurs after transition from PLL mode to sub RUN (or STOP) status, the oscillation stabilization wait time of the main clock should be set longer than the PLL clock wait time. | Yes / No | |
| | Switching of the internal clock operation mode | When switching the internal clock operation mode (PLL, main, sub), is the operation mode switched to another mode? | If, when switching the internal clock operation mode (PLL, main, sub), the operation mode is switched to another mode, problems may arise when switching the mode（Behavior such as attempting to transition to the PLL mode during main clock oscillation stabilization wait time in transition from sub-clock oscillation to main clock oscillation is prohibited). | Yes / No | See the explanation of the MCS and SCM bits in the manual. |
| | Transition to standby mode | Do you know the notes to be followed at transition to standby mode? | For transition to standby mode, to access the low power consumption mode control register, add the following commands.<br>*MOV LPMCR,#xxh ;standby mode transition com.*<br>*NOP*<br>*NOP*<br>*JMP S+3 ;jump to next com.*<br>For details, see the hardware manual. (See the chapter on low power consumption mode.) | Yes / No | Applied only when standby mode is used. |
| | Time-base timer | Is the time-base timer interrupt prohibited during transition from the main mode to the PLL mode or from the main mode to the submode? | Since the time-base timer is used as a counter of the oscillation stabilization wait time and PLL clock stabilization wait time, the counter is automatically cleared in the following state transitions:<br>- Transition from the main clock mode to the PLL clock mode<br>- Transition to the subclock mode<br>- Transition to the stop mode<br>When the time-base timer interrupt is not prohibited during state transition from the main mode to the PLL mode or from the main mode to the sub-clock mode, an unintended time-base timer interrupt may occur. | Yes / No | |

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|---|---|---|---|---|---|
| | A/D converter | Is analog impedance the analog impedance described in the datasheet or less. When the analog impedance is higher, it is required to set the sample hold time longer or install an external capacitor of approximate 0.1 uF. | When the analog impedance is higher, the sampling time of analog data may become shorter than required time. | Yes / No | Only when A/D converter is used. |
| | | Is voltages of AVR and AVCC are sufficiently stable? | To separate power supplies of analog system and digital system, a reactance device may be mounted in AVR and AVCC. In this case, it is reconmmended to configure the circuit by adding a capacitor of some micro F so that sufficient power is supplied at A/D start. | Yes / No | Only when A/D converter is used. |
| | | Is analog sampling time sufficiently long? | When anolog input impedance is larger, a glitch may occur at analog input pin.. The glitch is determine by the analog impedance and time constant of internal capacitance. When sample hold time is shorter, sample hold value may be affected by the glitch. Because the influence of the glitch is different beteween FLASH product and MASK product, it is recommmended to set a sufficient sample hold time when the analog input impedance is larger. | Yes / No | Only when the analog input impedance used is larger than the analog input impedance recommended by th Data Sheet. |
| | | Are the completion and start of A/D conversion implemented at the same time? | When the comletion and start of A/D conversion are implemented at the same time, the later operation, the start of the A/D conversion, may be ignored. | Yes / No | Only when A/D conversion is started during A/D conversion performed. |
| | Unused pin treatment | Is any unused pin pulled up or pulled down by the resistor of 2 kΩ or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened? | When an unused pin is treated without a resistor and the port level opposite to the processing level is output due to CPU runaway, problems such as latch-up may arise. | Yes / No | |
| | Interrupt | Is the interrupt vector processing of an exceptional interrupt performed? | Runaway may be caused when an undefined instruction is executed due, for example, to runaway. | Yes / No | When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended. |
| | | Are interrupt factors cleared in the main routine? | Since interrupt factors may be cleared and set simultaneously, it is recommended to clear interrupt factors in an interrupt routine. When interrupt sources are to be cleared in the main routine, it is recommended to clear them after prohibiting interrupts of the target peripheral. | Yes / No | Since, particularly for UART, reception interrupts are set asynchronously, it is recommended to clear interrupt factors in an interrupt routine so that they should not occur simultaneously with reception interrupt setting or clear them after prohibiting reception interrupts. |
| | | Is processing of an unused interrupt vector performed? | Runaway may be caused when an unused interrupt occurs due, for example, to runaway. | Yes / No | When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended |
| | Bit manipulation instruction | Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register? | The instruction may not be executed normally, resulting in unintended data being written. | Yes / No | Read-modify-write related instruction is indicated in the instruction list by * in RMW. |
| | Main clock oscillation stabilization wait | Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator? | CPU may be run before oscillation has stabilized. | Yes / No | Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used. |
| | Subclock oscillation stabilization wait | Has the state transition from the main mode to the subclock mode taken place while the subclock oscillation is still unstable? | The subclock needs longer oscillation stabilization time than the main clock does. Thus, before the state transition to the subclock mode takes place, oscillation of the subclock needs to stabilize. | Yes / No | Only when the subclock is used |

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|---|---|---|---|---|---|
| | Stop mode | When transiting directly to the stop mode or clock mode from the PLL mode without passing through the main mode, is the oscillation stabilization wait time set to 2^14/HCLK or more? | To return from the PLL stop or PLL clock mode, both the oscillation stabilization wait time of the oscillator and the PLL stabilization wait time are required (2^14/HCLK or more). Thus, the WS1 and WS0 values of CKSCR should be set to "10" or "11." | Yes / No | |
| | Watchdog | Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings and the intermittent operation mode considered?) | When the watchdog reset interval is not sufficient, whether a program is proceeding normally cannot be detected. | Yes / No | |
| | | When using the built-in watchdog timer during sub-clock operation, is the watchdog clock resource set so that the clock timer is used (WDCS=0)? | When using the built-in watchdog timer during sub-clock operation, if the time-base timer is set as the watchdog clock resource (WDCS=1), no watchdog may be generated during sub-clock operation. | Yes / No | |
| | External reset IC | When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered? | When no reset within the guaranteed operation voltages is entered, a malfunction may occur. | Yes / No | Confirm the guaranteed operation voltage range in the data sheet. |
| | I/O port | Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output? | Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports. | Yes / No | |
| | | When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register? | Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first. | Yes / No | |
| | General | Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Fujitsu? When any of them does not satisfy the standards, is any special guarantee considered and supported? | When not used within the guarantee range, no product guarantee can be provided. | Yes / No | Check the guaranteed operation range in the data sheet. |
| Noise reduction measures and others | Mode(MOD) pin | Is the same level for processing of the MOD pin ensured even while executing instructions? | The level of the MOD pin may be read incorrectly (When a high-impedance resistor is used for treating the MOD pin, the MOD pin level may not be ensured due to noise). | Yes / No | When external noise tends to propagate to the MOD pin, it is recommended to take countermeasures against static electricity such as connecting a capacitor to the mode pin. |
| | | Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect? | The level of the MOD pin may be read incorrectly due to power supply deviation and noise. | Yes / No | |
| | Oscillation | When using a crystal oscillator, is an appropriate dumping resistor inserted? | To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed. | Yes / No | Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used. |
| | | Is oscillation matching data of mass-produced products obtained? | Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products. | Yes / No | Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used. |

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| | | Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude? | When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase. | Yes / No | When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise. |
| | | Is the oscillator arranged as close to the chip as possible? | CPU runaway due to external noise may be presumed. | Yes / No | It is recommended to arrange the oscillator as close to the chip as possible? |
| | Vcc, GND | Is consideration given to making Vcc and GND as strong as possible? | Problems of unnecessary radiation noise and CPU runaway due to external noise may be presumed. | Yes / No | To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened). |
| | ESD, latch-up, noise | Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances? | Since the resistances against ESD, latch-up, and noise of Flash products and those of mask products are different, it is recommended to use mass-produced products to evaluate ESD and latch-up resistance. | Yes / No | Since it is possible to submit measurement results of Fujitsu as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them. |
| | Capacitor | Is the optimum capacitor connected near the chips as a capacitor for reducing noise? | The capacitor connected to reduce noise may not work with reactance components of interconnect (Measures that take noise components into account are needed) | Yes / No | |
| | C pin | The capacitance of the smoothing capacitor connected to Vcc is larger than that of the capacitor connected to C pin? | When the capacitance of the smoothing capacitor is smaller, the internal regulator may become unstable. | Yes / No | |
| | Connection of reactance | Is reactance connected directly with power supply? | The characteristic of internal requlator might not be obtained by the reactance element. | Yes / No | If reactance is put directly in the power supply of chip , it is necessary to conect capacitor between chip power supply and reactance. |
| | Memory map | Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation? | The built-in memory amount of the EVA chip for evaluation and that of the Flash and mask chip are different. Therefore, the actual chips may not work even if normal operation is confirmed by using a tool. | Yes / No | |
| | Stack usage | Is the maximum usage of stack confirmed? | Incorrect estimation of the stack usage could lead to RAM damage. | Yes / No | It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack (Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage). |
| | Operation mode of tools | Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation? | The native mode and debug mode are available as the operation modes of tools. Since the working speed in debug mode is different from the actual working speed, it is recommended to make an evaluation after setting the native mode. | Yes / No | |