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AN205101

F²MC-8L/8FX/16LX16FX, MB89XXX / MB95XXX / MB90xxx / MB96Xxx, Performing SPI

It is said that SPI (Serial Peripheral Interface) is a simple communication between two digital devices. Because of no general specification and much different formats, SPI is not so simple at all. This application note describes the most common SPI formats and how to implement them on Cypress 8-, and16-Bit MCUs.

Contents

1 Introduction

It is said that SPI (Serial Peripheral Interface) is a simple communication between two digital devices. Because of no general specification and much different formats, SPI is not so simple at all.

This application note describes the most common SPI formats and how to implement them on Cypress 8-, and16-Bit MCUs.

2 SPI Formats

This chapter describes the most common SPI formats

2.1 General SPI

SPI is a single master single slave synchronous serial communication. Each data bit from and to the master has its own clock pulse. Therefore SPI uses at least three different signals:

1. SCK: Serial Clock
2. SI: Serial Input (Data from Slave to Master)
3. SO: Serial Output (Data from Master to Slave)

Some SPI formats use a fourth signal called “Chip Select” (CS) which enables the communication by the master. This signal can be positive or negative active.

2.2 SPI Clock (SCK)

Because there exists no common SPI specification, the timing of the SPI clock signal is device dependent and it seems so, that every producer uses its own timing.

For most SPI protocols four different settings are possible, which are mostly defined by the internal SPI master control settings: CPOL (Clock polarity) and CPHA (Clock phase).

- CPOL defines the active state of the SPI serial clock and thus the mark level.
- CPHA defines the clock phase in respect of the SO-data bit.

  There is no common classification of SPI protocols and SPI devices, which defines the settings of CPOL and CPHA in respect of the protocol itself. So this document defines the settings as follows:

- CPOL = 0: SPI clock has mark level “0”
- CPOL = 1: SPI clock has mark level “1”
- CPHA = 0: SPI clock is delayed by a half bit time in respect of SO-data bit
- CPHA = 1: SPI clock is synchronous to SO-data bits

2.3 Data direction

In the most SPI formats the serial data direction is MSB first.

2.4 Communication speed

The transfer rate of SPI communication is defined by the hardware itself. Mostly the speed is limited by set-up and hold timing of the data signals.

SPI is used in a wide communication speed range. The range reaches from some K Bits/s to some M Bits/s.

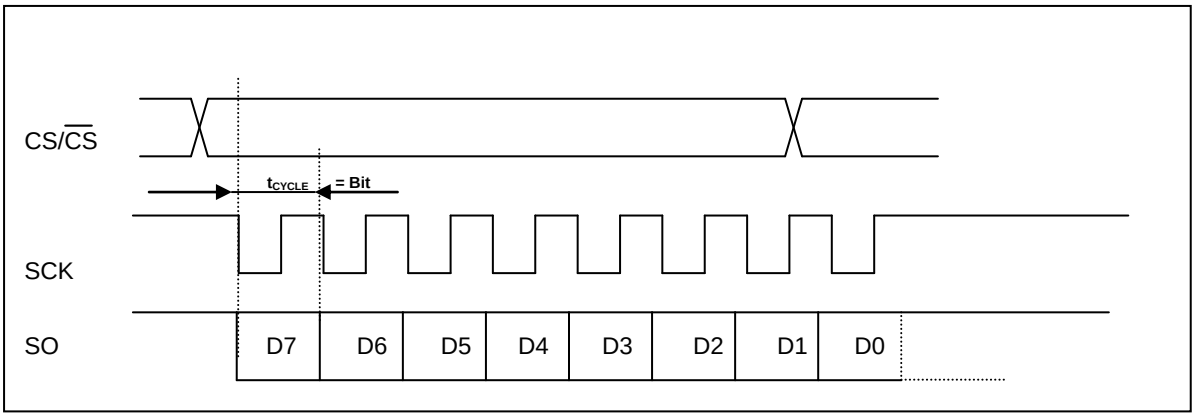
2.5 SPI protocols

This section describes the most common different SPI protocol timings.

2.5.1 CPOL = 1, CPHA = 1

This SPI format is in accordance with the “standard” serial synchronous format. The timing of the signals is shown in the illustration below:

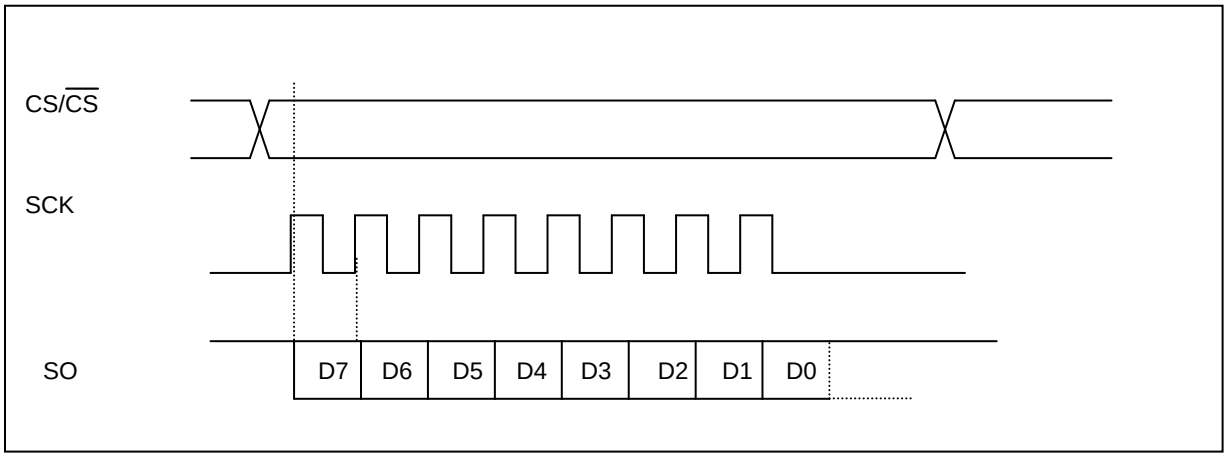
Figure 1. SPI clock in phase with data (mark level = “1”)



2.5.2 CPOL = 0, CPHA = 1

This SPI format is in accordance with the “standard” serial synchronous format with inverted clock signal.

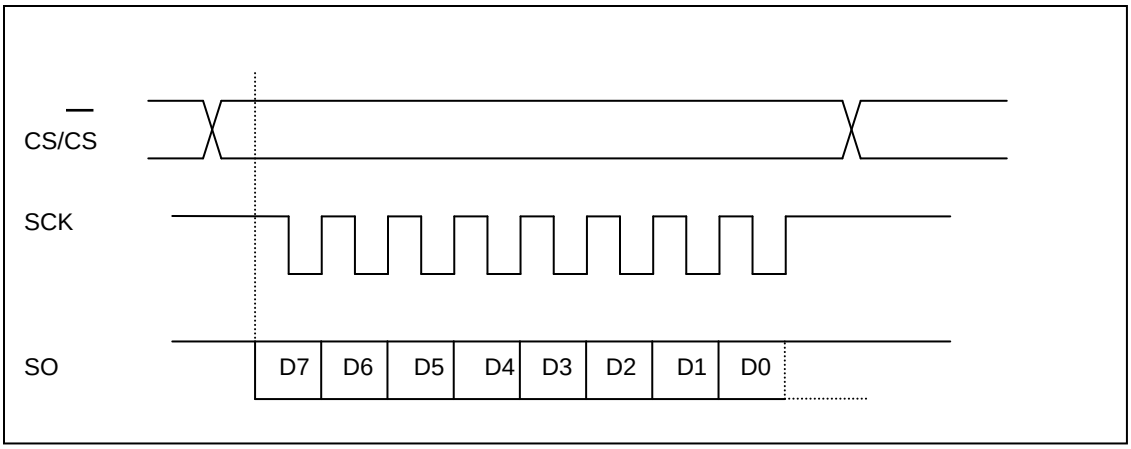
Figure 2. SPI clock in phase with data (mark level = “0”, inverted)



2.5.3 CPOL = 1, CPHA = 0

In this SPI format the clock signal is delayed by a half bit time to the “standard” synchronous format.

Figure 3. SPI clock delayed by half bit time (mark level = “1”)

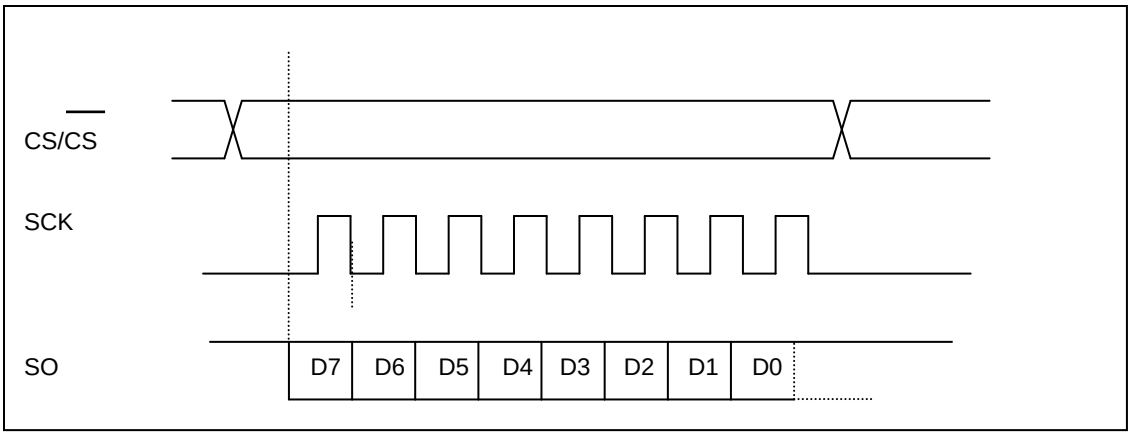


Note, that in this format the first data bit has to be set on SO *before* the first clock pulse occurs.

2.5.4 CPOL = 0, CPHA = 0

In this SPI format the clock signal is delayed by a half bit time to the “standard” synchronous protocol and the clock signal is inverted.

Figure 4. SPI clock delayed by half bit time (mark level = “0”, inverted)



Note, that in this format the first data bit has to be set on SO *before* the first clock pulse occurs.

3 Implementing SPI-Master Communication

This chapter describes how to implement the different SPI formats

3.1 Implementing SPI Formats with CPHA = 1

3.1.1 SPI with CPHA = 1 and CPOL = 1

This SPI format is available for all Cypress SIO interfaces.

Cypress UARTs with synchronous mode can also handle this format.

3.1.2 SPI with CPHA = 1 and CPOL = 0

This SPI format is available for all Cypress SIO interfaces with serial clock inversion (NEG-Bit).

Cypress UARTs with synchronous mode and serial clock inversion can also handle this format (NEG- or SCES-Bit).

3.2 Implementing SPI Formats with CPHA = 0

This format is available for the LIN-UART since MB90340 series. To implement this, programmer has to use synchronous mode and SCDE = 1 (Serial Clock Delay Enable) and SCES = x (Serial Clock Edge Select, means CPOL = x).

For all other SIOs or UARTs some tricks have to do.

3.2.1 SPI with SIO and CPHA = 0, CPOL = 1

The SIO can only handle SPI formats with CPHA = 1 in its normal operation mode. When external shift clock mode is selected, the SIO can be clocked by the toggling the port in respect of its SCK pin.

An undocumented feature is that the SIO can also be clocked by toggling the NEG bit of the SES register (Serial Edge Select). Thus it is possible to set the first data bit to SO before the clock is generated via the port pin.

The following C code shows an example of this method. Note, that the maximum communication speed depends on the execution time of the instructions (MCU speed) and the function `SPI_Byte` must not be broken by an Interrupt:

Example C code of CPHA = 0 and CPOL = 1 with SIO

```
void InitSIO (void)
{
   PDR4 = 0x80;        // SCK2 port 47 pin MB90540 series
   DDR4 = 0x80;        // SCK2 set to "1"

   SMCS_SOE = 1;       // Serial Output enable
   SMCS_SCOE = 0;      // Internal serial clock disable
   SES2_NEG = 1;       // Invert clock
   SMCS_STOP = 0;      // Reset STOP
   SMCS_SMD = 0x05;    // External shift clock mode
   SMCS_BDS = 1;       // Set MSB first
}
```

```
unsigned char SPI_Byte(data)
{
   SDR = data; // Write data to shifter
   SMCS_STRT = 1;      // Set communication start

   SES2_NEG = 0;       // Generate "internal clock" pulse
   SES2_NEG = 1;       // to set first data bit on SOT2

   PDR4_P47 = 0;       // generate 8 clock pulses on SCK2
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;
   PDR4_P47 = 0;
   PDR4_P47 = 1;

   SES2_NEG = 0;              // "internal clock" pulse to fulfill
   SES2_NEG = 1;              //   SIO communication

   data = SDR;         // read shifter
   return data;
}
```

Note: A CS signal can easily performed using another port pin.

3.2.2 SPI with SIO and CPHA = 0, CPOL = 0

The method for CPOL = 0 is much like the method above (3.2.1).

The following C code shows an example of this method. Note, that the maximum communication speed also depends on the execution time of the instructions (MCU speed) and the function `SPI_Byte` must not be broken by an Interrupt:

Example C code of CPHA = 0 and CPOL = 0 with SIO

```
void InitSIO (void)
{
   PDR4 = 0x00;        // SCK2 port 47 pin MB90540 series
   DDR4 = 0x80;        // SCK2 set to "0"

   SMCS_SOE = 1;       // Serial Output enable
   SMCS_SCOE = 0;      // Internal serial clock disable
   SES2_NEG = 0;       // Normal clock
   SMCS_STOP = 0;      // Reset STOP
   SMCS_SMD = 0x05;    // External shift clock mode
   SMCS_BDS = 1;       // Set MSB first
}
```

Note: A CS signal can easily performed using another port pin.

3.2.3 SPI with UART synchronous and CPHA = 0, CPOL = 1

The method for SPI (CPHA = 0 and CPOL = 1) with a UART in synchronous mode is similar to the method used with the SIO.In this example the clock of the UART is also generated internal with toggling the NEG-Bit and generating an “external” clock via the Port state of the corresponding SCK pin.

Note, that this example only works for UARTs, which support a synchronous serial mode and a pre-scalar, not a reload counter. Those UARTs are identifiable by the CDC register (Clock Division Control).

Example C code of CPHA = 0 and CPOL = 1 with UART synchronous

```
void InitUART(void)
{
   SMR1_MD1 = 1;       // Set synchronous mode
   SMR1_MD0 = 0;
   SMR1_CS2 = 1;       // Set external clock source
   SMR1_CS1 = 1;
   SMR1_CS0 = 1;
   SMR1_SCKE = 0;      // External clock
```

Note: A CS signal can easily performed using another port pin.

3.2.4 SPI with UART synchronous and CPHA = 0, CPOL = 1

The method for SPI (CPHA = 0 and CPOL = 1) with a UART in synchronous mode is much like the example above (3.2.3)

Example C code of CPHA = 0 and CPOL = 1 with UART synchronous

```
void InitUART(void)
{
   SMR1_MD1 = 1;       // Set synchronous mode
   SMR1_MD0 = 0;
   SMR1_CS2 = 1;       // Set external clock source
   SMR1_CS1 = 1;
   SMR1_CS0 = 1;
   SMR1_SCKE = 0;      // External clock
   SMR1_SOE = 1;       // Serial Output Enable
   SES1_NEG = 0;       // Normal Clock
   SCR1_TXE = 1;       // Transmission Enable

   PDR4 = 0x00;        // SCK1 Port 44 pin on MB90540 series
   DDR4 = 0x10;        // SCK1 set to "0"
}

unsigned char SPI_Byte(data)
{
   SODR1 = data;              // Write data to transmission register

   DI();               // Disable all interrupts

   SES1_NEG = 1;              // Generate "internal clock" pulse
   SES1_NEG = 0;              //   to set first data bit on SOT1

   PDR4_P44 = 1;              // generate 8 clock pulses on SCK1
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;
   PDR4_P44 = 1;
   PDR4_P44 = 0;

   SES1_NEG = 1;              // "internal clock" pulse to fulfill
   SES1_NEG = 0;              //   serial task

   EI();               // Enable all interrupts (optional)

   data = SIDR;               // read from reception register
   return data;
}
```

Note: A CS signal can easily performed using another port pin.

4 Implementing SPI-Slave Communication

How to implement spi slave communication

4.1 Preface

SPI is a 1 master to n slave communication. All described SPI modes are valid for both master and slave. The main difference is, that a slave does not generate a serial clock signal, but is clocked by the master.

4.2 SPI-Slave Communication with LIN-U(S)ART

The following program flow should be used to set the LIN-U(S)ART (to be found e. g. in the MB90340 series) in the synchronous serial SPI mode, so that its state is well defined for communication.

Register	CPOL = 1 CPHA = 1	CPOL = 0 CPHA = 1	CPOL = 1 CPHA = 0	CPOL = 0 CPHA = 0	Remark
SSR	0x00	0x00	0x00	0x00	Disallow interrupts, if previously enabled
SCR	0x04	0x04	0x04	0x04	Cut of all possible previous communication, clear possible reception errors
SMR	0xB1	0xB1	0xB1	0xB1	Mode2, One-to-one external clock, enable SOT pin
ECCR	0x20	0x20	0x30	0x30	Slave mode, adjust Clock phase
ESCR	0x00	0x01	0x00	0x01	Adjust Clock polarity
SMR	0xB9	0xB9	0xB9	0xB9	Reset LIN-U(S)ART
SSR*	0x03	0x03	0x03	0x03	Allow interrupts (optional)
SCR	0x03	0x03	0x03	0x03	Allow communication

* optional - only needed, if interrupts are used

Note, that the TXE and RXE control bits of the Serial Communication Register (SCR) should be enabled as the **last step** in the initialization process. Otherwise a correct behaviour of the LIN-U(S)ART cannot be guaranteed.

5 Overview of SPI-Master capability of several MCU families

The SPI-Master Capability Of UARTS In Several MCU Families

5.1 SPI capability table

Note, that this table gives an overview of the UART SPI-Master mode capability *without* “port clocking”.

MCU family	CPOL = 1	CPOL = 0	CPHA = 1	CPHA = 0
MB89210	X	X	X	X[1]
MB90330/335	X[2]	X[2]	X[2]	X[2]
MB90340/350/360	X	X	X	X
MB90390	X	X[3]	X	X[3]
MB90385	X		X	
MB90495	X		X	
MB90540	X		X	
MB90945	X	X[3]	X	X[3]
MB95xxx	X	X	X	X
MB96xxx	X	X	X	X

X = setting possible in serial synchronous mode of UART

0 delay only by 1 MCU clock, not by half serial communication bit time

1 only two combinations possible: CPOL = CPHA = 1 or CPOL = CPHA = 0

2 only UART3

6 Appendix A

Further Information

6.1 Software example archives

- 90340_uart_sync_spi_nm93cs46-v10.zip
- 90340_uart_sync_sio_max1286-v10.zip

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	MKEA	02/26/2003	MWi; First version
			10/04/2005	MWi; 8FX series, UART cross table, and appendix added
			04/05/2006	MWi; SPI-Slave chapter added
			06/11/2010	MWi; CPOL, CPHA logic corrected
*A	5062290	HKLO	04/06/2016	Converted Spansion Application Note “MCU-AN-3000002-E-V13” to Cypress format
*B	5873121	AESATP12	09/05/2017	Updated logo and copyright.

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