FM3 Microcontroller PWM Waveform Generation by Multi-function Timer

Target Products: Refer to Section 2

This application note introduces the way how to set up multi-function timer integrated on FM3 series.

Contents

1 Introduction

This application note introduces the way how to set up multi-function timer integrated on FM3 series.

The multi-function timer has the functionality to generate three phase complement PWM waveforms. These are suitable for an inverter control which is used on white goods, FA instrument, UPS and so on.

This application note provides the basic specification of multi-function timer and shows some samples to explain briefly which setups can generate which waveforms. Besides, refer to FM3 peripheral manual (Timer Part) accordingly.

2 Target Products

This application note applies to the following products.

Series
MB9B500B
MB9B400A
MB9B300B
MB9B100A
MB9A310A
MB9A110A
MB9BD10T
MB9B610T
MB9B510T
MB9B410T
MB9B310T
MB9B210T
MB9B110T
MB9A130LA

Series
MB9B510R
MB9B410R
MB9B310R
MB9B110R
MB9A310K
MB9A110K
MB9AA30N
MB9A130N
MB9A150R
MB9B520M
MB9B320M
MB9B120M

3 Multi-function Timer Specification

3.1 Multi-function Timer Specification

The multi-function timer is a function block that enables three-phase motor control. In conjunction with PPG and A/D converter (called “ADC’ hereinafter), it can provide various types of motor control.

3.1.1 Functions

The multi-function timer has the following functions.

- It can output PWM signals with any cycle/pulse length (PWM signal output function).
- It can start PPG in synchronization with PWM signal output. It can superimpose PPG's output signal on the PWM signal and output it (DC chopper waveform output function).
- It can generate a non-overlap signal that maintains the response time of the power transistor (dead time) from PWM signal output (dead timer function).
- It can capture the timing of the input signal changing and its pulse width in synchronization with PWM signal output (Input capture function).
- It can start ADC at any timing, in synchronization with PWM signal output (ADC activation function).
- It performs noise canceling to the emergency motor shutdown interrupt signal (DTTIX input signal). It can set freely the pin state at the time of motor shutdown, when a valid signal input is detected (DTIF interrupt function).

PPG（Programmable Pulse Generator：PPG is the timer which can generate PWM waveform with any cycle and duty configured via software.

3.1.2 Block Configuration

1 unit of multi-function timer consists of the following function blocks.

Free-run Timer Unit	: 3channels
Output Compare Unit	: 6channels (2channels ×3units)
Waveform Generator Unit	: 3channels
Noise Canceller Unit	: 1channel
Input Capture Unit	: 4channels (2channels ×2units)
ADC Activation Compare Unit	: 3channels

ADC Activation Trigger Selector Unit: 3channels

The multi-function timer is configured to enable one three-phase motor control, when 1 unit is used. Some models in FM3 series contain multiple units of the multi-function timer, which are configured to support multiple three-phase motor controls.

Hereinafter, using multi-function timer unit-0 as example, this application note introduces the usage of the multi-function timer along with sample programs.

3.1.3 Abbreviations

In this application note, the following abbreviations are used.

MFT	Multi-function Timer Unit
PPG	Programmable Pulse Generator Unit
FRT	Free-run Timer Unit
OCU	Output Compare Unit
WFG	Waveform Generator Unit
ADCMP	ADC Activation Compare Unit
ATSA	ADC Activation Trigger Selector Unit

4 Configuration of Multi-function Timer

4.1 Free-Run Timer and Output Compare

- FRT is a timer function block that outputs the reference counter value for the operation of each function block in MFT.
- FRT consists of a clock prescaler, 16-bit Up/Down counter, cycle setting register (TCCP register) and controller.
- Each MFT unit is in a 3-channel configuration with three FRT's, which can operate independently from one another.
-
- OCU is a function block that generates and outputs PWM signals based on the count value of FRT. The signal names of PWM signals output by OCU are RT0 to RT5. These signals are output to LSI's external output pins via WFG.
- OCU consists of the compare value store register (OCCP register) and controller. The basic unit is in a 2-channel configuration with two sets of each circuit.
- Each MFT contains three of these OCU's and consists of a total 6 compare registers, 6 output signal pins and 6 interrupt outputs (2-channel × 3-unit configuration).

The main feature of OCU is to invert the output signal level when the FRT counting value matches OCCP value. The FRT to be synchronized with OCU can be selected out of 3 channels. For example, each channel in 1 unit of OCU can be synchronized with different FRT individually.

There are 2 types of FRT counting mode, Up-count mode and Up/Down-count mode.

Figure 1 shows each count mode. The count cycle can be set on TCCP0 register. It has a buffer register to change a cycle during count operation.

Figure 1. FRT mode and cycle calculation formula

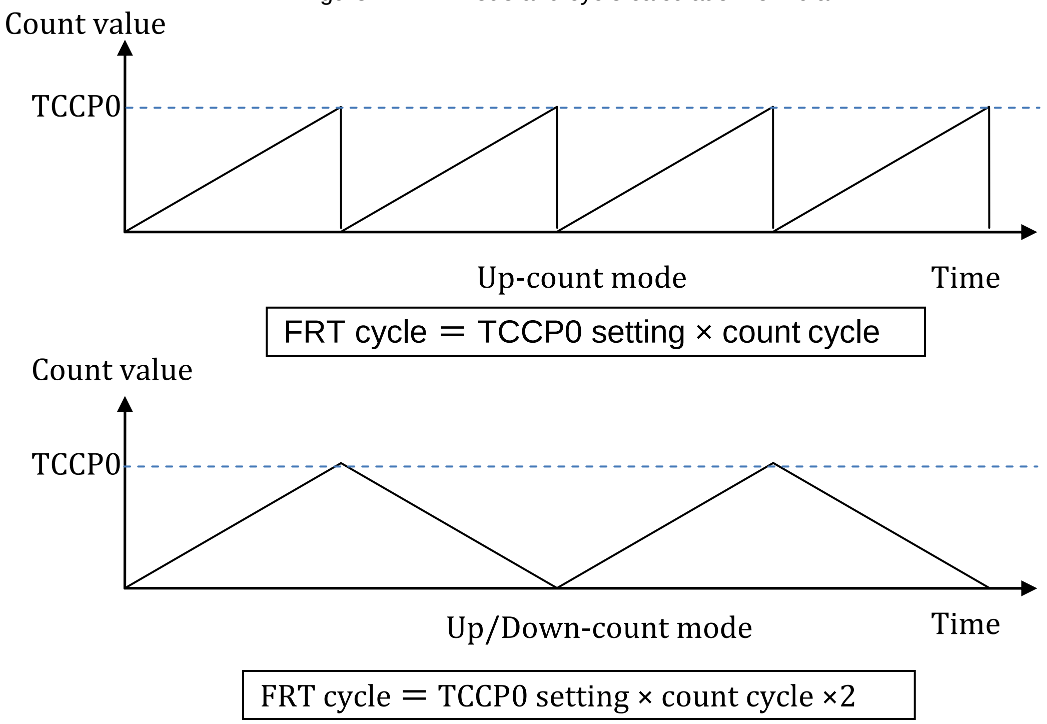

Count value
TCCP0
Up-count mode
Time
FRT cycle ＝ TCCP0 setting × count cycle
Count value
TCCP0
Up/Down-count mode
Time
FRT cycle ＝ TCCP0 setting × count cycle ×2

Figure 2 and Figure 3 show several output waveforms which use FRT and OCU. As shown in Figure 2, several OCU outputs can be synchronized with same one FRT. Figure 3 shows the example of waveform which three individual FRTs are used and three OCU outputs are synchronized with each operating FRT respectively. It should be noted that each FRT cannot be synchronized one another because each FRT channel has the start trigger bit in separate registers .

Figure 2. Example of waveforms which OCU 3 channels are synchronous with FRT 1 channel

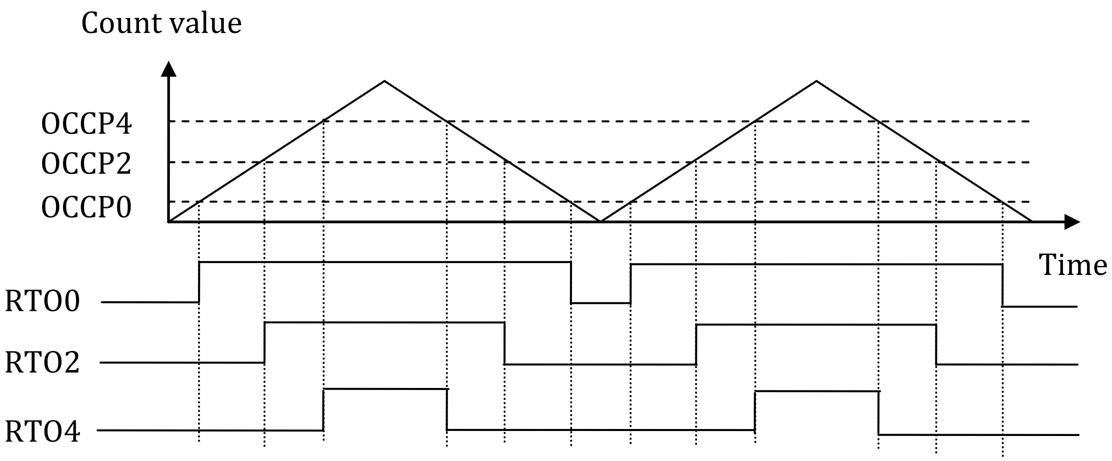
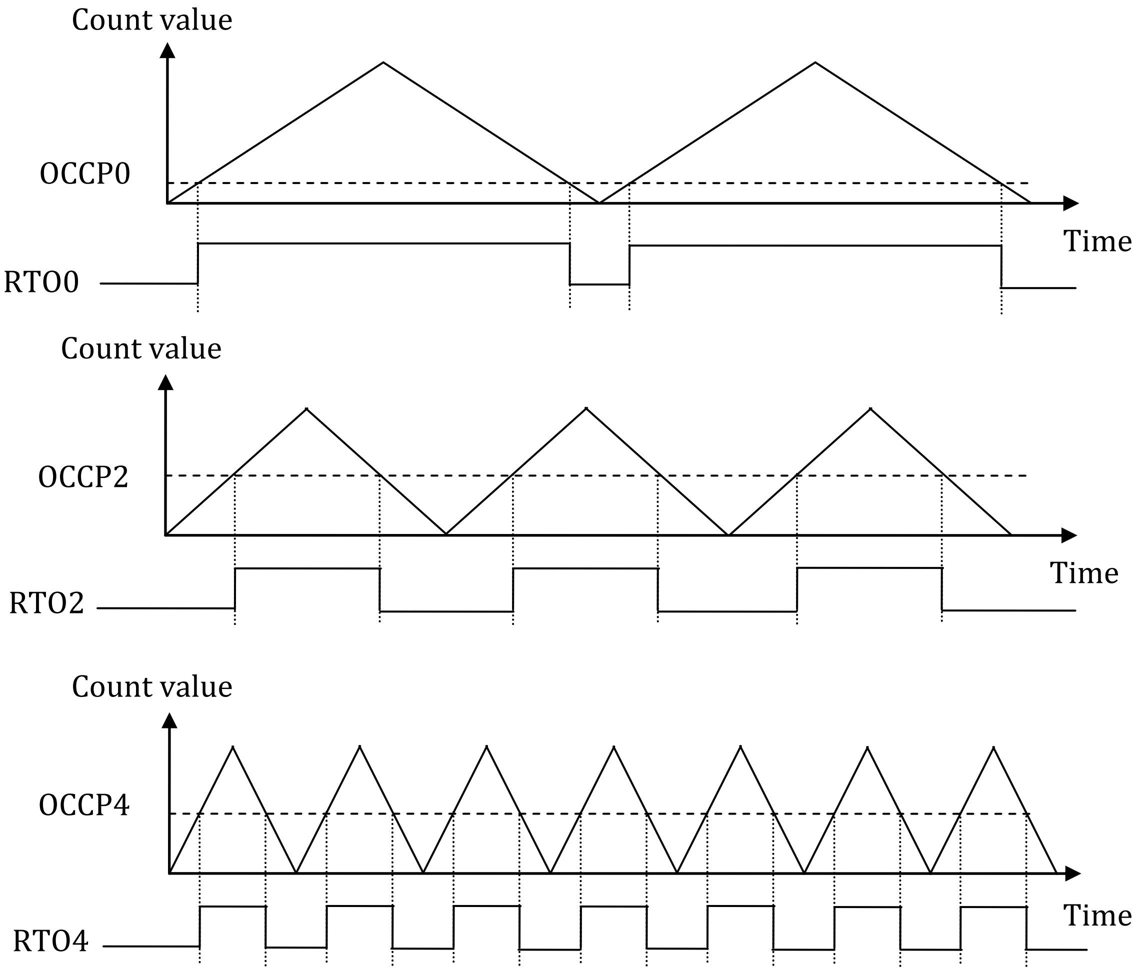


Figure 3. Example of waveforms which each OCU is synchronous with individual FRT channel



4.2 Register basic setup and example waveform output

Hereinafter it shows several examples of waveform. OCU channel 0, OCU channel 1 and FRT channel 0 are used.

As a register setting hereinafter, it is shown like “Register name = value”. Without any particular remark,

Φ = PCLK (peripheral clock) = 40MHz is supposed. In case that MFT is output, port function setting register (PFR) has to be set to enable peripheral input/output function, and extended port function setting register (EPFR) has to be set to enable MFT output function.

Example 1 of output waveform

< Setting of main registers >

TCCP0 = 0x7FFF // FRT cycle：0x7FFF ×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0 // FRT：Up/Down count mode

OCCP0 = 0x1000 // RTO0 L width 0x1000 ×1/40MHz ×2 = 0.20ms

OCCP1 = 0x3000 // RTO1 L width 0x3000 ×1/40MHz ×2 = 0.61ms

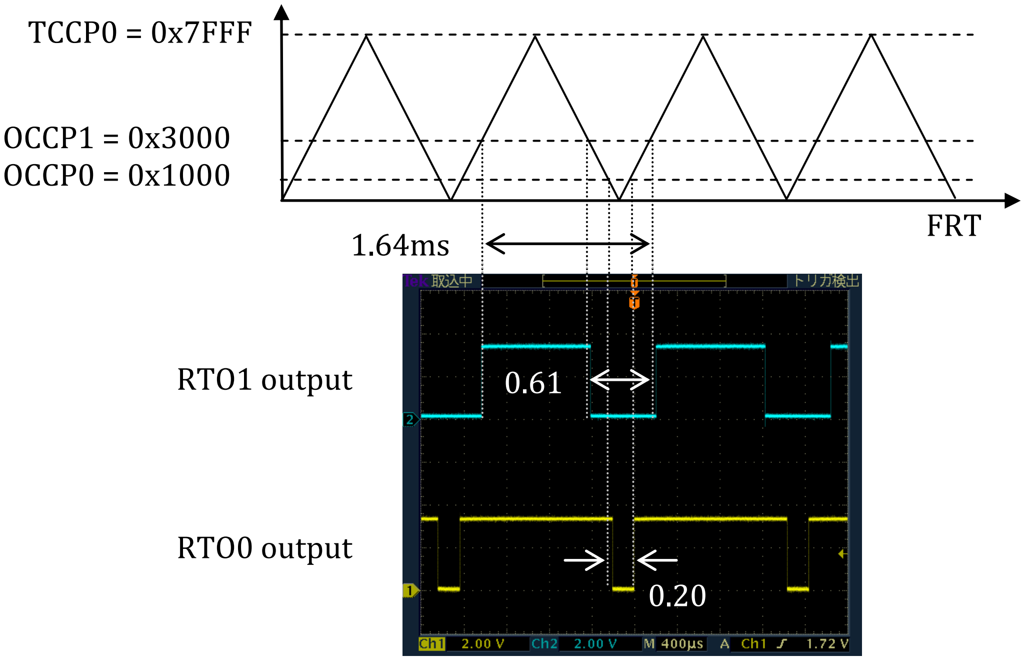
OCSA10 = 0x3F

OCSB10 = 0x60

OCSC10 = 0x00

Figure 4 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 4. Example 1 of output waveform



Example 2 of output waveform

The change from Example 1 of output waveform is only to write “1” to the CMOD bit in the OCSB10 register.

In case that OCSB10 : CMOD bit = 1 and OCSC10 : MOD bit = 0, output of RTO1 which belongs to odd-numbered channels inverts that polarity when OCCP0 or 1 register value matches FRT counter value.

< Setting of main registers >

TCCP0 = 0x7FFF //Cycle 0x7FFF ×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0 //FRT：Up/Down counter mode

OCCP0 = 0x1000 //RTO0 L width 0x1000 ×1/40MHz ×2 = 0.20ms

OCCP1 = 0x3000 //RTO1 H width 0x3000 ×1/40MHz ×2 = 0.61ms

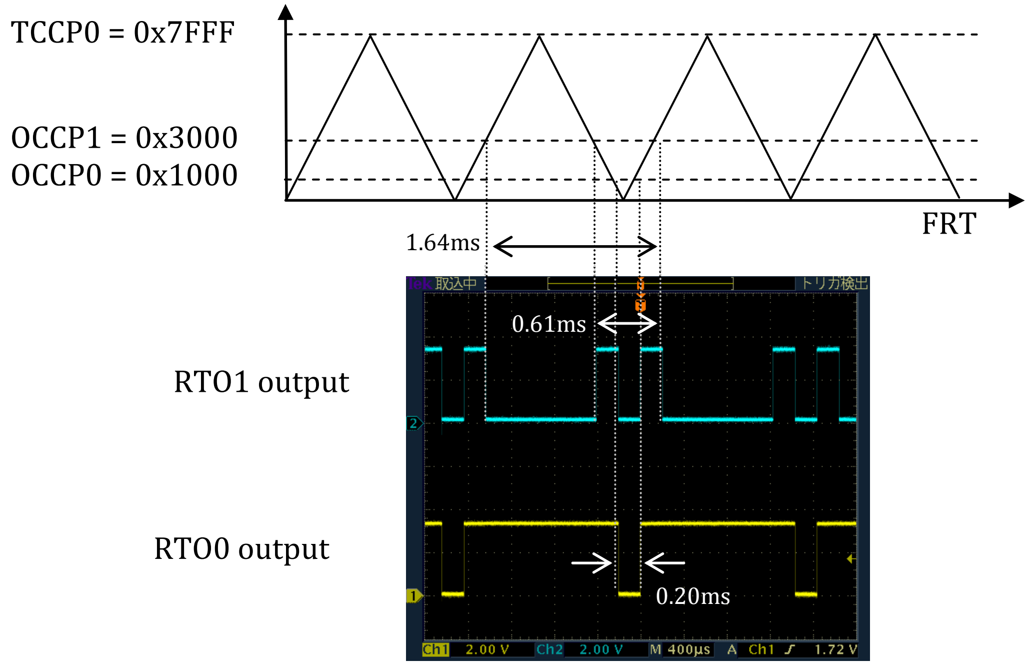
OCSA10 = 0x3F

OCSB10 = 0x70 //CMOD bit = 1

OCSC10 = 0x00

Figure 5 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 5. Example 2 of output waveform



Example 3 of output waveform

The change from Example 1 of output waveform is setting of each MOD bit in the OCSC10 register.

In case that OCSB10 : CMOD bit = 0 and OCSC10 : MOD bit = 1, when OCCP1 or OCCP0 register value matches FRT counter value, the output signal level of respective RTO1 and RTO0 is changed to “H” while FRT is up-counting, whereas “L” while FRT is down-counting.

< Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0 // FRT : Up/Down count mode

OCCP0 = 0x1000 // RTO0 L width 0x1000 ×1/40MHz ×2 = 0.20ms

OCCP1 = 0x3000 // RTO1 L width 0x3000 ×1/40MHz ×2 = 0.61ms

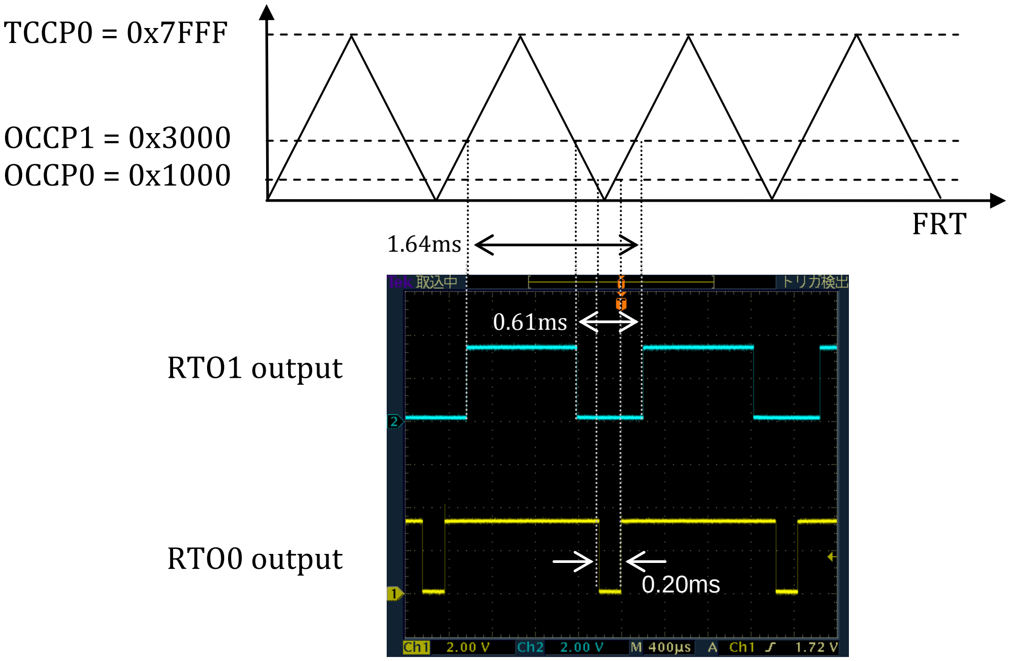
OCSA10 = 0x3F

OCSB10 = 0x60 // CMOD bit = 0

OCSC10 = 0x03 // each MOD bit = 1

Figure 6 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 6. Example 3 of output waveform



Example 4 of output waveform

The change from Example 1 of output waveform is setting of each MOD bit in the OCSC10 register and CMOD bit in the OCSB10 register. With these settings, the output signal is just inversion output of Example 3 of output waveform.

< Setting of main registers >

TCCP0 = 0x7FFF // Cycle 0x7FFF ×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0 // FRT : Up/Down counter mode

OCCP0 = 0x1000 // RTO0 H width 0x1000 ×1/40MHz ×2 = 0.20ms

OCCP1 = 0x3000 // RTO1 H width 0x3000 ×1/40MHz ×2 = 0.61ms

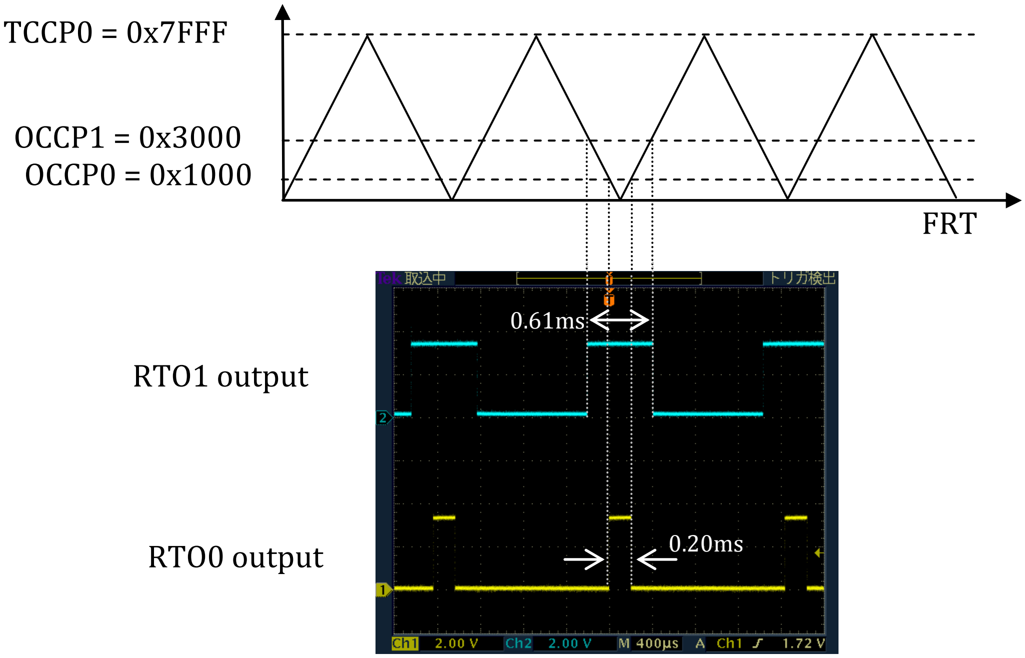
OCSA10 = 0x3F

OCSB10 = 0x70 // CMOD bit = 1

OCSC10 = 0x03 // each MOD bit = 1

Figure 7 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 7. Example 4 of output waveform



Example 5 of output waveform

The change from Example 1 of output waveform is setting of MODE bit in the TCSA0 register.

With these settings, FRT operates with Up-count mode.

< Setting of main registers >

TCCP0 = 0x7FFF // Cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0   // FRT：Up counter mode

OCCP0 = 0x1000 // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RTO1 L width = H width = 0.82ms,

                    // phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

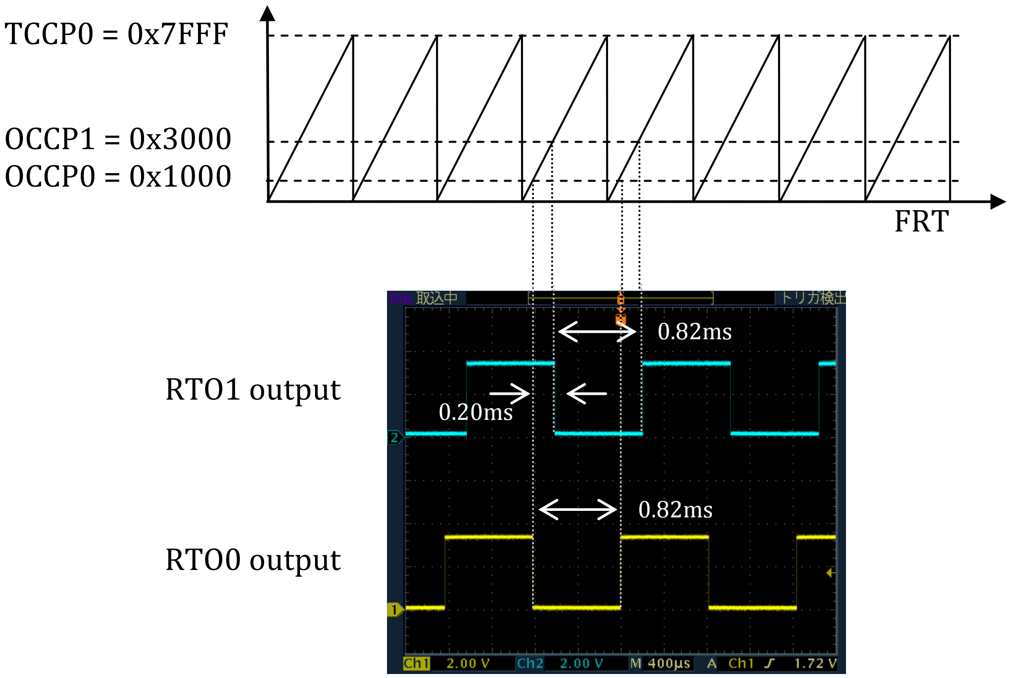
OCSA10 = 0x3F

OCSB10 = 0x60   // CMOD bit = 0

OCSC10 = 0x00   // each MOD bit = 0

Figure 8 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 8. Example 6 of output waveform



Example 6 of output waveform

The change from Example 5 of output waveform is to write “1” to CMOD bit in OSCB10 register. RTO0 (even-numbered channels) inverts the polarity when FRT counting value matches corresponding OCCP0 register value. Whereas RTO1 (odd-numbered channels) inverts the polarity at both timing when FRT counting value matches OCCP1 and OCCP0 register value respectively.

< Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT : up counter mode

OCCP0 = 0x1000 // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RTO1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

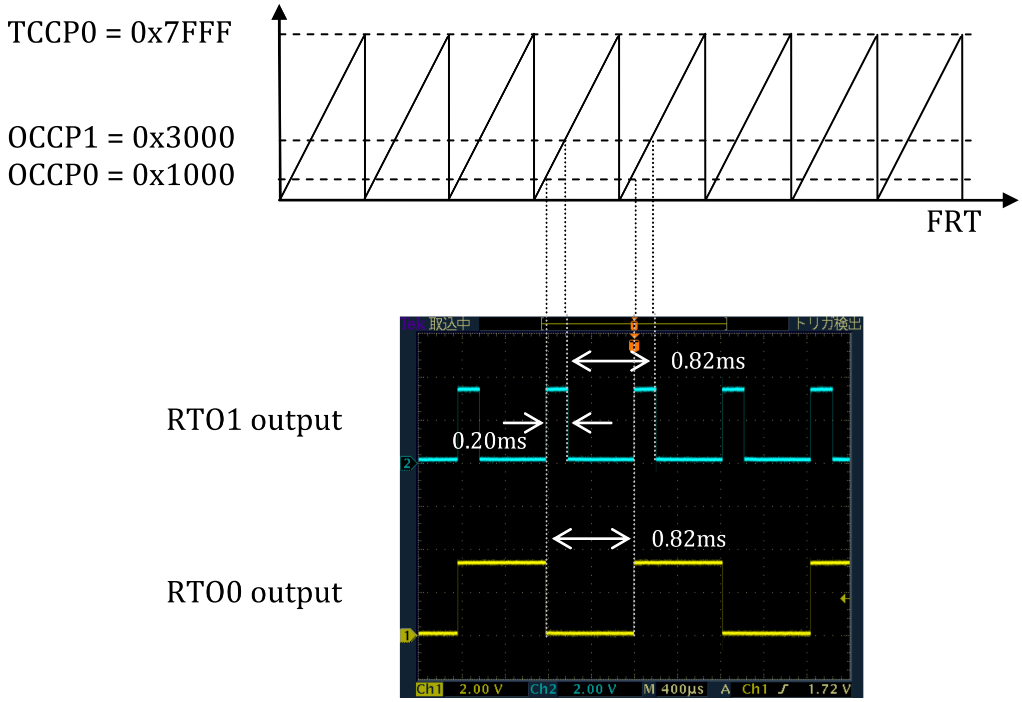
OCSA10 = 0x3F

OCSB10 = 0x70 // CMOD bit = 1

OCSC10 = 0x00 // each MOD bit = 0

Figure 9 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 9. Example 6 of output waveform



Example 7 of output waveform

The change from Example 5 of output waveform is setting of MOD bit in OCSC10 register.

In case that OCSB10 : CMOD bit = 0 and OCSC10 : MOD bit =1, when OCCP1 or OCCP0 register value matches FRT counter value, the output signal level of respective RTO1 and RTO0 is changed to “H” while FRT is up-counting, whereas “L” while FRT is down-counting. But since FRT is Up-count mode, both RTO1 and RTO0 are fixed to “H” only.

< Setting of main registers >

TCCP0 = 0x7FFF   // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0   // FRT：up count mode

OCCP0 = 0x1000   // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000   // RTO1 L width = H width = 0.82ms,

// phase difference from RTO0 : 0x2000 ×1/40MHz = 0.2ms

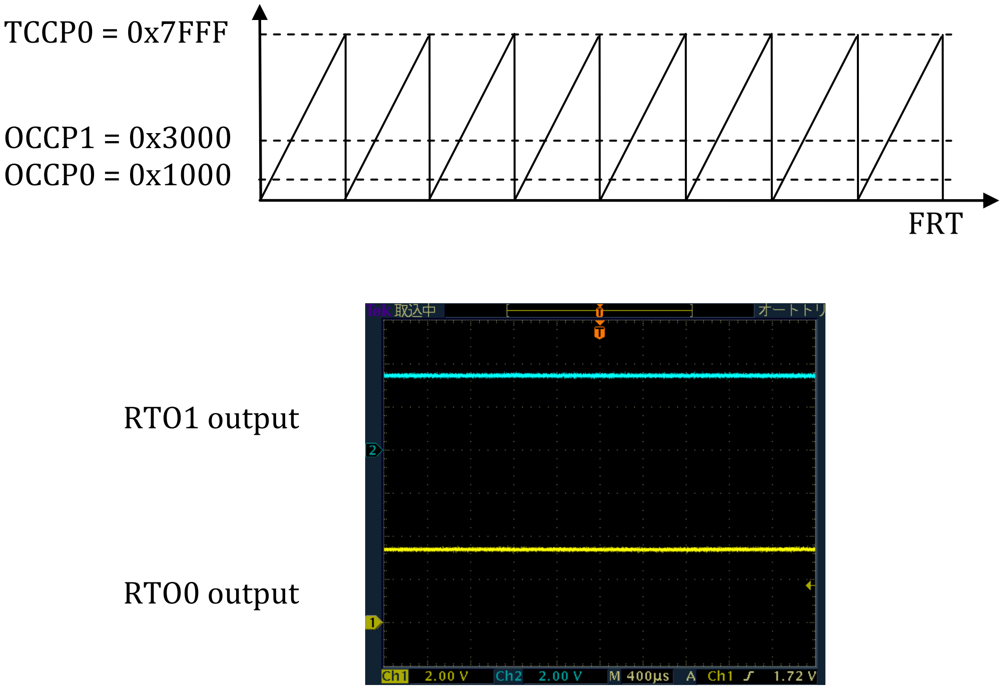
OCSA10 = 0x3F

OCSB10 = 0x60   // CMOD bit = 0

OCSC10 = 0x03   // each MOD bit = 1

Figure 10 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 10. Example 7 of output waveform



Example 8 of output waveform

The change from Example 5 of output waveform is setting of CMOD bit in OCSB10 register and each MOD bit in OCSC10 register. In case that OCSB10 : CMOD bit = 1 and OCSC10 : MOD bit =1, when OCCP1 or OCCP0 register value matches FRT counter value, the output signal level of respective RTO1 and RTO0 is changed to “L” while FRT is up-counting, whereas “H” while FRT is down-counting. But since FRT is Up-count mode, both RTO1 and RTO0 are fixed to “L” only.

< Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0   // FRT : up count mode

OCCP0 = 0x1000 // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RTO1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

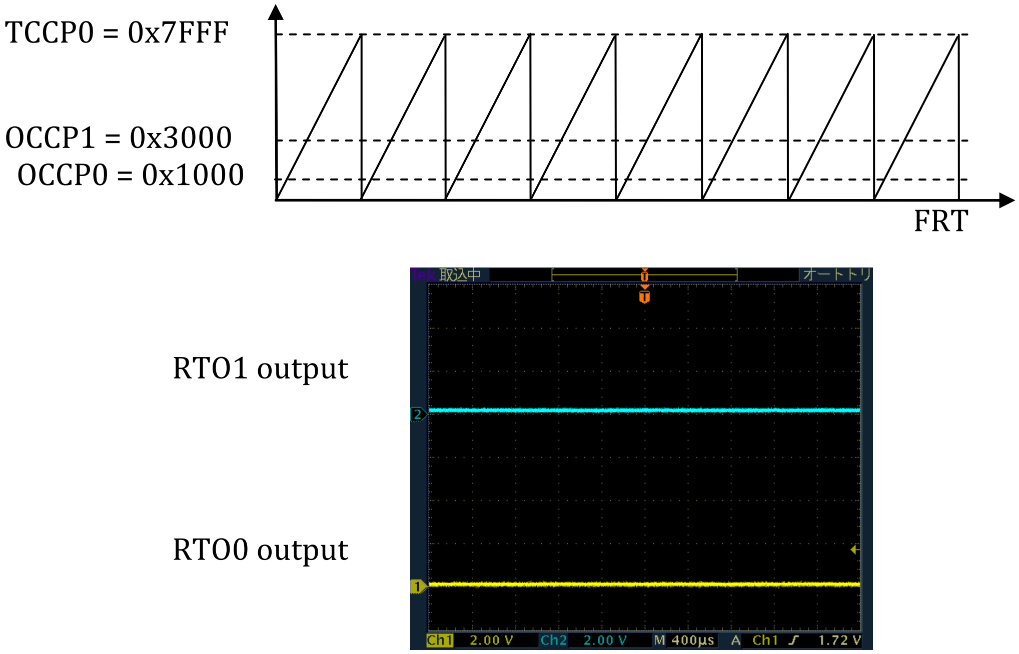
OCSA10 = 0x3F

OCSB10 = 0x60   // CMOD bit = 1

OCSC10 = 0x03   // each MOD bit = 1

Figure 11 shows the relation between RTO1 output, RTO0 output and FRT.

Figure 11. Example 8 of MFT output waveform



4.3 Dead Time Timer

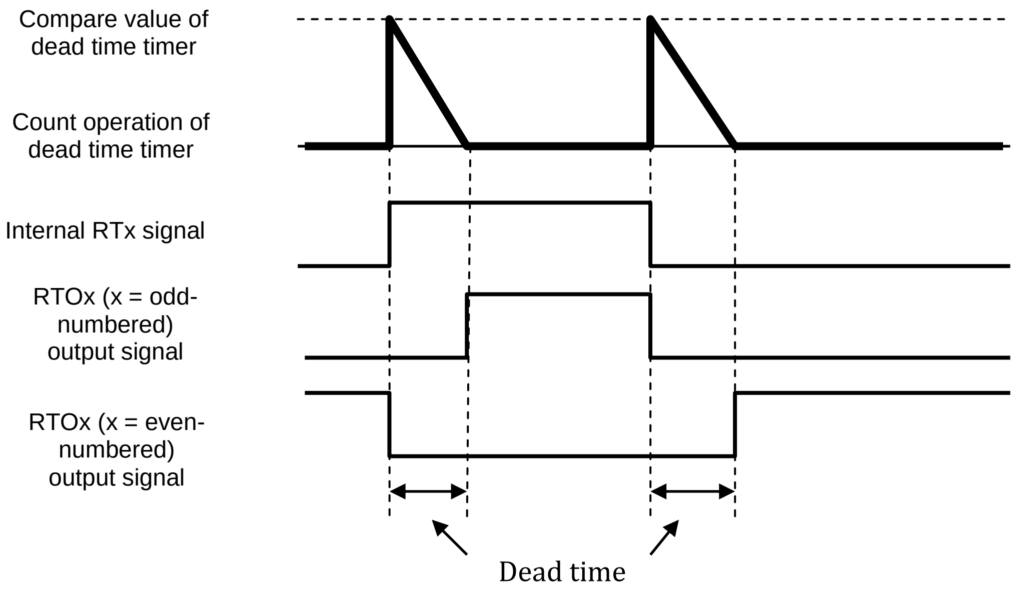
MFT has dead timer which can create non-overlapping output signal.

Each one channel of dead timer corresponds to one pair of output signal.

Since each MFT unit has three pairs (total 6 channels) of output signal, each MFT has 3 channels of dead timer block.

Note: Non-overlapping signal is to avoid the short circuit between H-side and L-side of the switching component like IGBT due to intrinsic switching delay. The appropriate span that both H-side and L-side output level remains “L” level is required.

Figure 12. Non-overlapping signal


Compare value of dead time timer
Count operation of dead time timer
Internal RTx signal
RTOx (x = odd-numbered) output signal
RTOx (x = even-numbered) output signal
Dead time

The dead time timer can be used as an internal interval timer unless the dead time is applied.

Hereinafter there are several examples of output waveform to which dead timer is applied along with sample program.

Example 9 of output waveform

In order to highlight RTO1 output and RTO0 output behavior, the description of only WFTM10 and WFSA10 register settings are added.

In case that the setting “010” is written to TMD [2:0] bits in WFSA10 register, the dead timer0 will start at the rising edge or internal RT1 and RT0 signal. Then “H” signal will be output from RTO1 and RTO0 until the overflow of dead timer counting.

< Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms）

TCSA0 = 0x21D0   // FRT：up count mode）

OCCP0 = 0x1000 // RT0 L width = H width = 0.82ms）

OCCP1 = 0x3000 // RT1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms）

OCSA10 = 0x3F

OCSB10 = 0x60   // CMOD bit = 0

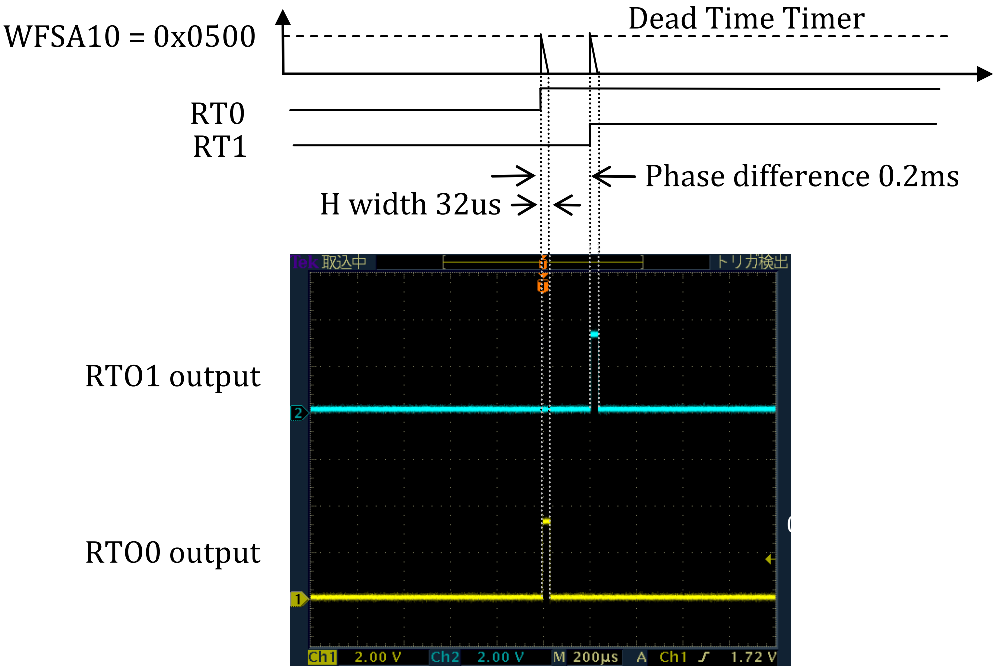
OCSC10 = 0x00   // each MOD bit = 0

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0010   // TMD = 0b010

Figure 13 shows the relation between RTO1 output, RTO0 output and dead time timer.

Figure 13. Example 9 of output waveform



Example 10 of output waveform

The change from Example 9 of output waveform is to write “1” to the CMOD bit in OCSB10 register.

RTO0 (even-numbered channels) inverts the polarity when FRT counting value matches corresponding OCCP0 register value. Whereas RTO1 (odd-numbered channels) inverts the polarity at both timing when FRT counting value matches OCCP1 and OCCP0 register value respectively. The dead timer starts at the rising edge of respective RT1 and RT0 signal, then “H” signal will be output from RTO1 and RTO0 until the overflow of dead timer counting.

<Setting of main registers>

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT：up count mode

OCCP0 = 0x1000 // RT0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RT1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

OCSA10 = 0x3F

OCSB10 = 0x70 // CMOD bit = 1

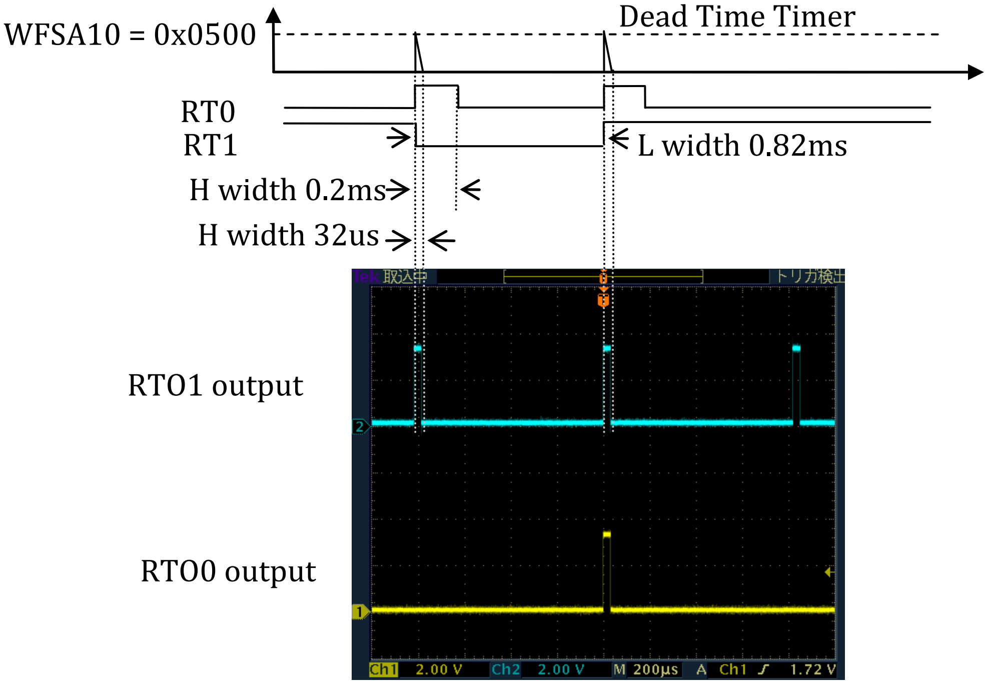
OCSC10 = 0x00 // each MOD bit = 0

WFTM10 = 0x0500 // cycle 0x500×1/40MHz = 32us

WFSA10 = 0x0010 // TMD = 0b010

Figure 14 shows the relation between RTO1 output, RTO0 output and dead time timer.

Figure 14. Example 10 of output waveform



Example 11 of output waveform

In case OCSB10 : CMOD bit = 0 and OCSC10 : MOD bit = 1, since FRT is Up-count mode, RT signals are fixed to "1" (same as Example 7 of output waveform). Therefore, since dead timer doesn't start, output signals are fixed to "L".

<Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT : up count mode

OCCP0 = 0x1000 // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RTO1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

OCSA10 = 0x3F

OCSB10 = 0x60 // CMOD bit = 0

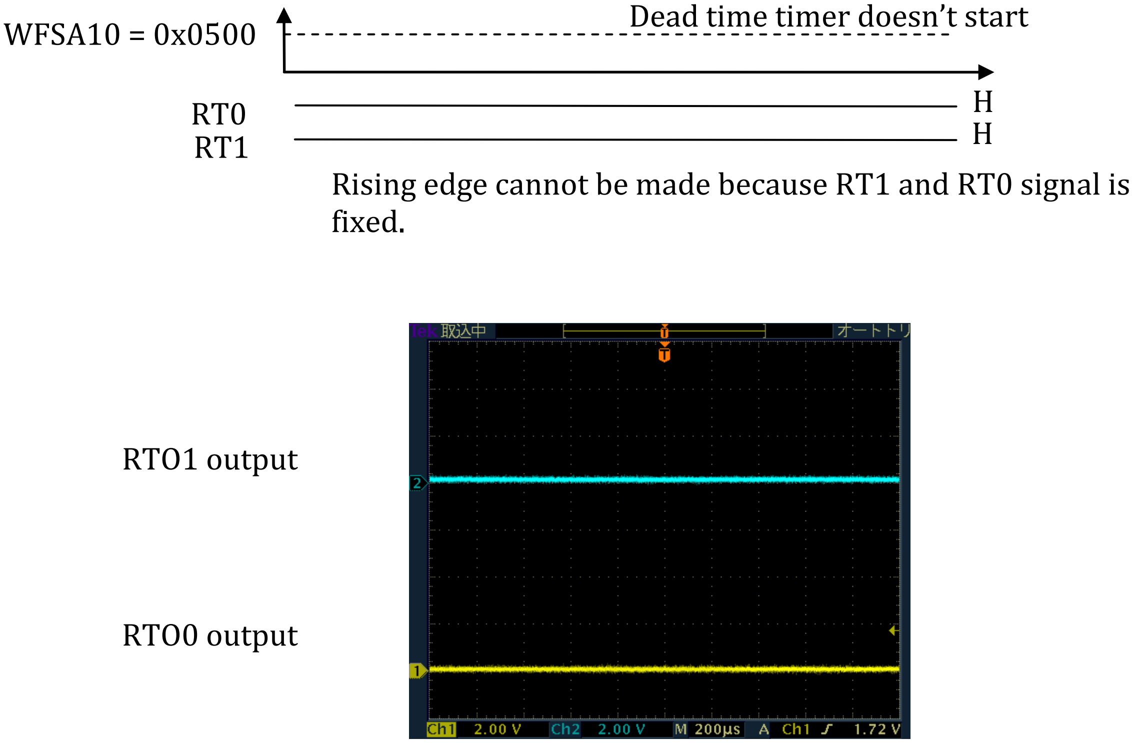
OCSC10 = 0x03 // each MOD bit = 1

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0010 // TMD = 0b010

Figure 15 shows the relation between RTO1 output, RTO0 output, dead time timer.

Figure 15. Example 11 of MFT output waveform



Example 12 of output waveform

In case OCSB10 : CMOD bit = 0 and OCSC10 : MOD bit = 1, since FRT is Up-count mode, RT signals are fixed to "0" (same as Example 8 of output waveform). Therefore, since dead timer doesn't start, output signals are fixed to "L". (As a result, the waveform is same as Example 11 of output waveform)

<Setting of main registers>

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT : up count mode

OCCP0 = 0x1000 // RTO0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RTO1 L width = H width = 0.82ms,

// phase difference with RTO0 : 0x2000 ×1/40MHz = 0.2ms

OCSA10 = 0x3F

OCSB10 = 0x70 // CMOD bit = 1

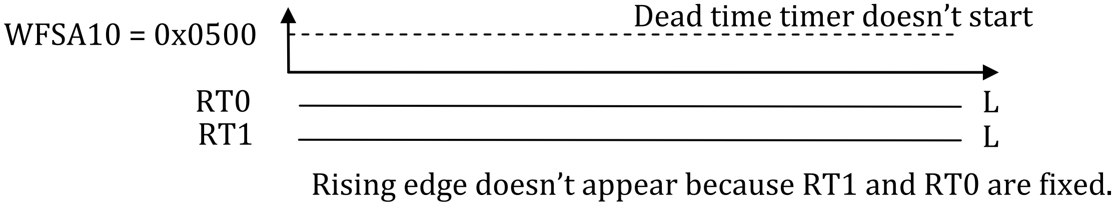
OCSC10 = 0x03 // each MOD bit = 1

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0010 // TMD = 0b010

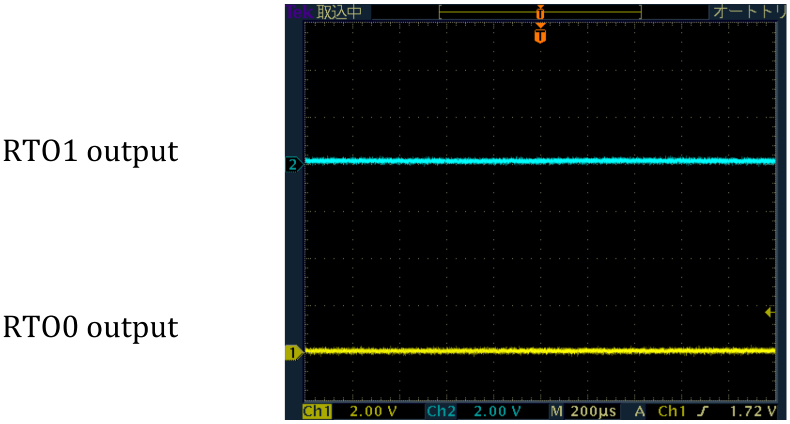
Figure 16 shows the relation between RTO1 output, RTO0 output and dead time timer.

Figure 16. Example 12 of output waveform



Dead time timer doesn't start

Rising edge doesn't appear because RT1 and RT0 are fixed.



Example 13 of output waveform

Non-overlapping signal can be generated by RT1 signal on condition of that the setting “100” is written to TMD [2:0] bits in WFSA10 register and CMOD bit in OCSB10 register is set to “1”.

The example of dead timer is shown on condition of that FRT is Up/Down count mode.

<Setting of main registers>

TCCP0 = 0x7FFF   // cycle 0x7FFF ×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0   // FRT：Up/down count mode

OCCP0 = 0x1000

OCCP1 = 0x3000   // RTO1 H width 0x3000×1/40MHz ×2 = 0.61ms

OCSA10 = 0x3F

OCSB10 = 0x70   // CMOD bit = 1

OCSC10 = 0x03   // each MOD bit = 1

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0020   // TMD ＝0b100

Figure 17 shows the relation between RTO1 output, RTO0 output and dead time timer.

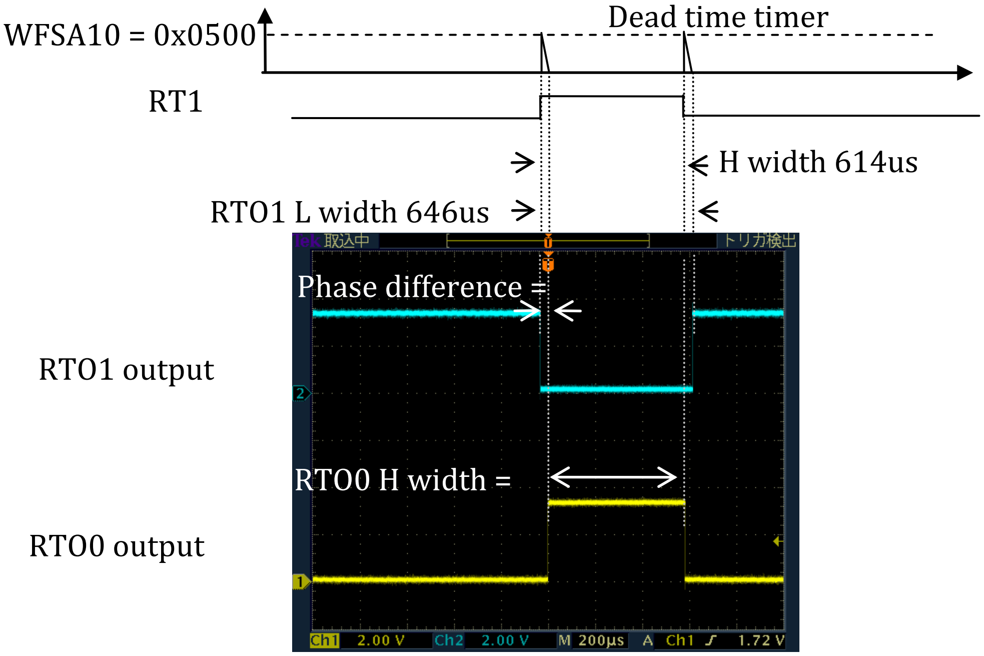
The phase difference between RTO1 output and RTO0 output is twice as much as the value made by dead time timer.

RTO1 output L width：RTO1 H width (0.61ms) ＋dead timer cycle (32us) ＝646us

RTO0 output H width：RTO1 H width (0.61ms) - dead timer cycle (32us) ＝582us

The output level of RTO1 and RTO0 will be inverted if DMOD bit in DTCR register is set to “1”.

Figure 17. Example 13 of output waveform



4.4 Cooperation with PPG timer function

MFT connects to PPG (PPG：Programmable Pulse Generator) internally and has the capability to output PPG timer waveform from RTOx output pin .

Hereinafter the cooperated function between MFT and PPG is shown along with examples of output waveform.

There are 3 ways of PPG timer start-up as follow,

- start-up by software trigger bit
(setting PEN bit in TRG register)

- start-up by timing generator
(simultaneous start-up is enable)

- start-up by internal GATE signal from MFT
(It is necessary to enable this function on GATEC register)

The way of GATE signal generation is up to the combination of TMD bit and GTEN bit in WFSA10 register.

Example 14 of output waveform

PPG waveform is output from RTO pin on condition of the combination of TMD bit, GTEN bit and PGEN bit in WFSA10 register.

In the following example, PPG timer starts beforehand. Then PPG signal is output from RTO0 pin only while internal RT0 signal is “H” level.

< Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT：up count mode

OCCP0 = 0x1000

OCCP1 = 0x3000 // RTO1 H width 0x3000 ×1/40MHz ×2 = 0.61ms

OCSA10 = 0x3F

OCSB10 = 0x60 // CMOD bit = 0

OCSC10 = 0x00 // each MOD bit = 0

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0408 // TMD ＝0b001, PGEN = 0b01：enable RT0 to output PPG

PPGC0 = 0x00

PRLL0 = 0x80 // PPG L width 0x80 ×1/40MHz = 3us

PRLH0 = 0x80 // PPG H width 0x80 ×1/40MHz = 3us

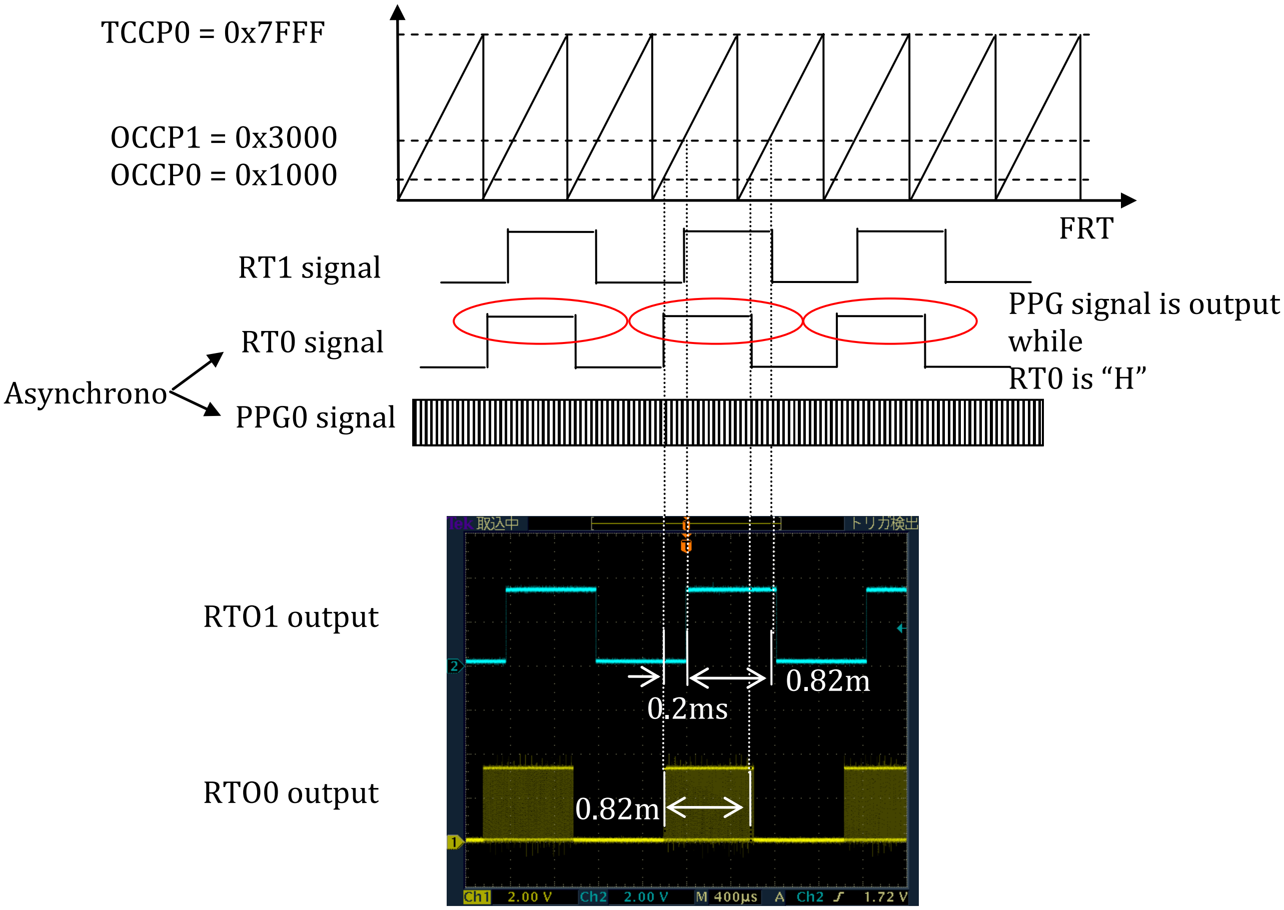
GATEC0 = 0x00 // start-up PPG by TRG register

(It is necessary to start up PPG timer beforehand .)

Figure 18 shows the relation between RTO1 output, RTO0 output and each timer.

Since RTO1 pin is not set to enable PPG output, the internal RT1 signal is output to RTO1 output terminal as it is.

Figure 18. Example 14 of output waveform



Example 15 of output waveform

In the following example, PPG signal is output from RTO0 pin only while internal RT0 signal is “H” level.

The difference with example 15 of output waveform is that PPG timer start-up trigger is not software but GATE signal from RT0. Use this setting in case PPG start-up and MFT are synchronized.

<Setting of main registers>

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT：up count mode

OCCP0 = 0x1000

OCCP1 = 0x3000 // RTO1 H width 0x3000 ×1/40MHz ×2 = 0.61ms

OCSA10 = 0x3F

OCSB10 = 0x60 // CMOD bit = 0

OCSC10 = 0x00 // each MOD bit = 0

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0408 // TMD ＝0b001, PGEN = 0b01：enable PPG output on RT0 pin, GTEN = 0b10

PPGC0 = 0x00

PRLL0 = 0x80 // PPG L width 0x80 ×1/40MHz = 3us

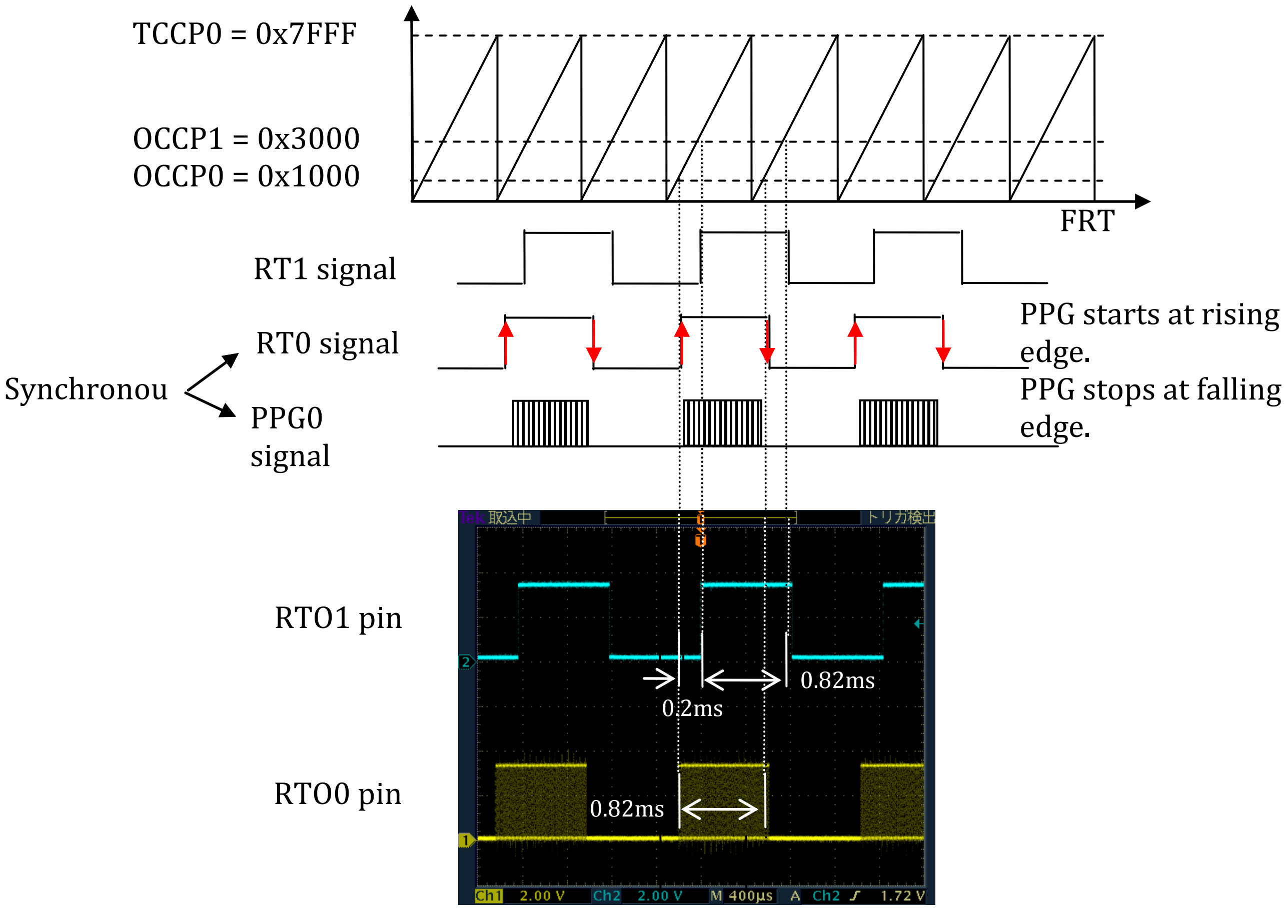
PRLH0 = 0x80 // PPG H width 0x80 ×1/40MHz = 3us

GATEC0 = 0x02 // start-up by MFT GATE signal

Figure 19 shows the relation between RTO1 pin, RTO0 pin and each timer.

Since RTO1 pin is not set to enable PPG output, the internal RT1 signal is output to RTO1 output terminal as it is.

Figure 19. Example 15 of output waveform



Example 16 of output waveform

The dead timer starts at the rising edge of RT1 and RT0 on condition of that TMD[2:0] bits in WFSA0 register is set to “010”.

In case GTEN bit in WFSA10 register is set to “0” and PGEN bit in WFSA10 register is set to “1”, PPG signal is output from RTO0 pin until the underflow of dead timer counting.

<Setting of main registers>

TCCP0 = 0x7FFF // cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0   // FRT：up count mode

OCCP0 = 0x1000

OCCP1 = 0x3000 // RTO1 H width 0x3000 ×1/40MHz ×2 = 0.61ms

OCSA10 = 0x3F

OCSB10 = 0x60   // CMOD bit = 0

OCSC10 = 0x00   // each MOD bit = 0

WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0410   // TMD ＝0b010, PGEN = 0b01：enable RT0 to output PPG, GTEN = 0b00

PPGC0 = 0x00

PRLL0 = 0x80   // PPG L width 0x80 ×1/40MHz = 3us

PRLH0 = 0x80   // PPG H width 0x80 ×1/40MHz = 3us

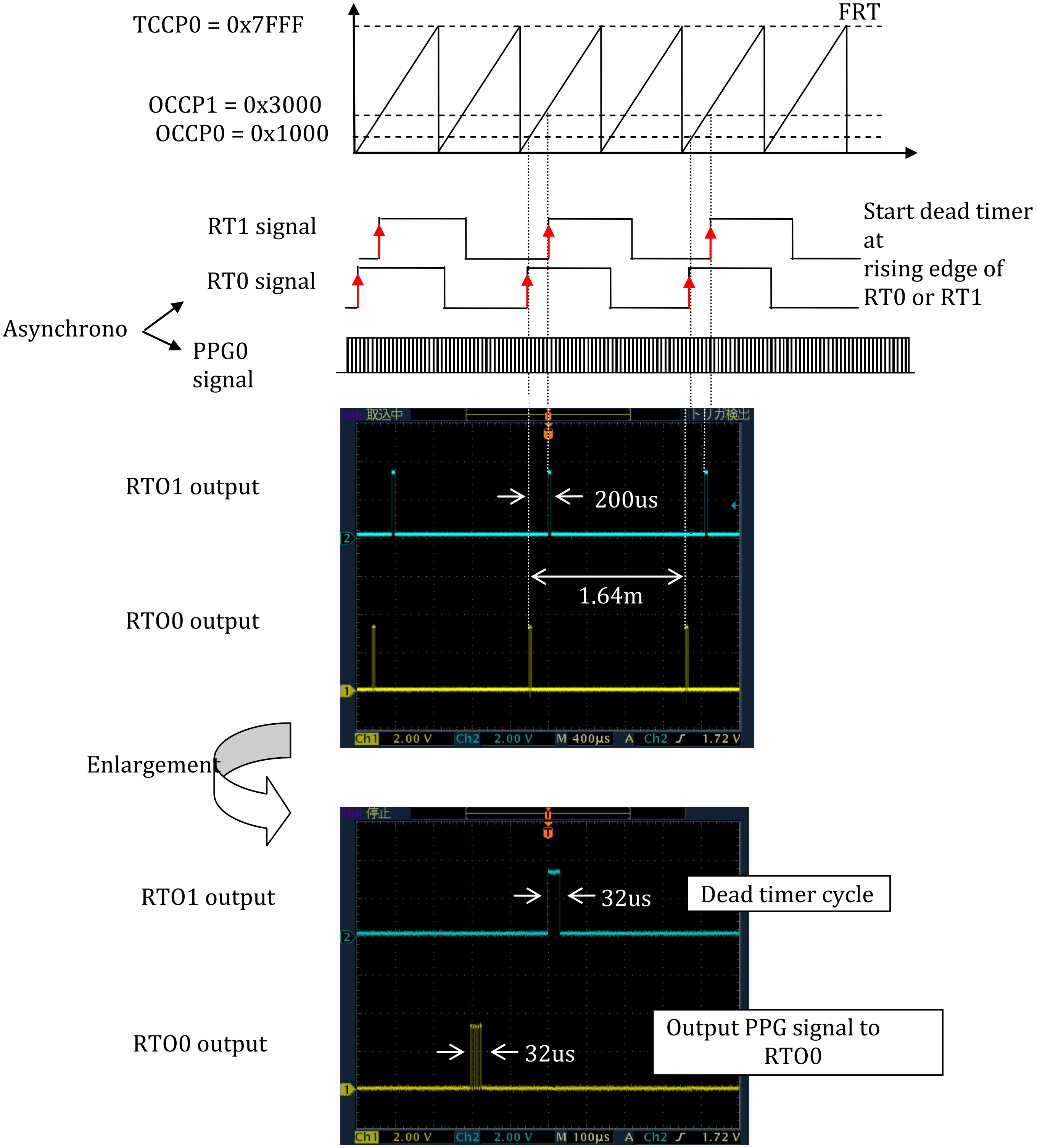
GATEC0 = 0x00   // start up PPG with TRG register

(PPG is necessary to be started up beforehand.)

Figure 20 shows the relation between RTO1 pin, RTO0 pin and dead timer.

Since RTO1 pin is not set to enable PPG output, RTO1 outputs “H” until the underflow of dead timer.

Figure 20. Example 16 of output waveform



Example 17 of output waveform

In case that TMD[2:0] bits are set to “010”, GTEN bit is set to “1” and PGEN bit is set to “1”,

the dead timer starts at the rising edge of RT1 and RT0, then PPG signal is output from RTO0 until the underflow of dead timer counting.

The difference with Example 16 of output waveform is that start trigger of PPG timer is not software, but GATE signal from RT0. Use this setting in case PPG start-up and MFT are synchronized.

In case multiple GTEN bits are set to “1”, the GATE signal becomes logical OR of all corresponding timers’ signals.

< Setting of main registers >

TCCP0 = 0x7FFF //cycle 0x7FFF ×1/40MHz = 0.82ms

TCSA0 = 0x21D0 // FRT：Up-count mode

OCCP0 = 0x1000 // RT0 L width = H width = 0.82ms

OCCP1 = 0x3000 // RT1 L width = H width = 0.82ms,

// phase difference with RT0 : 0x200 × 1/40MHz = 0.2ms

OCSA10 = 0x3F

OCSB10 = 0x60 // CMOD bit = 0

OCSC10 = 0x00 // each MOD bit = 0

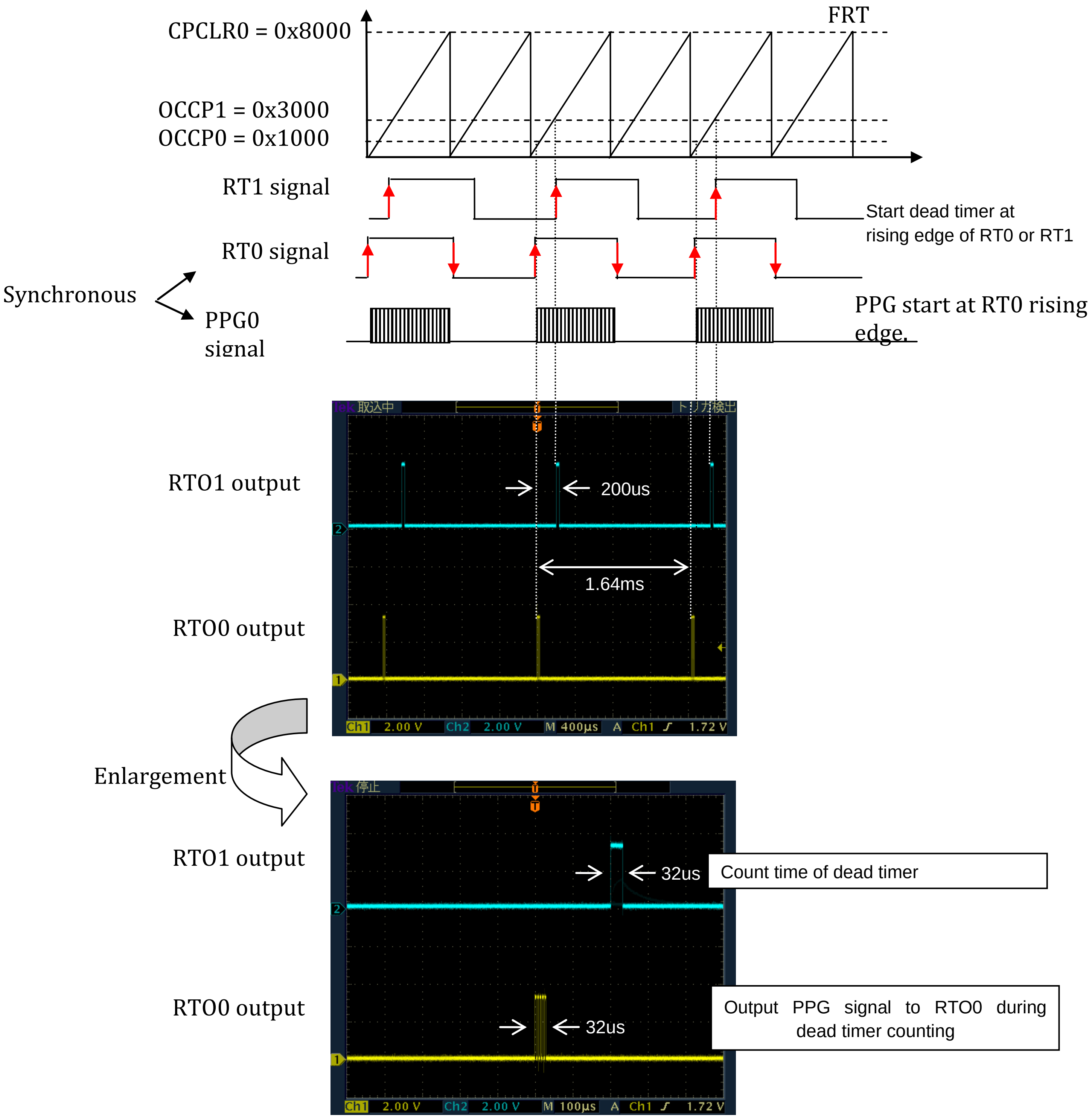
WFTM10 = 0x0500 // cycle 0x500 ×1/40MHz = 32us

WFSA10 = 0x0450 // TMD = 0b010, PGEN = 0b01：enable RT0 to output PPG, GTEN = 0b01

Figure 21 shows the relation between RTO1 , RTO0 and dead timer.

Since RTO1 pin is not set to enable PPG output, RTO1 outputs “H” until the underflow of dead timer.

Figure 21. Example 17 of output waveform



4.5 Cooperation with ADC function

MFT connects internally with ADC and can start ADC synchronizing with PWM signal output.

Hereinafter the example of FRT and ADC activation compare function is shown.

<Setting of main registers >

TCCP0 = 0x7FFF // cycle 0x7FFF×1/40MHz ×2 = 1.64ms

TCSA0 = 0x21F0 // FRT：Up/Down-count mode

ACSA = 0x0100 // compare during Up-counting

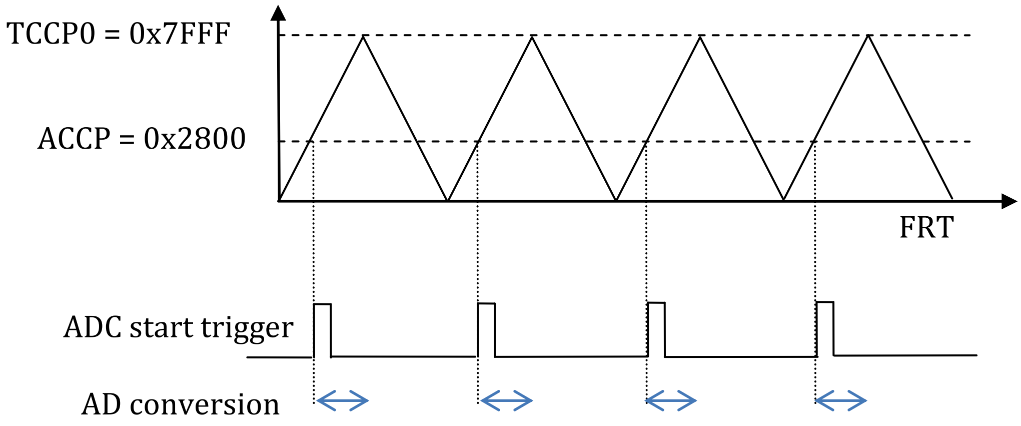
ACSB = 0x0000 // buffer function：disable

ACCP = 0x2800 // specify start time for ADC

ATSA = 0x0000

Figure 22 shows the relation of ADC activation trigger and FRT.

Figure 22. The relation of ADC activation trigger and FRT



4.6 Three- phase motor control（sample program of Sine Wave）

1 unit of MFT can generate the PWM waveforms which can control the three-phase motor drivers.

Hereinafter, with showing sample program using look-up table corresponding to sample sine wave, three-phase PWM waveforms, RTO5 to RTO0 (odd-numbered pins and even-numbered pins are reverse polarity respectively), are shown.

The PWM waveform equivalent to sine wave can be generated with loading sequentially the look-up table value corresponding to sine wave to OCCP registers.

Figure 23 shows the example of PWM waveform which OCU outputs and corresponding sine wave.

Figure 24 shows three-phase motor control sine waves which are phase-shifting 120 degrees each other and corresponding PWM output waveforms from WFG.

Figure 23. Sine waveform and PWM waveform

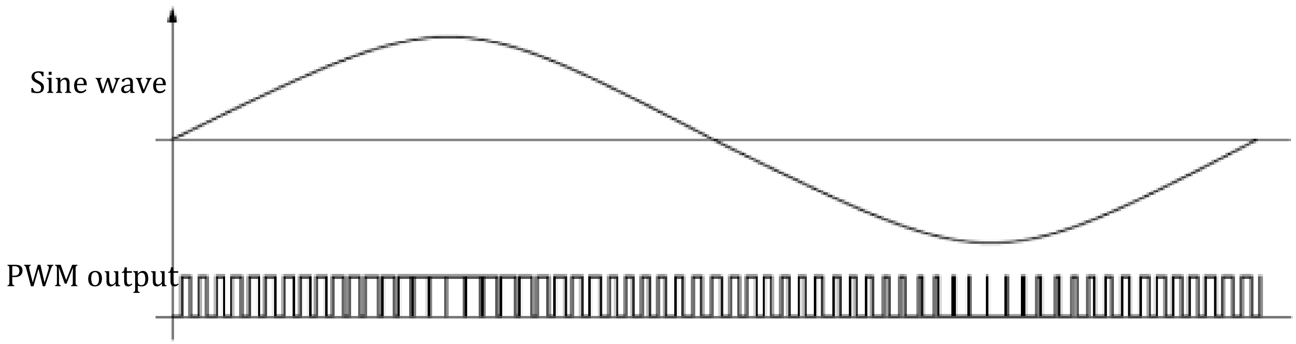
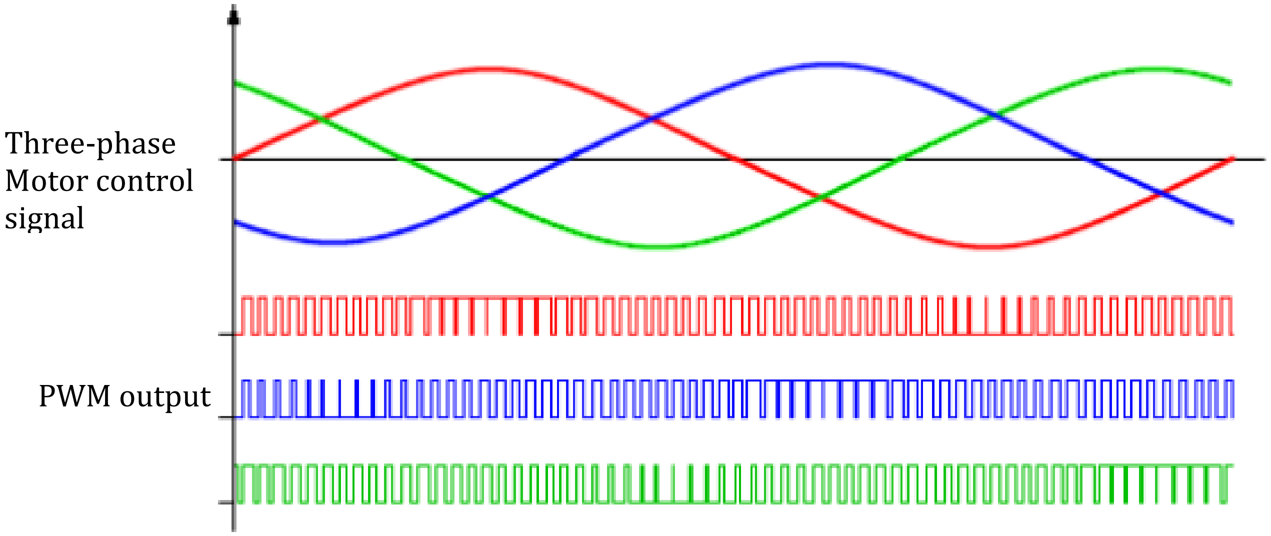


Figure 24. Three-phase motor control signals and PWM waveforms



In this sa

FRT : Up/Down-count mode, enable interruption

OCU : Up/Down-count mode (Active High), disable interruption

WFG : RT-dead timer mode (Active High)

ADCMP/ATSA：instruct ADC unit0 to start scan conversion under match condition during up-counting.

<Setting of main registers >

****

・ Set Up/Down-count mode on FRT channel 0. Enable the interruption of zero detection.

・ Set the operation cycle on FRT channel 0. In this sample, “0x5FFF” is set. On condition of that the FRT clock prescaler setting = 1/4 and PCLK = 40MHz, the count cycle of FRT is 4.915ms.

****

TCCP0 = 0x5FFF // cycle 0x5FFF ×1/40MHz ×2 ×4 = 4.915ms

TCSA0 = 0x20F2 // FRT：Up/Down count mode, FRT clock prescaler setting：1/4,

// Zero detection interruption：enable

****

・Connect FRT channel 0 to OCU channel 1, 3, 5

・Setting Up/Down mode (Active High) to OCU channel 1,3,5.
Setting initial output level on output signal (RT1, RT3, RT5).

****

OCFS10 = 0x0000 // connect FRT channel 0 to each OCU channels.

OCFS32 = 0x0000 // connect FRT channel 0 to each OCU channels.

OCFS54 = 0x0000 // connect FRT channel 0 to each OCU channels.

OCSA10 = 0x02 // OCCP buffer function : enable, OCU channel 1 : enable the operation

OCSA32 = 0x02 // OCCP buffer function : enable, OCU channel 1 : enable the operation

OCSA54 = 0x02 // OCCP buffer function : enable, OCU channel 1 : enable the operation

```
OCSB10 = 0x00    // RT1 output level : Low,  buffer transfer : at Zero value detection
OCSB32 = 0x00    // RT1 output level : Low,  buffer transfer : at Zero value detection
OCSB54 = 0x00    // RT1 output level : Low,  buffer transfer : at Zero value detection
OCSC = 0x2A      // operation mode of OCU channel 1,3,5 : Up/Down mode (Active High )
*******************************************************************************************************************
 ・Setting the change timing of OCU output signal on RT1, RT3, RT5.
 ・The setting value on buffer registers will be transferred to each corresponding OCCP1, OCCP3 and
  OCCP5 registers at zero value detection.
******************************************************************************************************************
OCCP1 = 0x4800
OCCP3 = 0x4800
OCCP5 = 0x4800
*******************************************************************************************************************
 ・Initial setting of RT-dead timer mode (Active High) on each WFG channel.
 ・In this WFG mode, the even-numbered channels output the same polarity of RT1, RT3 and RT5
  respectively, whereas the odd-numbered channels output reverse polarity.
*******************************************************************************************************************
WFSA10 = 0x0021     // TMD = 0b100, PGEN = 0b00, PSEL = 0b00, GTEN = 0b00, DCK = 0b001）
WFSA32 = 0x0021     // TMD = 0b100, PGEN = 0b00, PSEL = 0b00, GTEN = 0b00, DCK = 0b001）
WFSA54 = 0x0021     // TMD = 0b100, PGEN = 0b00, PSEL = 0b00, GTEN = 0b00, DCK = 0b001）
*******************************************************************************************************************
 ・ Setting the dead time on each WFG channels. In this example, since “0x0014” is set, the inserted
   dead time is 1.0us on condition of that WFG prescaler setting is 1/2 and PCLK = 40MHz.
*******************************************************************************************************************
WFTM10 = 0x0014     // dead time cycle   (0x14 ×1/40MHz ×2 = 1.0us)
WFTM32 = 0x0014     // dead time cycle   (0x14 ×1/40MHz ×2 = 1.0us)
WFTM54 = 0x0014     // dead time cycle   (0x14 ×1/40MHz ×2 = 1.0us)
 ・ Setting each register of ADCMP channel 0 to operate ADC unit-0 when FRT value matches
   ACCP0 value at FRT up-count only.
   (Note) In this sample program, there is just start trigger of AD conversion.
        No actual ADC operation is implemented.
*******************************************************************************************************************
```

```
ACSA  = 0x0001      // ADC start trigger : at FRT Up-count mode only
ACSB  = 0x0000      // buffer function : disable
ACCP0 = 0x2800       // specify start trigger timing of ADC0
ATSA  = 0x0000      // select scan conversion start signal as ADC’s start signal from ADCMP
```

****

In MFT/FRT interrupt handler

・ FRT channel 0 generates the interruption of zero value detection when count value becomes “0”.

(Note) The interruption of zero value detection will not be generated on 1st Zero value before FRT starts counting.

・ Reload next value on look-up table corresponding to sine wave to OCCP1, OCCP3 and OCCP5 respectively in this interrupt handler.

・ Clear the zero value detection flag and return to main routine.

****

```
TCSA0 : IRQZF bit = 0        // clear Zero value detection flag
OCCP1  = sinVal1        // reloaded value from Sin-wave look-up table
                        // (phase difference of 120 degrees from sinVal5)
OCCP3  = sinVal3        // phase difference of 120 degrees from sinVal1
OCCP5  = sinVal5        // phase difference of 120 degrees from sinVal3
```

5 Additional Information

For more information on FM3 32-bit ARM® Cortex®-M3 Microcontroller (MCU) Families, and the sample programs, please visit our website:

http://www.cypress.com/products/fm3-32-bit-arm-cortex-m3-microcontroller-mcu-families

6 Document History

Document Title: AN204430 - FM3 Microcontroller PWM Waveform Generation by Multi-function Timer

Document Number: 002-04430

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	_	YUIS	03/12/2014	Initial release
*A	5036015	YUIS	06/14/2016	Converted Spansion Application Note “FM3_AN706-00081” to Cypress format
*B	5874551	AESATMP9	09/06/2017	Updated logo and copyright.

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