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Errata

This errata sheet is for F²MC-16FX Family Programming Manual Rev. 3 (CM44-00203-3E).

F²MC-16FX
16-BIT MICROCONTROLLER
PROGRAMMING MANUAL

2011.1.17
: Collected Part

Date	Page	Item	Description
2011/ 1/17	38	5.1	"• String manipulation instructions" was corrected as corrected by the shading below. (Error) • String manipulation instructions MOVS MOVSW SCEQ SCWEQ FILS FILSW (Correct) • String manipulation instructions MOVS MOVSD MOVSW MOVSWD SCEQ SCEQD SCWEQ SCWEQD FILS FILSW
2011/ 1/17	40	5.2	"• String manipulation instructions" was corrected as corrected by the shading below. (Error) • String instructions MOVS NOVSW SCEQ FILS FILSW If an interrupt is requested during execution of a string manipulation instruction attached with a prefix code, the prefix becomes ineffective for the string manipulation instruction after a return is made from the interrupt handling routine, possibly resulting in a malfunction. Do not place the CMR prefix before these string manipulation instructions. (Correct) • String manipulation instructions MOVS MOVSD MOVSW MOVSWD SCEQ SCEQD SCWEQ SCWEQD FILS FILSW Placing a CMR prefix before the string manipulation instructions listed above is ignored. Counter register RW0 is referred always using actual value of the register bank pointer (RP), regardless of a CMR prefix is specified or not.
2011/ 1/17	40	5.2	"• Stack manipulation instructions" was added as below. • Stack manipulation instructions LINK UNLINK Placing a CMR prefix before the stack manipulation instructions listed above is ignored. Frame pointer RW3 is referred always using actual value of the register bank pointer (RP), regardless of a CMR prefix is specified or not.

Date	Page	Item	Description
2011/ 1/17	41	5.3	"• String manipulation instructions" was corrected as corrected by the shading below. (Error) • String instructions SCEQ SCWEQ FILS FILSW (Correct) • String manipulation instructions SCEQ SCEQD SCWEQ SCWEQD FILS FILSW
2011/ 1/17	154	8.42	The following item was added to "FILS, FILSI (Fill String Byte)". ● Malfunction of instruction execution In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

Date	Page	Item	Description
2011/ 1/17	156	8.43	The following item was added to “FILSW, FILSWI (Fill String Word)”. ● Malfunction of instruction execution In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.
2011/ 1/17	210	8.74	The following item was added to “MOVS, MOVSI (Move String Byte with Increment)”. ● Malfunction of instruction execution 1 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

Date	Page	Item	Description
2011/ 1/17	210	8.74	The following item was added to “MOVS, MOVSI (Move String Byte with Increment)”. ● Malfunction of instruction execution 2 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Execution condition limitation of MOVS/I, MOVSW/I Instructions (CI-00006-xE)" for details. **Condition of malfunction :** Source and destination areas are overlapping. • AH – AL < RW0 • AH < AL (only for the case of wrap-around where AL=FFFF$_H$ and AH=0000$_H$) AH or a bank register (ADB,DTB,PCB,SSB,USB) has been changed immediately before the instruction in the method of all the following. • A bank register is changed by two or less instructions just before the instruction execution, and then the bank register is used by the instruction. • After AH or a bank register is changed, or simultaneously, RW0 has not been changed.. • After AH or a bank register is changed, RW0 has not been changed. **Malfunction :** A wrong data transfer is done.
2011/ 1/17	211	8.75	The following item was added to “MOVSD (Move String Byte with Decrement)”. ● Malfunction of instruction execution In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

Date	Page	Item	Description
2011/ 1/17	213	8.76	The following item was added to “MOVSW, MOVSWI (Move String Word with Increment)”. ● Malfunction of instruction execution 1 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.
2011/ 1/17	213	8.76	The following item was added to “MOVSW, MOVSWI (Move String Word with Increment)”. ● Malfunction of instruction execution 2 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Execution condition limitation of MOVS/I, MOVSW/I Instructions (CI-00006-xE)" for details. **Condition of malfunction :** Source and destination areas are overlapping. • AH – AL < 2 × RW0 • AH < AL (only for the case of wrap-around where AL=FFFF$_H$ and AH=0000$_H$) AH or a bank register (ADB,DTB,PCB,SSB,USB) has been changed immediately before the instruction in the method of all the following. • A bank register is changed by two or less instructions just before the instruction execution, and the bank register is used by the instruction. • After AH or a bank register is changed, or simultaneously, RW0 has not been changed.. • After AH or a bank register is changed, RW0 has not been changed. **Malfunction :** A wrong data transfer is done.

Date	Page	Item	Description
2011/ 1/17	214	8.77	The following item was added to “MOVSWD (Move String Word with Decrement)”. ● Malfunction of instruction execution In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data transfer correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.
2011/ 1/17	274	8.116	The following item was added to “SCEQ, SCEQI (Scan String Byte until equal with Increment)”. ● Malfunction of instruction execution 1 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data scan correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

Date	Page	Item	Description
2011/ 1/17	274	8.116	The following item was added to “SCEQ, SCEQI (Scan String Byte until equal with Increment)”. ● Malfunction of instruction execution 2 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Report on wrong execution of scan string instruction SCEQ/SCWEQ at Interrupt (CI07-00003-xE)" for details. **Condition of malfunction :** • An interrupt request was generated during executing the instruction. • The interrupt service was started at the same time when the specified byte data in AL is found in the field of data. **Malfunction :** Data in AH, RW0 and the N, Z, V, C flags are wrong at the end of the execution of the instruction.
2011/ 1/17	276	8.117	The following item was added to “SCEQD (Scan String Byte until equal with Decrement)”. ● Malfunction of instruction execution In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data scan correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

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2011/ 1/17	276	8.117	The following item was added to “SCEQD (Scan String Byte until equal with Decrement)”. ● Malfunction of instruction execution 2 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Report on wrong execution of scan string instruction SCEQ/SCWEQ at Interrupt (CI07-00003-xE)" for details. **Condition of malfunction :** • An interrupt request was generated during executing the instruction. • The interrupt service was started at the same time when the specified byte data in AL is found in the field of data. **Malfunction :** Data in AH, RW0 and the N, Z, V, C flags are wrong at the end of the execution of the instruction.
2011/ 1/17	278	8.118	The following item was added to “SCWEQ, SCWEQI (Scan String Word until equal with Increment)”. ● Malfunction of instruction execution 1 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data scan correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

Date	Page	Item	Description
2011/ 1/17	278	8.118	The following item was added to “SCWEQ, SCWEQI (Scan String Word until equal with Increment)”. ● Malfunction of instruction execution 2 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Report on wrong execution of scan string instruction SCEQ/SCWEQ at Interrupt (CI07-00003-xE)" for details. **Condition of malfunction :** • An interrupt request was generated during executing the instruction. • The interrupt service was started at the same time when the specified word data in AL is found in the field of data. **Malfunction :** Data in AH, RW0 and the N, Z, V, C flags are wrong at the end of the execution of the instruction.
2011/ 1/17	280	8.119	The following item was added to “SCWEQD (Scan String Word until equal with Decrement)”. ● Malfunction of instruction execution 1 In F^{2}MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details. **Condition of malfunction :** The following two cases were happened at the same time. • Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles). • An interrupt was generated while executing the instruction. **Malfunction :** The execution of the instruction is terminated without performing data scan correctly, and then the next instruction is executed. **Possible interrupt disable operations :** • Clear the interrupt source flags of peripheral functions. • Set the interrupt enable/disable bits of peripheral functions. • Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value] • Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured. **Other interrupt disable operations (not included) :** • Clear the interrupt enable flag (CCR:I) • Clear the privileged mode flag (CCR:P). • Change the interruption level mask (ILM) value.

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>2011/
1/17</td><td>280</td><td>8.119</td><td>The following item was added to “SCWEQD (Scan String Word until equal with Decrement)”.

● Malfunction of instruction execution 2

In F²MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Report on wrong execution of scan string instruction SCEQ/SCWEQ at Interrupt (CI07-00003-xE)" for details.

Condition of malfunction :
• An interrupt request was generated during executing the instruction.
• The interrupt service was started at the same time when the specified word data in AL is found in the field of data.

Malfunction :
Data in AH, RW0 and the N, Z, V, C flags are wrong at the end of the execution of the instruction.</td></tr>
<tr><td>2011/
1/17</td><td>299</td><td>8.132</td><td>The following item was added to “WBTc (Wait until Bit Condition satisfied)”.

● Malfunction of instruction execution

In F²MC-16FX family, this instruction has a malfunction as the following. Refer to customer information "Failure of String Instructions and WBTC/WBTS Instructions (CI-00002-xE)" for details.

Condition of malfunction :
The following two cases were happened at the same time.
• Interrupt disabling is performed just before the instruction execution (with in 4 CPU clock cycles).
• An interrupt was generated while executing the instruction.

Malfunction :
Bit wait status is cancelled, and then the next instruction is executed.

Possible interrupt disable operations :
• Clear the interrupt source flags of peripheral functions.
• Set the interrupt enable/disable bits of peripheral functions.
• Set the interrupt level setting value of a peripheral function (ILR/ICR) to the ILM value or higher. [ILR/ICR values ≧ ILM value]
• Allow the DMA transfer from a peripheral function for which an interrupt setting has been configured.

Other interrupt disable operations (not included) :
• Clear the interrupt enable flag (CCR:I)
• Clear the privileged mode flag (CCR:P).
• Change the interruption level mask (ILM) value.</td></tr>
<tr><td>2011/
1/17</td><td>331</td><td>APPEN
DIX B</td><td>Line of RETI instruction of “Table B-12” was corrected as corrected by the shading below.

(Error)

<table>
<tr><th>Mnemonic</th><th>#</th><th>~</th><th></th><th>Operation</th><th>LH</th><th>AH</th></tr>
<tr><td>RETI</td><td>1</td><td>22/6 *1</td><td>1</td><td>Return from interrupt</td><td>-</td><td>-</td></tr>
</table>

(Correct)

<table>
<tr><th>Mnemonic</th><th>#</th><th>~</th><th>B</th><th>Operation</th><th>LH</th><th>AH</th></tr>
<tr><td>RETI</td><td>1</td><td>22/6 *1</td><td>1</td><td>Return from interrupt</td><td>*</td><td>*</td></tr>
</table>
</td></tr>
</table>