MB3773

Power Supply Monitor with Watch-Dog Timer

Description

MB3773 generates the reset signal to protect an arbitrary system when the power-supply voltage momentarily is intercepted or decreased. It is IC for the power-supply voltage watch and “Power on reset” is generated at the normal return of the power supply. MB3773 sends the microprocessor the reset signal when decreasing more than the voltage, which the power supply of the system specified, and the computer data is protected from an accidental deletion.

In addition, the watch-dog timer for the operation diagnosis of the system is built into, and various microprocessor systems can provide the fail-safe function. If MB3773 does not receive the clock pulse from the processor for a specified period, MB3773 generates the reset signal.

Features

- Precision voltage detection ($V_S = 4.2 \text{ V} \pm 2.5\%$)
- Detection threshold voltage has hysteresis function
- Low voltage output for reset signal ($V_{CC} = 0.8 \text{ V Typ}$)
- Precision reference voltage output ($V_R = 1.245 \text{ V} \pm 1.5\%$)
- With built-in watch-dog timer of edge trigger input.
- External parts are few.(1 piece in capacity)
- The reset signal outputs the positive and negative both theories reason.
- One type of package (SOP-8pin : 1 type)

Application

- Industrial Equipment
- Arcade Amusement etc.
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</table>
1. Pin Assignment

![Pin Assignment Diagram](image)

2. Block Diagram

![Block Diagram](image)
3. Functional Descriptions

Comp.S is comparator including hysteresis. it compare the reference voltage and the voltage of Vs, so that when the voltage of Vs terminal falls below approximately 1.23 V, reset signal outputs. Instantaneous breaks or drops in the power can be detected as abnormal conditions by the MB3773 within a 2 μs interval. However because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the Vs terminal.

Comp.O is comparator for turning on/off the RESET/RESET outputs and, compare the voltage of the CT terminal and the threshold voltage. Because the RESET/RESET outputs have built-in pull-up circuit, there is no need to connect to external pull-up resistor when connected to a high impedance load such as CMOS logic IC. (It corresponds to 500 kΩ at Vcc = 5 V.) when the voltage of the CK terminal changes from the “high” level into the “Low” level, pulse generator is sent to the watch-dog timer by generating the pulse momentarily at the time of drop from the threshold level. When power-supply voltages fall more than detecting voltages, the watch-dog timer becomes an interdiction.

The Reference amplifier is an op-amp to output the reference voltage. If the comparator is put up outside, two or more power-supply voltage monitor and overvoltage monitor can be done. If it uses a comparator of the open-collector output, and the output of the comparator is connected with the Vs terminal of MB3773 without the pull-up resistor, it is possible to voltage monitor with reset-hold time.
### MB3773 Basic Operation

![Logic Circuit Diagram]

- **VCC**
- **RESET**
- **CK**
- **CT**
- **GND**

#### Logic Circuit

- **TPR (ms)** \(\approx 1000 \cdot CT (\mu F)\)
- **TWD (ms)** \(\approx 100 \cdot CT (\mu F)\)
- **TWR (ms)** \(\approx 20 \cdot CT (\mu F)\)

#### Example:

- \(CT = 0.1 \mu F\)
- \(T_{RR} (ms) \approx 100\) (ms)
- \(T_{WD} (ms) \approx 10\) (ms)
- \(T_{WR} (ms) \approx 2\) (ms)

#### Timing Diagrams:

- **VCC**
- **VSH**
- **VEL**
- **0.8 V**

- **CK**
- **TCK**

- **CT**

- **RESET**
- \(T_{PR}\)
- \(T_{WR}\)
- \(T_{WD}\)

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4. Operation Sequence

1. When Vcc rises to about 0.8 V, \( \text{RESET} \) goes “Low” and \( \text{RESET} \) goes “High”.
   The pull-up current of approximately 1 \( \mu \text{A} \) (Vcc = 0.8 V) is output from \( \text{RESET} \).

2. When Vcc rises to \( V_{\text{SH}} \) (≈ 4.3V), the charge with \( C_T \) starts.
   At this time, the output is being reset.

3. When \( C_T \) begins charging, \( \text{RESET} \) goes “High” and \( \text{RESET} \) goes “Low”.
   After \( T_{PR} \) reset of the output is released.
   Reset hold time: \( T_{PR} \) (ms) = 1000 \( \times \) \( C_T \) (\( \mu \text{F} \))
   After releasing reset, the discharge of \( C_T \) starts, and watch-dog timer operation starts.
   \( T_{PR} \) is not influenced by the CK input.

4. \( C \) changes from the discharge into the charge if the clock (Negative edge) is input to the CK terminal while discharging \( C_T \).

5. \( C \) changes from the charge into the discharge when the voltage of \( C_T \) reaches a constant
   threshold (≈ 1.4 V).
   4 and 5 are repeated while a normal clock is input by the logic system.

6. When the clock is cut off, gets, and the voltage of \( C_T \) falls on threshold (≈ 0.4 V) of reset on, \( \text{RESET} \) goes “Low” and \( \text{RESET} \) goes “High”.
   Discharge time of \( C_T \) until reset is output: \( T_{WD} \) is watch-dog timer monitoring time.
   \( T_{WD} \) (ms) = \( 100 \times C_T \) (\( \mu \text{F} \))
   Because the charging time of \( C_T \) is added at accurate time from stop of the clock and getting to the output of reset of the clock,
   \( T_{WD} \) becomes maximum \( T_{WD} \) + \( T_{WR} \) by minimum \( T_{WD} \).

7. Reset time in operating watch-dog timer: \( T_{WR} \) is charging time where the voltage of \( C_T \) goes up to off
   threshold (≈ 1.4 V) for reset.
   \( T_{WR} \) (ms) = \( 20 \times C_T \) (\( \mu \text{F} \))
   Reset of the output is released after \( C_T \) reaches an off threshold for reset, and \( C_T \) starts the discharge, after that if the clock is
   normally input, operation repeats 4 and 5, when the clock is cut off, operation repeats 6 and 7.

8. When Vcc falls on \( V_{\text{SL}} \) (≈ 4.2 V), reset is output. \( C_T \) is rapidly discharged of at the same time.

9. When Vcc goes up to \( V_{\text{SH}} \), the charge with \( C_T \) is started.
   When Vcc is momentarily low, 
   After falling \( V_{\text{SL}} \) or less Vcc, the time to going up is the standard value of the Vcc input pulse width in \( V_{\text{SH}} \) or more.
   After the charge of \( C_T \) is discharged, the charge is started if it is \( T_p \) or more.

10. Reset of the output is released after \( T_{PR} \), after Vcc becomes \( V_{\text{SH}} \) or more, and the watch-dog timer starts. After that, when Vcc
    becomes \( V_{\text{SL}} \) or less, 8 to 10 is repeated.

11. While power supply is off, when Vcc becomes \( V_{\text{SL}} \) or less, reset is output.

12. The reset output is maintained until Vcc becomes 0.8 V when Vcc falls on 0 V.
5. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>V_CC</td>
<td>- 0.3</td>
<td>+ 18 V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>V_S</td>
<td>- 0.3</td>
<td>V_CCC (≤ +18)</td>
</tr>
<tr>
<td></td>
<td>V_CK</td>
<td>- 0.3</td>
<td>+ 18 V</td>
</tr>
<tr>
<td>RESET, RESET Supply voltage</td>
<td>V_OH</td>
<td>- 0.3</td>
<td>V_CCC (≤ +18)</td>
</tr>
<tr>
<td>Power dissipation (Ta ≤ +85°C)</td>
<td>P_D</td>
<td>—</td>
<td>200 mW</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T_STG</td>
<td>- 55</td>
<td>+ 125 °C</td>
</tr>
</tbody>
</table>

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

6. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>V_CC</td>
<td>+ 3.5</td>
<td>+ 16 V</td>
</tr>
<tr>
<td>RESET, RESET sink current</td>
<td>I_OL</td>
<td>0</td>
<td>20 mA</td>
</tr>
<tr>
<td>VREF output current</td>
<td>I_OUT</td>
<td>- 200</td>
<td>+ 5 μA</td>
</tr>
<tr>
<td>Watch clock setting time</td>
<td>t_WD</td>
<td>0.1</td>
<td>1000 ms</td>
</tr>
<tr>
<td>CK Rising/falling time</td>
<td>t_FC, t_RC</td>
<td>—</td>
<td>100 μs</td>
</tr>
<tr>
<td>Terminal capacitance</td>
<td>C_T</td>
<td>0.001</td>
<td>10 μF</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>Ta</td>
<td>- 40</td>
<td>+ 85 °C</td>
</tr>
</tbody>
</table>

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.
7. Electrical Characteristics

7.1 DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
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<tr>
<td>Supply current</td>
<td>$I_{CC}$</td>
<td>Watch-dog timer operating</td>
<td>600</td>
<td>900</td>
</tr>
<tr>
<td>Detection voltage</td>
<td>$V_{SL}$</td>
<td>$V_{CC}$, $Ta = -40°C to +85°C$</td>
<td>4.10</td>
<td>4.20</td>
</tr>
<tr>
<td></td>
<td>$V_{SH}$</td>
<td>$V_{CC}$, $Ta = -40°C to +85°C$</td>
<td>4.20</td>
<td>4.30</td>
</tr>
<tr>
<td>Hysteresis width</td>
<td>$V_{HYS}$</td>
<td>$V_{CC}$</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>$V_{REF}$</td>
<td>—</td>
<td>1.227</td>
<td>1.245</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Ta = -40°C to +85°C$</td>
<td>1.215</td>
<td>1.245</td>
</tr>
<tr>
<td>Reference voltage change rate</td>
<td>$\Delta V_{REF1}$</td>
<td>$V_{CC} = 3.5 V to 16 V$</td>
<td>—</td>
<td>3</td>
</tr>
<tr>
<td>Reference voltage output loading change rate</td>
<td>$\Delta V_{REF2}$</td>
<td>$I_{OUT} = -200 \mu A to +5 \mu A$</td>
<td>-5</td>
<td>—</td>
</tr>
<tr>
<td>CK threshold voltage</td>
<td>$V_{TH}$</td>
<td>$V_{CC} = 5.0 V$</td>
<td>0.8</td>
<td>1.25</td>
</tr>
<tr>
<td>CK input current</td>
<td>$I_H$</td>
<td>$V_{CM} = 5.0 V$</td>
<td>—</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$I_L$</td>
<td>$V_{CM} = 0.0 V$</td>
<td>-1.0</td>
<td>-0.1</td>
</tr>
<tr>
<td>C_T discharge current</td>
<td>$I_{CTD}$</td>
<td>Watch-dog timer operating $V_{CT} = 1.0 V$</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>High level output voltage</td>
<td>$V_{OH1}$</td>
<td>$V_S$ open, $I_{RESET} = -5 \mu A$</td>
<td>4.5</td>
<td>4.9</td>
</tr>
<tr>
<td></td>
<td>$V_{OH2}$</td>
<td>$V_S = 0 V$, $I_{RESET} = -5 \mu A$</td>
<td>4.5</td>
<td>4.9</td>
</tr>
<tr>
<td>Output saturation voltage</td>
<td>$V_{OL1}$</td>
<td>$V_S = 0 V$, $I_{RESET} = 3 mA$</td>
<td>—</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>$V_{OL2}$</td>
<td>$V_S = 0 V$, $I_{RESET} = 10 mA$</td>
<td>—</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>$V_{OL3}$</td>
<td>$V_S$ open, $I_{RESET} = 3 mA$</td>
<td>—</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>$V_{OL4}$</td>
<td>$V_S$ open, $I_{RESET} = 10 mA$</td>
<td>—</td>
<td>0.3</td>
</tr>
<tr>
<td>Output sink current</td>
<td>$I_{OL1}$</td>
<td>$V_S = 0 V$, $V_{RESET} = 1.0 V$</td>
<td>20</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>$I_{OL2}$</td>
<td>$V_S$ open, $V_{RESET} = 1.0 V$</td>
<td>20</td>
<td>60</td>
</tr>
<tr>
<td>C_T charge current</td>
<td>$I_{CTU}$</td>
<td>Power on reset operating $V_{CT} = 1.0 V$</td>
<td>0.5</td>
<td>1.2</td>
</tr>
<tr>
<td>Min supply voltage for RESET</td>
<td>$V_{CCL1}$</td>
<td>$V_{RESET} = 0.4 V$, $I_{RESET} = 0.2 mA$</td>
<td>—</td>
<td>0.8</td>
</tr>
<tr>
<td>Min supply voltage for RESET</td>
<td>$V_{CCL2}$</td>
<td>$V_{RESET} = V_{CC} - 0.1 V$, $R_L$ (between pin 2 and GND) = 1 MΩ</td>
<td>—</td>
<td>0.8</td>
</tr>
</tbody>
</table>
### 7.2 AC Characteristics

(V<sub>CC</sub> = 5 V, Ta = +25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC &lt;/sub&gt; input pulse width</td>
<td>T&lt;sub&gt;PI&lt;/sub&gt;</td>
<td>5 V, V&lt;sub&gt;CC&lt;/sub&gt; 4 V</td>
<td>8.0</td>
<td>μs</td>
</tr>
<tr>
<td>CK input pulse width</td>
<td>T&lt;sub&gt;CKW&lt;/sub&gt;</td>
<td>CK or</td>
<td>3.0</td>
<td>μs</td>
</tr>
<tr>
<td>CK input frequency</td>
<td>T&lt;sub&gt;CK&lt;/sub&gt;</td>
<td>—</td>
<td>20</td>
<td>μs</td>
</tr>
<tr>
<td>Watch-dog timer watching time</td>
<td>T&lt;sub&gt;WD&lt;/sub&gt;</td>
<td>C&lt;sub&gt;T&lt;/sub&gt; = 0.1 μF</td>
<td>5 10 15</td>
<td>ms</td>
</tr>
<tr>
<td>Watch-dog timer reset time</td>
<td>T&lt;sub&gt;WR&lt;/sub&gt;</td>
<td>C&lt;sub&gt;T&lt;/sub&gt; = 0.1 μF</td>
<td>1 2 3</td>
<td>ms</td>
</tr>
<tr>
<td>Rising reset hold time</td>
<td>T&lt;sub&gt;PR&lt;/sub&gt;</td>
<td>C&lt;sub&gt;T&lt;/sub&gt; = 0.1 μF, V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>50 100 150</td>
<td>ms</td>
</tr>
<tr>
<td>Output propagation delay time from VCC</td>
<td>T&lt;sub&gt;PD1&lt;/sub&gt;</td>
<td>RESET, R&lt;sub&gt;L&lt;/sub&gt; = 2.2 kΩ, C&lt;sub&gt;L&lt;/sub&gt; = 100 pF</td>
<td>— 2 10</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>T&lt;sub&gt;PD2&lt;/sub&gt;</td>
<td>RESET, R&lt;sub&gt;L&lt;/sub&gt; = 2.2 kΩ, C&lt;sub&gt;L&lt;/sub&gt; = 100 pF</td>
<td>— 3 10</td>
<td>μs</td>
</tr>
<tr>
<td>Output rising time*</td>
<td>t&lt;sub&gt;R&lt;/sub&gt;</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 2.2 kΩ, C&lt;sub&gt;L&lt;/sub&gt; = 100 pF</td>
<td>— 1.0 1.5</td>
<td>μs</td>
</tr>
<tr>
<td>Output falling time*</td>
<td>t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 2.2 kΩ, C&lt;sub&gt;L&lt;/sub&gt; = 100 pF</td>
<td>— 0.1 0.5</td>
<td>μs</td>
</tr>
</tbody>
</table>

*: Output rising/falling time are measured at 10 % to 90 % of voltage.
8. Typical Characteristic Curves

- Supply current vs. Supply voltage
- Output voltage vs. Supply voltage
- Detection voltage (VSH, VSL) vs. Operating ambient temperature
- Output saturation voltage vs. Output sink current
(Continued)

Reset time vs. Operating ambient temperature
(At watch-dog timer)

Watch-dog timer watching time vs. Operating ambient temperature

Watch-dog timer watching time vs. \( C_T \) terminal capacitance

Reset time vs. \( C_T \) terminal capacitance
(at watch-dog timer)

Rising reset hold time vs. \( C_T \) terminal capacitance

\[ \begin{align*}
V_{CC} &= 5 \text{ V} \\
C_T &= 0.1 \mu\text{F}
\end{align*} \]
9. Application Circuit

EXAMPLE 1: Monitoring 5V Supply Voltage and Watch-dog Timer

![Circuit Diagram]

Notes:
- Supply voltage is monitored using $V_S$.
- Detection voltage are $V_{SH}$ and $V_{SL}$.

EXAMPLE 2: 5V Supply Voltage Monitoring (external fine-tuning type)

![Circuit Diagram]

Notes:
- $V_S$ detection voltage can be adjusted externally.
- Based on selecting $R_1$ and $R_2$ values that are sufficiently lower than the resistance of the IC’s internal voltage divider, the detection voltage can be set according to the resistance ratio of $R_1$ and $R_2$ (Refer to the table below.)

<table>
<thead>
<tr>
<th>$R_1$ (kΩ)</th>
<th>$R_2$ (kΩ)</th>
<th>Detection voltage: $V_{SL}$ (V)</th>
<th>Detection voltage: $V_{SH}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>3.9</td>
<td>4.4</td>
<td>4.5</td>
</tr>
<tr>
<td>9.1</td>
<td>3.9</td>
<td>4.1</td>
<td>4.2</td>
</tr>
</tbody>
</table>
EXAMPLE 3: With Forced Reset (with reset hold)

(a)

![Circuit Diagram](image)

Note: Grounding pin 7 at the time of SW ON sets RESET (pin 8) to Low and RESET (pin 2) to High.

(b)

![Circuit Diagram](image)

Note: Feeding the signal to terminal RESIN and turning on Tr sets the RESET terminal to Low and the
RESET terminal to High.
EXAMPLE 4: Monitoring Two Supply Voltages (with hysteresis, reset output and NMI)

VCC1 (512348765 MB3773
VCC2 (12

Example: Comp. 1, Comp. 2
: MB4204, MB47393

Notes:
• The 5 V supply voltage is monitored by the MB3773.
• The 12 V supply voltage is monitored by the external circuit. Its output is connected to the NMI terminal and, when voltage drops, Comp. 2 interrupts the logic circuit.
• Use VCC1 (= 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
• The detection voltage of the VCC2 (= 12 V) supply voltage is approximately 9.2 V/9.4 V and has a hysteresis width of approximately 0.2 V.

VCC2 detection voltage and hysteresis width can be found using the following formulas:

→ Detection voltage
\[ V_{2H} = \frac{R_3 + \left( \frac{R_4}{R_5} \right)}{\frac{R_4}{R_5}} \times V_{\text{REF}} \]
(Aproximately 9.4 V in the above illustration)

\[ V_{2L} = \frac{R_3}{R_5} \times V_{\text{REF}} \]
(Aproximately 9.2 V in the above illustration)

→ Hysteresis width
\[ V_{\text{HYS}} = V_{2H} - V_{2L} \]
EXAMPLE 5: Monitoring Two Supply Voltages (with hysteresis and reset output)

V_{CC2} (12)
V_{CC1} (5 V)

MB3773
1 8
2 7
3 6
4 5

20 kΩ
20 kΩ

30 kΩ
30 kΩ

R₁
R₂

1.2 kΩ
5.1 kΩ

R₃
R₄

180 kΩ
180 kΩ

R₅

Comp. 1
Comp. 2

Diode

Diode

RESET
RESET

CK
GND

CT

Example : Comp. 1, Comp. 2
: MB4204, MB47393

Notes:
- When either 5 V or 12 V supply voltage decreases below its detection voltage (V_{SL}), the MB3773 RESET terminal is set to High and the MB3773 RESET terminal is set to Low.
- Use V_{CC1} ( = 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
- The detection voltage of the V_{CC2} ( = 12 V) supply voltage is approximately 9.2 V/9.4 V and has a hysteresis width of approximately 0.2 V. For the formulas for finding hysteresis width and detection voltage, refer to section 4.
EXAMPLE 6: Monitoring Low voltage and Overvoltage Monitoring (with hysteresis)

Notes:
- Comp. 1 and Comp. 2 are used to monitor for overvoltage while the MB3773 is used to monitor for low voltage. Detection voltages $V_{1L}/V_{1H}$ at the time of low voltage are approximately 4.2 V/4.3 V. Detection voltages $V_{2L}/V_{2H}$ at the time of overvoltage are approximately 6.0 V/6.1 V. For the formulas for finding hysteresis width and detection voltage, see EXAMPLE 4.
- Use $V_{CC}$ (= 5 V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.

Example: Comp. 1, Comp. 2 : MB4204, MB47393
EXAMPLE 7: Monitoring Supply Voltage Using Delayed Trigger

Note: Adding voltage such as shown in the figure to VCC increases the minimum input pulse width by 50 μs (C1 = 1000 pF).
EXAMPLE 8: Stopping Watch-dog Timer (Monitoring only supply voltage)

These are example application circuits in which the MB3773 monitors supply voltage alone without resetting the microprocessor even if the latter, used in standby mode, stops sending the clock pulse to the MB3773.

- The watch-dog timer is inhibited by clamping the $C_T$ terminal voltage to $V_{REF}$.

The supply voltage is constantly monitored even while the watch-dog timer is inhibited. For this reason, a reset signal is output at the occurrence of either instantaneous disruption or a sudden drop to low voltage. Note that in application examples (a) and (b), the hold signal is inactive when the watch-dog timer is inhibited at the time of resetting.

If the hold signal is active when the microprocessor is reset, the solution is to add a gate, as in examples (c) and (d).

(a) Using NPN transistor

(b) Using PNP transistor
(c) Using NPN transistor

(d) Using PNP transistor
EXAMPLE 9: Reducing Reset Hold Time

Notes:
- **RESET** is the only output that can be used.
- Standard **TPR**, **TWD**, and **TWR** value can be found using the following formulas.
  - Formulas:
    - \( T_{PR} \approx 100 \times CT \) (μF)
    - \( T_{WD} \approx 100 \times CT \) (μF)
    - \( T_{WR} \approx 16 \times CT \) (μF)
- The above formulas become standard values in determining **TPR**, **TWD**, and **TWR**.

<table>
<thead>
<tr>
<th></th>
<th><strong>TPR reduction circuit</strong></th>
<th><strong>Standard circuit</strong></th>
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<tr>
<td><strong>TPR</strong></td>
<td>10 ms</td>
<td>100 ms</td>
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<tr>
<td><strong>TWD</strong></td>
<td>10 ms</td>
<td>10 ms</td>
</tr>
<tr>
<td><strong>TWR</strong></td>
<td>1.6 ms</td>
<td>2.0 ms</td>
</tr>
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</table>

\( CT = 0.1 \mu F \)
EXAMPLE 10: Circuit for Monitoring Multiple Microprocessor

Notes:
- connects from FF1 and FF2 outputs $\overline{Q}_1$ and $\overline{Q}_2$ to the NOR input.
- Depending on timing, these connections may not be necessary.
- Example: $R_1 = R_2 = 2.2 \, \text{k}\Omega$
  \[ C_T = 0.1 \, \mu\text{F} \]

* : Microprocessor

Figure 1

Figure 2
Description of Application Circuits

Using one MB3773, this application circuit monitors multiple microprocessor in one system. Signals from each microprocessor are sent to FF1, FF2 and FF3 clock inputs. Figure 2 shows these timings. Each flip-flop operates using signals sent from microprocessor as its clock pulse. When even one signal stops, the relevant receiving flip-flop stops operating. As a result, cyclical pulses are not generated at output Q3. Since the clock pulse stops arriving at the CK terminal of the MB3773, the MB3773 generates a reset signal. Note that output Q3 frequency f will be in the following range, where the clock frequencies of CK1, CK2 and CK3 are f1, f2 and f3 respectively.

\[
\frac{1}{f_0} \leq \frac{1}{f} \leq \frac{1}{f_1} + \frac{1}{f_2} + \frac{1}{f_3}
\]

where \(f_0\) is the lowest frequency among \(f_1\), \(f_2\) and \(f_3\).
EXAMPLE 11: Circuit for Limiting Upper Clock Input Frequency

Notes:

- This is an example application to limit upper frequency \(f_H\) of clock pulses sent from the microprocessor. If the CK cycle sent from the microprocessor exceeds \(f_H\), the circuit generates a reset signal. (The lower frequency has already been set using \(C_T\).)
- When a clock pulse such as shown below is sent to terminal CK, a short \(T_2\) prevents \(C_2\) voltage from reaching the CK input threshold level \((= 1.25 \text{ V})\), and will cause a reset signal to be output. The \(T_1\) value can be found using the following formula:

\[
T_1 \approx 0.3 \ C_2 \ R_2
\]

where \(V_{CC} = 5 \text{ V}, \ T_3 \geq 3.0 \ \mu\text{s}, \ T_2 \geq 20 \ \mu\text{s}\)

Example: Setting \(C\) and \(R\) allow the upper \(T_1\) value to be set (Refer to the table below).

<table>
<thead>
<tr>
<th>(C)</th>
<th>(R)</th>
<th>(T_1)</th>
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<tbody>
<tr>
<td>0.01 (\mu\text{F})</td>
<td>10 k(\Omega)</td>
<td>30 (\mu\text{s})</td>
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<tr>
<td>0.1 (\mu\text{F})</td>
<td>10 k(\Omega)</td>
<td>300 (\mu\text{s})</td>
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10. Notes on Use

■ Take account of common impedance when designing the earth line on a printed wiring board.

■ Take measures against static electricity.
  ❐ For semiconductors, use antistatic or conductive containers.
  ❐ When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  ❐ The work table, tools and measuring instruments must be grounded.
  ❐ The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

■ Do not apply a negative voltage
  ❐ Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

11. Ordering Information

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<th>Part number</th>
<th>Package</th>
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<tr>
<td>MB3773PF-□□□E1</td>
<td>8-pin plastic SOP (SOE008)</td>
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12. RoHS Compliance Information of Lead (Pb) Free version

The LSI products of Cypress with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

The product that conforms to this standard is added “E1” at the end of the part number.
13. Package Dimension

Package Code: SOE008

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NOTES
1. ALL DIMENSIONS ARE IN MILLIMETER.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D AND E1 DIMENSION ARE DETERMINED AT DATUM H.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "B" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "B" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15857 Rev. **
Document History

Spansion Publication Number: DS04-27401-8Ea

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