

FR Family, All series, Setting initialization reset and Operation Initialization reset

The reset operations of the FR family are classified into two levels, each of which has different causes and initialization operations.

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1 Reset Level

The reset operations of the FR family are classified into two levels, each of which has different causes and initialization operations.

1.1 Settings Initialization Reset (INIT)

The highest-level reset, which initializes all settings, is called a settings initialization reset (INIT).

1.2 Operation Initialization Reset (RST)

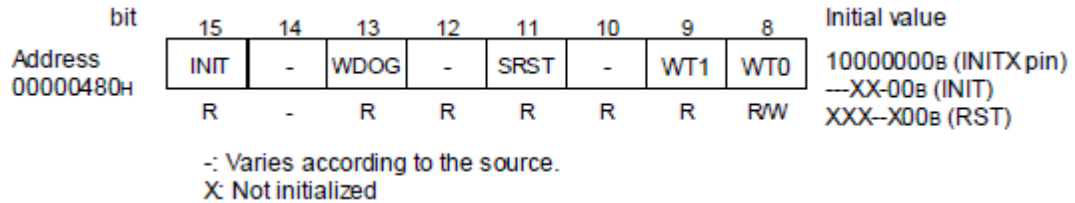
A normal-level reset that initializes the operation of a program is called an operation initialization reset (RST). If a settings initialization reset (INIT) occurs, an operation initialization reset (RST) also occurs.

But after RST, the initial value at some registers are different after INIT such as internal clock settings, PLL settings, divided gear settings, and clock stabilization time settings.

2 The difference of register value after each reset

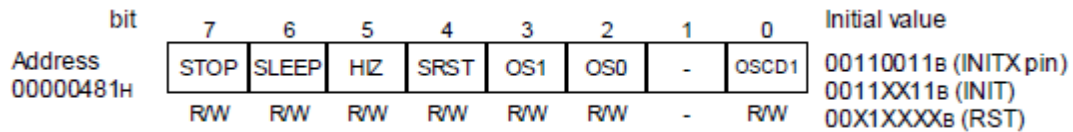
2.1 RSRR: reset source register

Figure 1. RSRR



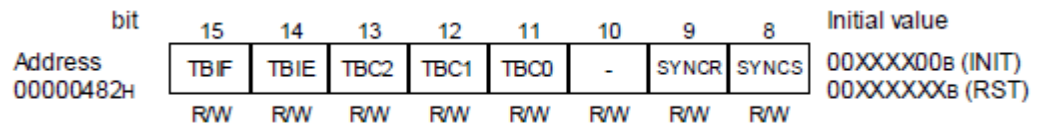
2.2 STCR: Standby control register

Figure 2. STCR



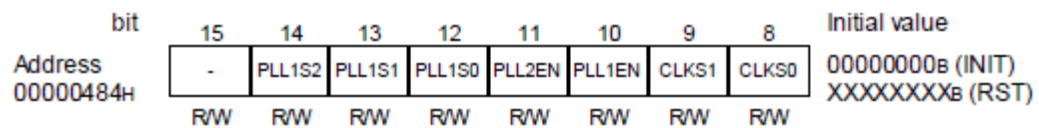
2.3 TBCR: Time base counter control register

Figure 3. TBCR



2.4 CLKR: Clock source control register

Figure 4. CLKR



2.5 DIVR0: Base clock division setting register 0

Figure 5. DIVR0

bit	15	14	13	12	11	10	9	8	Initial value
Address	B3	B2	B1	B0	P3	P2	P1	P0	0000011 _B (INIT) XXXXXXXX _B (RST)
00000486H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

2.6 DIVR1: Base clock division setting register 1

Figure 6. DIVR1

bit	7	6	5	4	3	2	1	0	Initial value
Address	T3	T2	T1	T0	-	-	-	-	00000000 _B (INIT) XXXXXXXX _B (RST)
00000487H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

2.7 OSCCR: Oscillation control register

Figure 7. OSCCR

Bit	7	6	5	4	3	2	1	0
Address : 0000048Ah	-	-	-	RTCSRC	-	-	-	OSCD _{S1}
	-	R/W	R/W	R/W	-	-	-	R/W
INIT	×	0	0	0	×	×	×	0
RST	×	×	×	×	×	×	×	0

2.8 OSCR: Main oscillator stabilization time control register

Figure 8. OSCR

bit	15	14	13	12	11	10	9	8	Initial value
Address	WIF	WIE	WEN	-	-	WS1	WS0	WCL	00000000 _B (INIT) XXXXXXXX _B (RST)
00000490H	R/W	R/W	R/W	-	-	R/W	R/W	W	

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	YUIS	03/21/2008	First Edition
*A	5294865	YUIS	06/02/2016	Migrated Spansion Application Note "AN07-00162-1E" to Cypress format.
*B	5876213	AESATMP9	09/07/2017	Updated logo and copyright.

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