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AN204410

FM3 Microcontroller Low Voltage Detect Interrupt Circuit Setting/Usage

Associated Part Family: Refer to Section 2

The low-voltage detection circuit is a circuit, which monitors the power supply voltage and outputs the reset signal and the interrupt signal when the power supply voltage drops below the detected voltage.

Contents

1 Introduction

The low-voltage detection circuit is a circuit, which monitors the power supply voltage and outputs the reset signal and the interrupt signal when the power supply voltage drops below the detected voltage.

The low-voltage detection interrupt circuit executes the following operations.

- Monitors the power supply voltage (VCC) and outputs the interrupt signal when the power supply voltage drops below the set voltage.
- Enables selection of accept or stop of the operation. It is stopped in the initial status.
- Sets the detect voltage.
- Monitors the power supply voltage even in the standby mode.
- Recovers from the standby mode when the decrease of power supply voltage is detected in the standby mode.

In this application note, the usage example and the setting method of the low-voltage detection are explained.

In addition, the sample program, which introduces the low-voltage detection interrupt setting, is indicated.

2 Target products

This application note is described about below products;

(TYPE0)

Series	Product Number (not included Package suffix)
MB9B500A	MB9BF504NA,MB9BF505NA,MB9BF506NA, MB9BF504RA,MB9BF505RA,MB9BF506RA
MB9B500B	MB9BF504NB,MB9BF505NB,MB9BF506NB, MB9BF504RB,MB9BF505RB,MB9BF506RB
MB9B400A	MB9BF404NA,MB9BF405NA,MB9BF406NA, MB9BF404RA,MB9BF405RA,MB9BF406RA
MB9B300A	MB9BF304NA,MB9BF305NA,MB9BF306NA, MB9BF304RA,MB9BF305RA,MB9BF306RA
MB9B300B	MB9BF304NB,MB9BF305NB,MB9BF306NB, MB9BF304RB,MB9BF305RB,MB9BF306RB
MB9B100A	MB9BF102NA,MB9BF104NA,MB9BF105NA,MB9BF106NA, MB9BF102RA,MB9BF104RA,MB9BF105RA,MB9BF106RA

(TYPE1)

Series	Product Number (not included Package suffix)
MB9A310	MB9AF311L,MB9AF312L,MB9AF314L, MB9AF311M,MB9AF312M,MB9AF314M,MB9AF315M,MB9AF316M, MB9AF311N,MB9AF312N,MB9AF314N,MB9AF315N,MB9AF316N
MB9A310A	MB9AF311LA,MB9AF312LA,MB9AF314LA,MB9AF311MA, MB9AF312MA,MB9AF314MA,MB9AF315MA,MB9AF316MA, MB9AF311NA,MB9AF312NA,MB9AF314NA,MB9AF315NA,MB9AF316NA
MB9A110	MB9AF111L,MB9AF112L,MB9AF114L, MB9AF111M,MB9AF112M,MB9AF114M,MB9AF115M,MB9AF116M, MB9AF111N,MB9AF112N,MB9AF114N,MB9AF115N,MB9AF116N
MB9A110A	MB9AF111LA,MB9AF112LA,MB9AF114LA,MB9AF111MA,MB9AF112MA, MB9AF114MA,MB9AF115MA,MB9AF116MA,MB9AF111NA,MB9AF112NA, MB9AF114NA,MB9AF115NA,MB9AF116NA

(TYPE2)

Series	Product Number (not included Package suffix)
MB9BD10T	MB9BFD16S,MB9BFD17S,MB9BFD18S, MB9BFD16T,MB9BFD17T,MB9BFD18T
MB9B610T	MB9BF616S,MB9BF617S,MB9BF618S, MB9BF616T,MB9BF617T,MB9BF618T
MB9B510T	MB9BF516S,MB9BF517S,MB9BF518S, MB9BF516T,MB9BF517T,MB9BF518T
MB9B410T	MB9BF416S,MB9BF417S,MB9BF418S, MB9BF416T,MB9BF417T,MB9BF418T
MB9B310T	MB9BF316S,MB9BF317S,MB9BF318S,

Series	Product Number (not included Package suffix)
	MB9BF316T,MB9BF317T,MB9BF318T
MB9B210T	MB9BF216S,MB9BF217S,MB9BF218S, MB9BF216T,MB9BF217T,MB9BF218T
MB9B110T	MB9BF116S,MB9BF117S,MB9BF118S, MB9BF116T,MB9BF117T,MB9BF118T

(TYPE3)

Series	Product Number (not included Package suffix)
MB9A130L	MB9AF131K,MB9AF132K, MB9AF131L,MB9AF132L
MB9A130LA	MB9AF131KA,MB9AF132KA, MB9AF131LA,MB9AF132LA

(TYPE4)

Series	Product Number (not included Package suffix)
MB9B510R	MB9BF512N,MB9BF514N,MB9BF515N,MB9BF516N, MB9BF512R,MB9BF514R,MB9BF515R,MB9BF516R
MB9B410R	MB9BF412N,MB9BF414N,MB9BF415N,MB9BF416N, MB9BF412R,MB9BF414R,MB9BF415R,MB9BF416R
MB9B310R	MB9BF312N,MB9BF314N,MB9BF315N,MB9BF316N, MB9BF312R,MB9BF314R,MB9BF315R,MB9BF316R
MB9B110R	MB9BF112N,MB9BF114N,MB9BF115N,MB9BF116N, MB9BF112R,MB9BF114R,MB9BF115R,MB9BF116R

(TYPE5)

Series	Product Number (not included Package suffix)
MB9A310K	MB9AF311K,MB9AF312K
MB9A110K	MB9AF111K,MB9AF112K

(TYPE6)

Series	Product Number (not included Package suffix)
MB9AB40N	MB9AFB41L,MB9AFB42L,MB9AFB44L,MB9AFB41M,MB9AFB42M, MB9AFB44M,MB9AFB41N,MB9AFB42N,MB9AFB44N
MB9AB40NA	MB9AFB41LA,MB9AFB42LA,MB9AFB44LA,MB9AFB41MA,MB9AFB42MA, MB9AFB44MA,MB9AFB41NA,MB9AFB42NA,MB9AFB44NA
MB9AA40N	MB9AFA41L,MB9AFA42L,MB9AFA44L,MB9AFA41M,MB9AFA42M, MB9AFA44M,MB9AFA41N,MB9AFA42N,MB9AFA44N
MB9AA40NA	MB9AFA41LA,MB9AFA42LA,MB9AFA44LA,MB9AFA41MA,MB9AFA42MA, MB9AFA44MA,MB9AFA41NA,MB9AFA42NA,MB9AFA44NA

Series	Product Number (not included Package suffix)
MB9A340N	MB9AF341L,MB9AF342L,MB9AF344L,MB9AF341M,MB9AF342M, MB9AF344M,MB9AF341N,MB9AF342N,MB9AF344N
MB9A340NA	MB9AF341LA,MB9AF342LA,MB9AF344LA,MB9AF341MA,MB9AF342MA, MB9AF344MA,MB9AF341NA,MB9AF342NA,MB9AF344NA
MB9A140N	MB9AF141L,MB9AF142L,MB9AF144L,MB9AF141M,MB9AF142M, MB9AF144M,MB9AF141N,MB9AF142N,MB9AF144N
MB9A140NA	MB9AF141LA,MB9AF142LA,MB9AF144LA,MB9AF141MA,MB9AF142MA, MB9AF144MA,MB9AF141NA,MB9AF142NA,MB9AF144NA

(TYPE7)

Series	Product Number (not included Package suffix)
MB9AA30N	MB9AFA31L,MB9AFA32L, MB9AFA31M,MB9AFA32M, MB9AFA31N,MB9AFA32N
MB9A130N	MB9AF131M,MB9AF132M, MB9AF131N,MB9AF132N

3 Usage Example of the Low-Voltage Detection Function

3.1 Overview

For the low-voltage detection reset circuit and the low-voltage detection interrupt circuit, the detection voltage can be set for each.

This section explains the usage example of the low-voltage detection function.

- **Low-voltage detection reset**

When the voltage supplied to FM3 VCC drops to the rated voltage or lower, the reset signal is output in order to prevent the FM3 from initiating unexpected operation.

It is used when the power supply voltage drops by the use of a battery for the power supply.

- **Low-voltage detection interrupt**

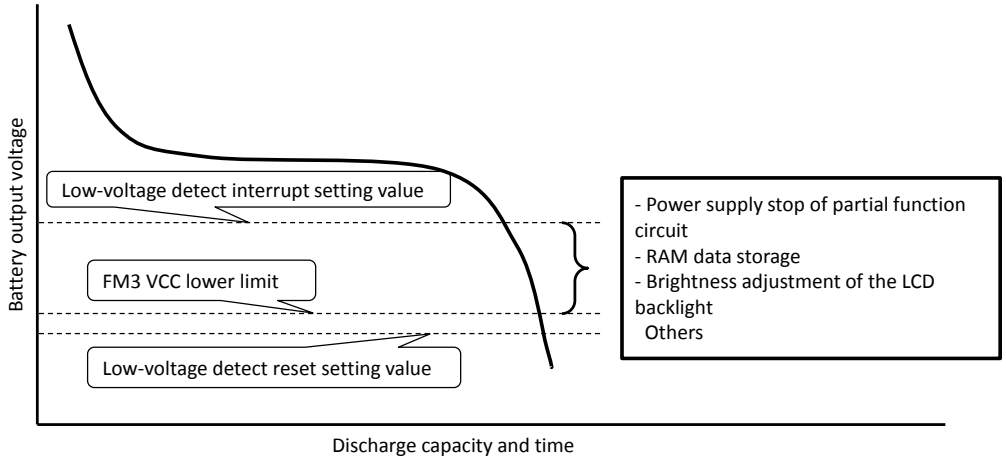
When the voltage supplied to FM3 VCC decreases to the monitoring voltage, the interrupt signal is output. When a battery is used for the power supply, it is used when an action has to be taken before the FM3 operation stops due to the power supply voltage dropping to the rated voltage or lower.

In general, batteries have the discharge characteristics as shown in Figure 1. The output voltage from a battery decreases when the battery is continuously used. The voltage drop characteristics vary between abrupt drop and gradual drop depending on the battery type.

Therefore, set the low-voltage detection interrupt voltage according to the characteristics of the battery used.

One example of using the low-voltage detection interrupt function is introduced here.

Figure 1. Usage Example of the Battery Discharge Characteristics and the Low-Voltage Detection Function



1. Power supply stop of partial function circuits or transition to the sleep status

When the low-voltage detection interrupt occurs, the power supply to partial circuits stops, and the control to transition to the sleep status activates.

To stop the power supply, mount the device such as FET, which can switch the power supply, to the power supply line for the control.

In this case, pay attention to the pin status of the FM3 I/O port, which is connected to the device that stops the power supply. In the standard devices, when the voltage, which is higher for a certain amount from the power supply pin, is applied to the I/O port, the voltage exceeds the absolute maximum rated voltage, and failure may result.

In addition, to transition to the sleep status, transition the pins and modes, which are used for transition to the power down status of each device, to the sleep status by setting the H/L level setting by GPIO and by sending commands by using SPI and I^2C functions.

2. RAM data storage

After the low-voltage detection interrupt occurs, the data on RAM integrated in FM3 are stored before the low-voltage detection reset occurs.

This operation is executed in order to prevent the FM3 integrated RAM data from being lost when the power supply from the battery is stopped and the voltage decreases to the VCC voltage or lower, which FM3 requires.

RAM data has to be stored within the period from the occurrence of the low-voltage detection interruption to the occurrence of the low-voltage detection reset. Therefore, it is recommended to use a device such as FRAM, of which the write speed is fast.

In addition, it is necessary to check the discharge characteristics of the battery used and determine the set voltages of the low voltage detection interrupt and the low voltage detection reset.

3. Brightness adjustment of the LCD backlight

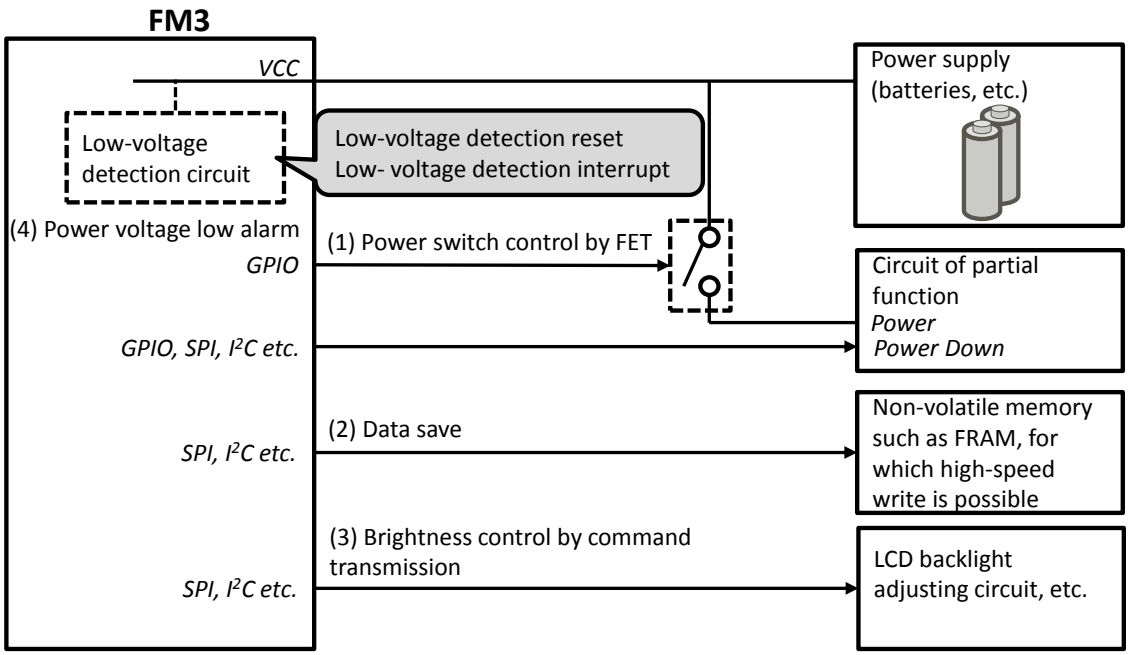
In the system that is using the LCD, the power consumption of the LCD backlight is sometimes relatively high.

Therefore, by setting the low-voltage detection interrupt and having the low-voltage detection interrupt occur, it keeps the power consumption low by detecting the remaining capacity of the battery and by darkening the backlight brightness.

4. Power supply voltage low alarm

By setting the low-voltage detection interrupt, the alarm is output. By knowing the power supply voltage low status, it can prevent the sudden system stop.

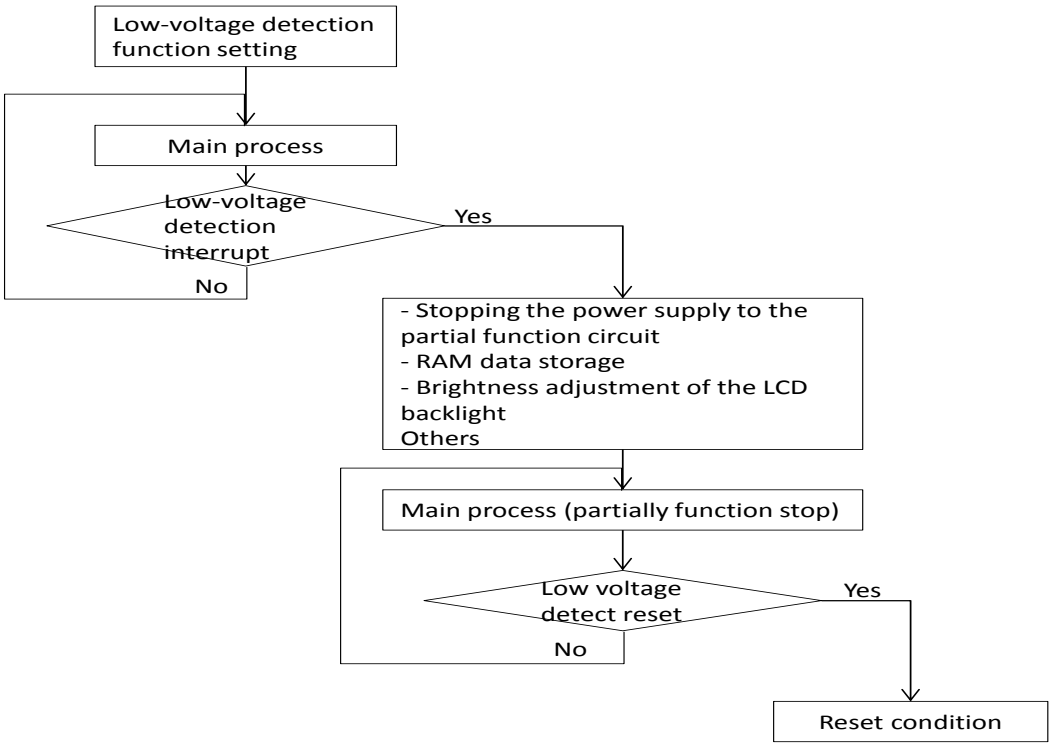
Figure 2. Usage Example of Low Voltage Detection Function



3.2 Software Process Example

The process flow example of the low voltage detection function is indicated in Figure 3

Figure 3 Process Flow Example of the Low Voltage Detection Function



4 Usage Method of Low-Voltage Detection Function

(* For the features and performance of the low-voltage detection and the block diagram, see “CHAPTER 5: LOW VOLTAGE DETECTION of MB9Axxx/MB9Bxxx Series Peripheral Manual.”)

4.1 Interrupt (NVIC)

(* For NVIC, see “CHAPTER 6: Nested Vectored Interrupt Controller of Cortex-M3 technical reference manual.”)

Table 1 indicates the source vector of the exception and interrupt (low-voltage detect) input to NVIC.

Table 1. Low Voltage Detection Interrupt Vector

Exception and Interrupt Source	Vector No.	IRQ No.	Vector Offset
Low-voltage detection (LVD)	18	2	0x48

All interruptions including the CPU core exceptions are controlled in NVIC.

In the “Cortex-M3 technical reference manual,” all exception types: IRQ are defined as external interrupt inputs.

In this manual, the exception types: IRQ are expressed as the peripheral interrupt. In the peripheral interrupt, there is the interrupt by the external pin “external interrupt and NMI control section” and the interrupt from the peripheral resource in LSI.

The NVIC interrupt can be accepted or prohibited by writing in the corresponding interrupt enable set register or the interrupt enable clear register bit field. This register has policies whereby writing 1 reads enable and writing 1 reads clear. In both registers, the current accept status of the corresponding (32) interrupt is read.

The interrupt enable set register is used for the following purposes.

- Enables the interrupt.
- Judges the currently enabled interrupt.

Each bit of the register corresponds to one of the 32 interrupts.

The corresponding interrupt is enabled by setting the bit to the interrupt enable set register. When the retained interrupt enable bit is set, the processer activates the interrupt according to the priority level of the interrupt.

When the enable bit is cleared, assert the interrupt signal. In that way, that interrupt is retained. However, activating this interrupt by ignoring the priority level is not possible.

Therefore, the prohibited interrupt can be used as the latching general-purpose I/O bit. In addition, clearing is possible by reading this bit without calling the interrupt.

To accept the usage of the low voltage detection interrupt, set the bit corresponding to IRQ No.2 of the interrupt enable set register to 1. Table 2 indicates the settings of the interrupt enable set registers.

Table 2. Interrupt Enable Set Register Setting

Address: 0xE000E100=0bXXXXXXXXXXXXXXXXXXXXXXXXXXXXX1XX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X

* X is a discretional value.

Address: 0xE000E104=0b00000000000000000XXXXXXXXXXXXXXX

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

* X is a discretional value.

(* For all interrupt contents and interrupt numbers, see “Exceptions and interrupt source vector, CHAPTER 7: INTERRUPT, in MB9Axxx/MB9Bxxx Series peripheral manual.”)

The priority level of the peripheral interrupt after vector No. 16 can be set in the interrupt priority level register. The interrupt priority level register is allocated to each interrupt by 4 bits.

The interrupt priority level register of the low-voltage detection (LVD) is IRQ No.2. Therefore, the address: 0xE000E402 becomes the interrupt priority level register of the low-voltage detection (LVD). At the time of the reset, it becomes 0x00, which is the highest priority level.

Because the vector offset is 0x48, the interrupt address is stored in 0x00000048.

4.2 APB2 Bus Clock

(* For details of APB2 bus clock, see “CHAPTER 2-1: CLOCK of MB9Axxx/MB9Bxxx Series peripheral manual.”)

The bus clock of the low-voltage detection is PCLK2 (see “Data sheet block diagram in FM3 MB9A310 series”), and the maximum internal operation clock frequency is 40 MHz. In this application note, the APB2 bus frequency is set to 20 MHz.

When a value higher than 20 MHz is set to the CPU/AHB bus clock, divide by the APB2 prescaler register (APBC2_PSR).

In addition, the wait time of the low-voltage detection circuit activation time is calculated by the APB2 clock frequency.

4.3 Low-Voltage Detection Voltage Protect Register (LVD_RLR)

The low -voltage detection voltage setting register (LVD_CTL) is protected, and the write operation during the protected status is ignored. By writing 0x1ACCE553, writing the low-voltage detection voltage setting register becomes possible (write protect release). Writing any other value disables writing in the voltage setting register of the low-voltage detection (write-protected).

In addition, by reading LVD_RLR, the protection status can be checked. When the protection is released, 0x00000000 is read. When the protection is active, 0x00000001 is read.

5 Setting Example (Sample Program)

5.1 Sample Program

This section explains the sample program that operates the low-voltage detect.

In the following section, the setting conditions of this sample program are explained.

Clock setting:

- Set the master clock to the PLL clock 40 MHz (multiply by inputting the external main clock 4 MHz to X0,X1)
- APB2 prescaler 2 division (APB0 bus clock 20 MHz)

In the above conditions, set the low-voltage detection interrupt circuit as follows.

  - When the master clock is changed to PLL, the low-voltage detection interrupt circuit is activated.
  - Execute the interrupt with a focus on 3.2V.

5.2 Activation Time of Low-voltage Detection Circuit

When the low-voltage detection circuit is activated by setting “1” to LVD_CTL: LVDIE, the wait time occurs before the activation completes. Calculate the time to the activation completion by using the following expression.

Wait time = 2002×tcycp

* tcpyp = PCLK 2cycles

2002×tcycp = 2002×50ns = 0.1001ms

5.3 Setting Step Example

The following procedure indicates the setting method of the low-voltage detection executed in the sample program.

Figure 4. Setting Step Example in the Sample Program

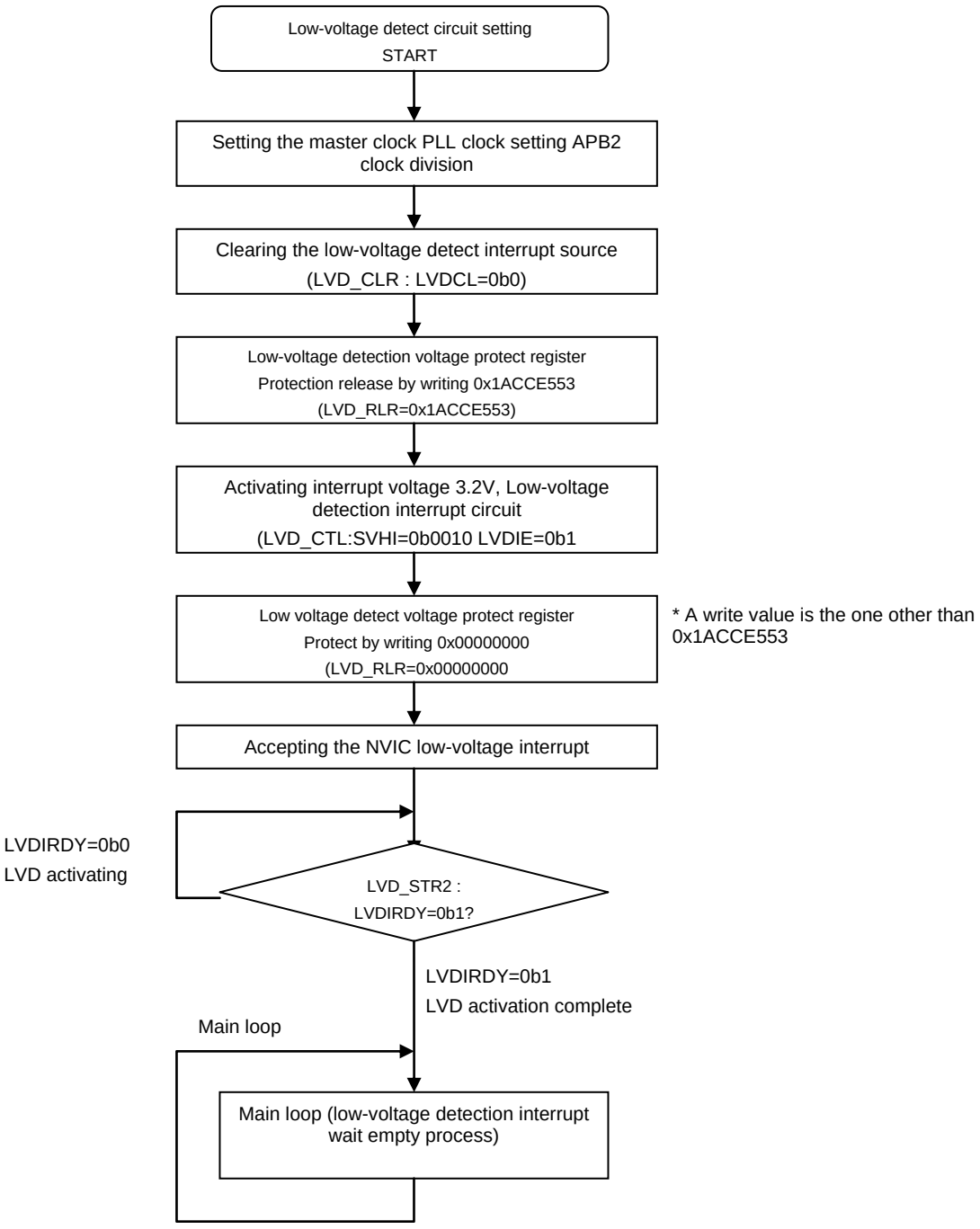
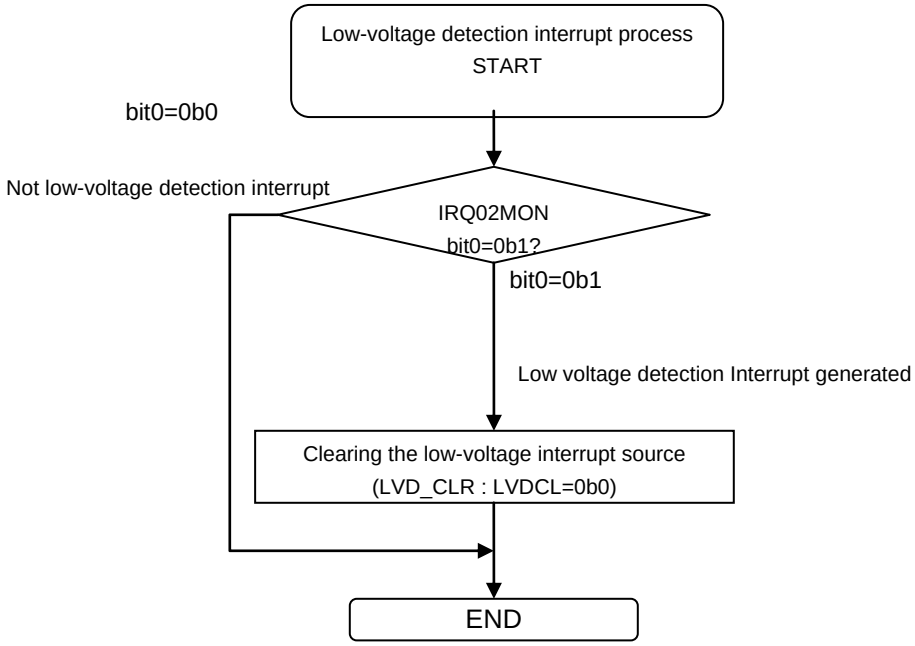


Figure 5. Low-Voltage Detection Interrupt Process Example



6 Cautions on Usage

- When PCLK is stopped by the timer mode, stop mode, and/or PBC2_PSR register during the low-voltage detection circuit stable wait period, monitoring of the power supply voltage is not executed. Transition after completion of the stable wait period.

  The sample project included in this application note is created by the IAR Embedded Workbench for ARM and KEIL MDK-ARM

7 Reference Documents

1. FM3 Family PERIPHERAL MANUAL MN706-00002-5v0-E

(Please refer to the latest document.)

Document History

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Document Number: 002-04410

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	YUIS	07/12/2012	Initial Release
			01/31/2014	Company name and layout design change
*A	5034485	YUIS	12/03/2015	Migrated Spansion Application Note from AN706-00052-1v1-E to Cypress format
*B	5872470	AESATP12	09/04/2017	Updated logo and copyright.

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