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The S6AE101A is a power management IC (PMIC) for energy harvesting that is built into circuits of solar cells connected in series, output power control circuits, output capacitor storage circuits, and power switching circuits of primary batteries. Super-low-power operation is possible using a consumption current of only 250 nA and startup power of only 1.2 µW. As a result, even slight amounts of power generation can be obtained from compact solar cells under low-brightness environments of approximately 100 lx. The S6AE101A stores power generated by solar cells to an output capacitor using built-in switch control, and it turns on the power switching circuit while the capacitor voltage is within a preset maximum and minimum range for supplying energy to a load. If the power generated from solar cells is not enough, energy can also be supplied in the same way as solar cells from connected primary batteries for auxiliary power. Also, an over voltage protection (OVP) function is built into the input pins of the solar cells, and the open voltage of solar cells is used by this IC to prevent an overvoltage state. The S6AE101A is provided as a battery-free wireless sensor node solution that is operable by super-compact solar cells.

**Features**
- Input power selection control: Solar cell or primary battery
- Operated by solar cells without the need for primary batteries
- Storage of energy from power supply to storage capacitors
- Output power gating control, output voltage regulation
- Operation input voltage range
  - Solar cell power: 2.0V to 5.5V
  - Primary battery power: 2.0V to 5.5V
- Adjustable output voltage range: 1.1V to 5.2V
- Low-consumption current: 250 nA
- Minimum input power at startup: 1.2 µW
- Input overvoltage protection: 5.4V
- Compact SON-10 package: 3 mm × 3 mm

**Applications**
- Energy harvesting power system with a very small solar cell
- Bluetooth® Smart sensor
- Wireless HVAC sensor
- Wireless lighting control
- Security system
- Smart home / Building / Industrial wireless sensor

**Block Diagram**
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1. Pin Assignment

Figure 1-1 Pin Assignment

(TOP VIEW)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N.C.</td>
<td>-</td>
<td>Non connection pin (Leave this pin open)</td>
</tr>
<tr>
<td>2</td>
<td>VINT</td>
<td>O</td>
<td>Internal circuit storage output pin</td>
</tr>
<tr>
<td>3</td>
<td>VBAT</td>
<td>I</td>
<td>Primary battery input pin (when being not used, leave this pin open)</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>I</td>
<td>Solar cell input pin (when being not used, leave this pin open)</td>
</tr>
<tr>
<td>5</td>
<td>AGND</td>
<td>-</td>
<td>Ground pin</td>
</tr>
<tr>
<td>6</td>
<td>SET_VOUTFB</td>
<td>O</td>
<td>Reference voltage output pin (for connecting resistor)</td>
</tr>
<tr>
<td>7</td>
<td>SET_VOUTH</td>
<td>I</td>
<td>VOUT1 output voltage setting pin (for connecting resistor)</td>
</tr>
<tr>
<td>8</td>
<td>SET_VOUTL</td>
<td>I</td>
<td>VOUT1 output voltage setting pin (for connecting resistor)</td>
</tr>
<tr>
<td>9</td>
<td>VOUT1</td>
<td>O</td>
<td>Output voltage pin</td>
</tr>
<tr>
<td>10</td>
<td>VSTORE1</td>
<td>O</td>
<td>Storage output pin</td>
</tr>
</tbody>
</table>

2. Pin Descriptions

Table 2-1 Pin Descriptions

Figure 2-1 I/O Pin Equivalent Circuit Diagram
3. Architecture Block Diagram

Figure 3-1 Architecture Block Diagram
4. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage (*1)</td>
<td>V\text{MAX}</td>
<td>VDD, VBAT pin</td>
<td>−0.3</td>
<td>+6.9 V</td>
</tr>
<tr>
<td>Signal input voltage (*1)</td>
<td>V\text{INPUTMAX}</td>
<td>SET_VOUTH, SET_VOUTL pin</td>
<td>−0.3</td>
<td>V\text{VDD}</td>
</tr>
<tr>
<td>VDD slew rate</td>
<td>V\text{SLOPE}</td>
<td>VDD pin</td>
<td>−</td>
<td>0.1 mV/µs</td>
</tr>
<tr>
<td>Power dissipation (*1)</td>
<td>P\text{D}</td>
<td>Ta ≤ 25°C</td>
<td>−</td>
<td>1200 (°2) mW</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T\text{TSTG}</td>
<td></td>
<td>−55</td>
<td>+125 °C</td>
</tr>
</tbody>
</table>

*1: When GND=0V

*2: 0ja (wind speed 0m/s): +58°C/W

**Warning:**
1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

5. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage 1 (*1)</td>
<td>V\text{VDD}</td>
<td>VDD pin</td>
<td>2.0</td>
<td>5.5 V</td>
</tr>
<tr>
<td>Power supply voltage 2 (*1)</td>
<td>V\text{VBAT}</td>
<td>VBAT pin</td>
<td>2.0</td>
<td>5.5 V</td>
</tr>
<tr>
<td>Signal input voltage (*1)</td>
<td>V\text{INPUT}</td>
<td>SET_VOUTH, SET_VOUTL pin</td>
<td>−</td>
<td>V\text{INT pin voltage} V</td>
</tr>
<tr>
<td>VOUT1 setting resistance</td>
<td>R\text{VOUT}</td>
<td>Sum of R1, R2, R3</td>
<td>10</td>
<td>5.0 MΩ</td>
</tr>
<tr>
<td>VDD capacitance</td>
<td>C1</td>
<td>VDD pin</td>
<td>10</td>
<td>− µF</td>
</tr>
<tr>
<td>VINT capacitance</td>
<td>C2</td>
<td>VINT pin</td>
<td>1</td>
<td>− µF</td>
</tr>
<tr>
<td>VSTORE1 capacitance</td>
<td>C3</td>
<td>VSTORE1 pin</td>
<td>100</td>
<td>− µF</td>
</tr>
<tr>
<td>VOUT maximum setting voltage</td>
<td>V\text{SYSH}</td>
<td>VSTORE1 pin</td>
<td>1.3</td>
<td>5.2 V</td>
</tr>
<tr>
<td>VOUT minimum setting voltage</td>
<td>V\text{SYSL}</td>
<td>VSTORE1 pin</td>
<td>V\text{SYSH} ≥ 1.7V</td>
<td>1.1</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>Ta</td>
<td>−</td>
<td>−40</td>
<td>+85 °C</td>
</tr>
</tbody>
</table>

*1: When GND = 0V

**Warning:**
1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.
6. Electrical Characteristics

The electrical characteristics excluding the effect of external resistors and external capacitors are shown in below.

Table 6-1 Electrical Characteristics (System Overall)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Input power in start-up</td>
<td>( W_{\text{START}} )</td>
<td>VDD pin, ( T_a = +25^\circ \text{C} ), ( V_{\text{VOUTH}} ) setting = 3V, By applying 0.4 ( \mu \text{A} ) to VDD, when ( V_{\text{OUT1}} ) reaches 3V ( \times 95% ) after the point when VDD reaches 3V.</td>
<td>–</td>
<td>( \mu \text{W} )</td>
</tr>
<tr>
<td>Consumption current 1</td>
<td>( I_{\text{QIN1}} )</td>
<td>VDD pin input current, VDD = 3V, Open VBAT pin, SW2 = OFF, ( T_a = +25^\circ \text{C} ), SET_VOUTFB resistance = 50 ( \Omega ), ( V_{\text{OUT1}} ) Load = 0 mA</td>
<td>–</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>390</td>
<td>nA</td>
</tr>
<tr>
<td>Power detection voltage</td>
<td>( V_{\text{DETH}} )</td>
<td>VDD, VBAT, VINT pin</td>
<td>1.0</td>
<td>1.4</td>
</tr>
<tr>
<td>Power undetection voltage</td>
<td>( V_{\text{DETL}} )</td>
<td>VDD, VBAT, VINT pin</td>
<td>0.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Power detection hysteresis</td>
<td>( V_{\text{DETHYS}} )</td>
<td>VDD, VBAT, VINT pin</td>
<td>–</td>
<td>0.1</td>
</tr>
<tr>
<td>VOUT maximum voltage</td>
<td>( V_{\text{VOUTH}} )</td>
<td>VSTORE1 pin, ( V_{\text{OUT1}} ) Load = 0 mA</td>
<td>( V_{\text{VSYS}} \geq 2\text{V} ) ( V_{\text{SYSH}} \times 0.95 )</td>
<td>( V_{\text{SYSH}} \times 1.050 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{\text{VSYS}} \leq 2\text{V} ) ( V_{\text{SYSH}} \times 0.935 )</td>
<td>( V_{\text{SYSH}} \times 1.065 )</td>
</tr>
<tr>
<td>Input power reconnect voltage</td>
<td>( V_{\text{VOUTM}} )</td>
<td>VSTORE1 pin, ( V_{\text{OUT1}} ) Load = 0 mA</td>
<td>( V_{\text{VSYS}} \geq 2\text{V} ) ( V_{\text{SYSH}} \times 0.90250 )</td>
<td>( V_{\text{VOUTH}} \times 0.95 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{\text{VSYS}} \leq 2\text{V} ) ( V_{\text{SYSH}} \times 0.88825 )</td>
<td>( V_{\text{VOUTH}} \times 0.95 )</td>
</tr>
<tr>
<td>VOUT minimum voltage</td>
<td>( V_{\text{VOUTL}} )</td>
<td>VSTORE1 pin, ( V_{\text{OUT1}} ) Load = 0 mA</td>
<td>( V_{\text{VSYS}} \geq 2\text{V} ) ( V_{\text{SYSL}} \times 0.95 )</td>
<td>( V_{\text{SYSL}} \times 1.050 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{\text{VSYS}} \leq 2\text{V} ) ( V_{\text{SYSL}} \times 0.935 )</td>
<td>( V_{\text{SYSL}} \times 1.065 )</td>
</tr>
<tr>
<td>OVP detection voltage</td>
<td>( V_{\text{OVPH}} )</td>
<td>VDD pin</td>
<td>5.2</td>
<td>5.4</td>
</tr>
<tr>
<td>OVP release voltage</td>
<td>( V_{\text{OVPL}} )</td>
<td>VDD pin</td>
<td>5.1</td>
<td>5.3</td>
</tr>
<tr>
<td>OVP detection hysteresis</td>
<td>( V_{\text{OVPHYS}} )</td>
<td>VDD pin</td>
<td>–</td>
<td>0.1</td>
</tr>
<tr>
<td>OVP protection current</td>
<td>( I_{\text{OPV}} )</td>
<td>VDD pin input current</td>
<td>6</td>
<td>–</td>
</tr>
</tbody>
</table>

Table 6-2 Electrical Characteristics (Switch)

VDD \( \geq 3\text{V} \), VBAT \( \geq 3\text{V} \), VINT \( \geq 3\text{V} \), \( V_{\text{VOUTL}} \geq 3\text{V} \), VSTORE1 \( \geq V_{\text{VOUTL}} \)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>On resistance 1</td>
<td>( R_{\text{ON1}} )</td>
<td>SW1, In connection of VSTORE1 pin and ( V_{\text{OUT1}} ) pin</td>
<td>–</td>
<td>1.5</td>
</tr>
<tr>
<td>On resistance 2</td>
<td>( R_{\text{ON2}} )</td>
<td>SW2, In connection of VDD pin and VSTORE1 pin</td>
<td>–</td>
<td>5.0</td>
</tr>
<tr>
<td>On resistance 4</td>
<td>( R_{\text{ON4}} )</td>
<td>SW4, In connection of VDD pin and VSTORE1 pin</td>
<td>–</td>
<td>5.0</td>
</tr>
<tr>
<td>Discharge resistance</td>
<td>( R_{\text{DIS}} )</td>
<td>VOUT1 pin</td>
<td>–</td>
<td>1.0</td>
</tr>
</tbody>
</table>
7. Functional Description

7.1 Power Supply Control

This IC can operate by two input power supplies, namely, the solar cell voltage VDD and the primary battery voltage VBAT. The voltages at the VDD pin and VBAT pin are monitored, and selection control of the input power supply is performed based on this voltage state (Figure 7-1).

The input power (solar cell or primary battery) is temporarily stored to a capacitor connected to the VSTORE1 pin. When the voltage of the VSTORE1 pin reaches a certain threshold value or higher, the power switching switch (SW1) connects VSTORE1 and VOUT1.

Table 7-1 Input Power Supply Selection Control

<table>
<thead>
<tr>
<th>VDD Voltage (Solar Cell)</th>
<th>VBAT Voltage (Primary Battery)</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DETH}$ (1.55V) or higher</td>
<td>$V_{DETH}$ (1.55V) or higher</td>
<td>VDD input power supply is performed</td>
</tr>
<tr>
<td>$V_{DETL}$ (1.45V) or less</td>
<td>$V_{DETL}$ (1.45V) or less</td>
<td>VDD input power supply is performed</td>
</tr>
<tr>
<td>$V_{DETL}$ (1.45V) or less</td>
<td>$V_{DETH}$ (1.55V) or higher</td>
<td>VBAT input power supply is performed</td>
</tr>
<tr>
<td>$V_{DETL}$ (1.45V) or less</td>
<td>$V_{DETL}$ (1.45V) or less</td>
<td>All paths are disconnected</td>
</tr>
</tbody>
</table>

Figure 7-1 Input Power Selection Control

(a) Switching Between VDD Input and VBAT Input

(b) Switching Between VDD Input and Disconnection of All Paths
1. VDD input voltage operation
This section describes operation when the VDD pin is set as the input power (Figure 7-2).

[1] When the voltage of the VDD pin reaches the power detection voltage ($V_{DETH} = 1.55V$) or higher, the switch (SW2) connects VDD and VSTORE1 (path S1). Also, when the voltage of the VDD pin falls to the power undetection voltage ($V_{DETL} = 1.45V$) or less, SW2 disconnects the path S1.

[2] When the voltage of the VSTORE1 pin reaches the threshold value ($V_{VOUTH}$) or higher that was set by the SET_VOUTH pin, SW2 disconnects the path S1. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage ($V_{VOUTM}$) or less, SW2 connects the path S1 (path S1+S2).

[4] In addition, when the voltage falls to the threshold value ($V_{VOUTL}$) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.
Figure 7-2 VDD Pin Input Power Operation
2. VBAT input voltage operation

This section describes operation when the VBAT pin is set as the input power (Figure 10-3).

[1] When the voltage of the VBAT pin reaches the power detection voltage (VDETH = 1.55V) or higher, the switch (SW2) connects VBAT and VSTORE1 (path S3). Also, when the voltage of the VDD pin falls to the power undetection voltage (VDETL = 1.45V) or less, SW4 disconnects the path S3.

[2] When the voltage of the VSTORE1 pin reaches the threshold value (VVOUTH) or higher that was set by the SET_VOUTH pin, SW4 disconnects the path S3. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (VVOUTM) or less, SW4 connects the path S3 (path S3+S2).

[4] In addition, when the voltage falls to the threshold value (VVOUTL) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.
Figure 7-3 VBAT Pin Input Power Operation

(a) Internal Operation Diagram

(b) Operation Sequence

- VBAT
- VINT
- VSTORE1
- VOUT1
- VOUTM
- VOUTH
- VDETH
- VDETL
- Load
- SW1
- SW4
- SW9

[Diagram showing the internal operation and operation sequence with labels for VBAT, VINT, VSTORE1, VOUT1, VOUTM, VOUTH, VDETH, VDETL, load, SW1, SW4, and SW9 with timing and states for on and off]
3. Input power supply switching

This section describes the input power switching operation (Figure 7-4).

[1] If the voltages of the VDD pin and VBAT pin increase from a state where both are less than the power detection voltage \(V_{DETH} = 1.55V\) so that the voltage of the VDD pin reaches the power detection voltage \(V_{DETH} = 1.55V\) or higher, and operation switches to VDD input power operation back from the stage of disconnecting all paths.

[2] When the voltage of the VBAT pin increases to the power detection voltage \(V_{DETH} = 1.55V\) or higher, if the power from the solar cell is reduced, and when the voltage of the VDD pin falls to the power undetection voltage \(V_{DETL} = 1.45V\) or less, operation switches from VDD input power operation to VBAT input power operation.

[3] When the amount of power supplied from the solar cell increases, and the voltage of the VDD pin reaches the power detection voltage \(V_{DETH} = 1.55V\) or higher, operation switches back to VDD input power operation. After switching, operation is performed based on VDD input power operation.
Figure 7-4 Input Power Switching

(a) Internal Operation Diagram

(b) Operation Sequence


VDD
VINT
VOUT1
VSTORE1
VINT
VOUTM
VOUTH
VDETH (VDD)
VDETL (VDD)

Operation Sequence:

- [1] Operation Stop
- [2] VDD Input Operation
- [3] VBAT Input Operation
- [4] VDD Input Operation

Switch States:

- SW1: off on off on off on off off
- SW2: off on off on off on off off
- SW7: off on off on off on off off
- SW4: off on off on off on off off
- SW9: off on off on off on off off
7.2 Power Gating
This IC has a power gating function for the external system. Once it is detected that the voltage of the VSTORE1 pin has reached the VOUT maximum voltage (VOUTH), the VSTORE1 pin and VOUT pin are connected by an internal switch until the VOUT minimum voltage (VOUTL) is reached.

Figure 7-5 Power Gating Operation

7.3 Discharge
This IC includes a VOUT1 pin discharge function.
When SW1 disconnects the VSTORE1 and VOUT1 path, the discharge circuit is activated between the VOUT1 pin and GND. The power of the VOUT1 pin is discharged to the GND level.

7.4 Over Voltage Protection (OVP Block)
This IC includes an input overvoltage protection (OVP) function for the VDD pin voltage.
When the VDD pin voltage reaches the OVP detection voltage (V_OVPH=5.4V) or higher, the OVP current (I_OVP) from the VDD pin is drawn in for limiting the increase in the VDD pin voltage for preventing damage to the IC. Also, when the OVP release voltage (V_OVPL=5.3V) or less is reached, drawing-in of the OVP current is stopped.

Figure 7-6 OVP Operation
8. Application Circuit Example and Parts list

Figure 8-1 Application Circuit Example

![Application Circuit Diagram](image)

Table 8-1 Parts List

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Item</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>Ceramic capacitor</td>
<td>10 μF</td>
<td>–</td>
</tr>
<tr>
<td>C2</td>
<td>Ceramic capacitor</td>
<td>1 μF</td>
<td>–</td>
</tr>
<tr>
<td>C3</td>
<td>Ceramic capacitor</td>
<td>100 μF</td>
<td>–</td>
</tr>
<tr>
<td>R1</td>
<td>Resistor</td>
<td>6.8 MΩ</td>
<td>*1</td>
</tr>
<tr>
<td>R2</td>
<td>Resistor</td>
<td>2.7 MΩ</td>
<td>*1</td>
</tr>
<tr>
<td>R3</td>
<td>Resistor</td>
<td>9.1 MΩ</td>
<td>*1</td>
</tr>
<tr>
<td>D1</td>
<td>Diode</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

*1: Setting of VOUT maximum voltage: \( V_{VOUTH} \approx 3.3 \text{V} \), VOUT minimum voltage: \( V_{VOUTL} \approx 2.6 \text{V} \).
9. Application Note

9.1 Setting the Operation Conditions

Setting of output voltage (VOUT1)
The resistor connecting the SET_VOUTH pin and SET_VOUTL pin can be changed to set the VOUT1 output voltage of this IC. This is because the VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) are set based on the connected resistance. The SET_VOUTFB pin outputs a reference voltage for setting the VOUT maximum voltage and VOUT minimum voltage. Resistor voltage division can be performed on this reference voltage outside the IC for creating a voltage applied to the SET_VOUTH pin and SET_VOUTL pin.

Figure 9-1 Setting of output voltage (VOUT1)

The VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) can be calculated using the formulas below.

\[
V_{\text{VOUTH}}[\text{V}] = \frac{57.5 \times (R2 + R3)}{11.1 \times (R1 + R2 + R3)}
\]

\[
V_{\text{VOUTL}}[\text{V}] = \frac{57.5 \times R3}{11.1 \times (R1 + R2 + R3)}
\]

The characteristics when the total value for R1, R2, and R3 is from 10 M\(\Omega\) to 50 M\(\Omega\) are shown in "6. Electrical Characteristics".
9.2 PCB Layout

Take into account the following points when designing the layout.
- Try to route the wiring for the diode (D1) and input capacitor (C1) for connecting the solar cell on the top layer as much as possible, and avoid implementing a connection using a through hole.
- For the AGND pin of S6AE101A, provide a through hole nearby, and connect it to the GND plane.
- Locate the capacitor (C2) for the internal power as near as possible to the VINT pin.
- Locate the resistors (R1, R2, R3) for setting the output voltage in a grid-type configuration with small loops, and locate them as near as possible to each pin (SET_VOUTFB, SET_VOUTH, SET_VOUTL). Also, removing the GND plane under the parts can be effective in preventing malfunctions due to the leakage current.
- To prevent a leakage current, locate and route the storage capacitor (C3) as far as possible from patterns that are different from the electrical potential of VSTORE1 (such as the GND line). Generally, the insulation resistor of printed circuit boards is extremely high, and normally, the passing of leakage current through the board does not pose a problem. However, in certain rare cases, the surface of the board may have a low insulation resistance, and when using these boards, a leakage current that cannot be ignored may occur.

Figure 9-2 PCB Layout Example

10. Development Support

This IC has a set of documentation, such as application notes, development tools, and online resources to assist you during your development process. Visit www.cypress.com/energy-harvesting to find out more.
11. Reference Data

For the circuit diagram of the reference data, Refer to "Figure 8-1 Application Circuit Example".

**Figure 11-1 Reference Data**

- **I\text{\textsubscript{DIN}} vs V\text{\textsubscript{DD}}**
  - V\text{\textsubscript{BAT}} voltage = 0V, SW2 = OFF, R\text{\textsubscript{VOUT}} = 50 M\text{\Omega}
  - V\text{\textsubscript{VOUTH}} = 1.3V, V\text{\textsubscript{VOUTL}} = 1.1V
  - T\text{\textsubscript{A}} = +95°C
  - T\text{\textsubscript{A}} = +25°C
  - T\text{\textsubscript{A}} = −40°C

- **R\text{\textsubscript{ON}} vs Temp.**
  - V\text{\textsubscript{DD}} = 3V

- **R\text{\textsubscript{ON}} vs Temp.**
  - V\text{\textsubscript{DD}} = 3V

- **V\text{\textsubscript{DETH}}, V\text{\textsubscript{DETL}} (of V\text{\textsubscript{DD}}) vs Temp.**

- **V\text{\textsubscript{DETH}}, V\text{\textsubscript{DETL}} (of V\text{\textsubscript{BAT}}) vs Temp.**

- **V\text{\textsubscript{DETH}}, V\text{\textsubscript{DETL}} (of V\text{\textsubscript{INT}}) vs Temp.**

- **VDD Input Power Supply**
  - V\text{\textsubscript{DD}} current = 4 µA, V\text{\textsubscript{VOUT1}} current = 1 µA, C\text{\textsubscript{3}} = 100 µF, T\text{\textsubscript{A}} = +25°C
  - V\text{\textsubscript{VOUTH}} = 5.2V, V\text{\textsubscript{VOUTL}} = 4.68V
  - V\text{\textsubscript{VOUT1}} current = 1 µA, C\text{\textsubscript{3}} = 100 µF, T\text{\textsubscript{A}} = +25°C
  - V\text{\textsubscript{VOUTH}} = 5.2V, V\text{\textsubscript{VOUTL}} = 4.68V
12. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.
- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.
The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

13. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

14. Ordering Information

Table 14-1 Ordering Part Number

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<th>Part number (MPN)</th>
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<tr>
<td>S6AE101A0DGNAB000</td>
<td>10-pin plastic SON (0.5mm pitch)</td>
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<td>(VNE010)</td>
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MPN: Marketing Part Number

Figure 14-1 Ordering Part Number Definitions

- Fixed on 000
- Packing: B = 13 inch Tape and Reel (ER)
- Package: NA = SON, Pd-PPF/Low-Halogen
- Reliability Grade: G = 100 ppm (Commercial Sample)
- Preset Condition
- Revision: A = 1st Revision
- Product ID: 01
- Topology: 1 = Buck Power Supply
- Product Type: E = Energy Harvesting PMIC
- Product Class: 6A = Consumer Analog
- Company ID: S = Cypress
15. Package Dimensions

**NOTES:**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.

**DIMENSION **b** ” APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION **b**” SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

5. MAXIMUM NUMBER OF TERMINALS ON D OR E SIDE.

6. MAX. PACKAGE LAYOUT IS 0.05 mm.

7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.

9. BLATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

**REFERENCES: **

3.00X3.00X0.9 MM 802D10 2.2X1.6 SMF (SAW N) PTH **REV**
16. Major Changes

Spansion Publication Number: S6AE101A_DS405-00026

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<td>Initial release</td>
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NOTE: Please see “Document History” about later revised information.

Document History

Document Title: S6AE101A Energy Harvesting PMIC for Wireless Sensor Node
Document Number: 002-08493

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Document Number: 002-08493 Rev. *D
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