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Understanding Typical and Maximum Program/Erase Performance

This application note discusses the typical and maximum program/erase performance of Cypress flash memory devices.

1 Overview

Flash program and erase performance characteristics are often misunderstood. Unlike other memory devices that provide a single access time for both reading and writing, flash memory is read much faster than it is programmed. In addition, because programming times vary greatly, publishing single write times for flash devices is very misleading to both system and board designers.

2 Typical and Maximum Values Calculations

Typical and maximum program/erase values in Spansion data sheets are derived from testing many individual devices and tightly controlling the manufacturing process.

Calculating typical values is fairly straightforward. A large number of devices with a checkerboard bit pattern are programmed, then erased. The program and erase process is repeated up to one million times at a constant temperature of 25°C. The timing results from every program and erase operation for all devices is then used to calculate the mean program/erase time. This is the process by which the typical value (the 50% point in Figure 1) is calculated.

Figure 1. Gaussian Distribution

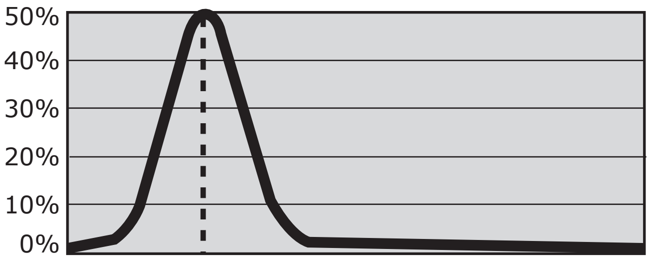
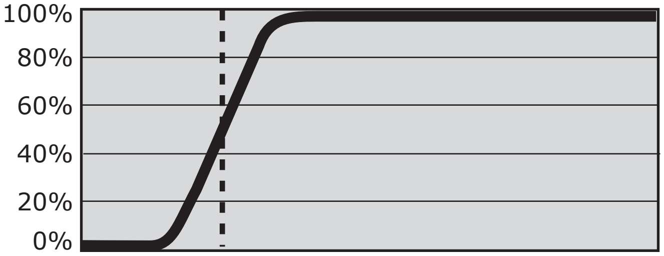


Figure 2. Cumulative Gaussian Distribution



Maximum values are derived from understanding memory structures in the device, extensive testing, and studying the Gaussian-like distribution of program/erase times. Unlike typical values, maximum values show how the device functions in the absolute worst conditions; the temperature is set to at least 90° C (194° F), V_{CC} is lowered to the minimum operating voltage, and the parts are programmed/erased for the maximum (up to 1,000,000) number of times.

3 Reading the Erase and Programming Performance Chart

Consider the erase and programming performance characteristics in Table 1 that are taken from a 128-Mb (8-M x 16-Bit) device with sixteen 4-Kword sectors and two hundred fifty-four 32-Kword sectors.

Table 1. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword	0.4	5	s	Excludes 00h programming prior to erasure (Note 4)
	4 Kword	0.2	5		
Chip Erase Time		103		s	
Word Programming Time		9	210	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time		4	120	µs	
Chip Programming Time (Note 3)		75.5	226.5	s	Excludes system level overhead (Note 6)
Accelerated Chip Programming Time		33	99	s	

Notes

1. Typical program and erase times assume the following conditions: 25° C, V_{CC} = 1.8 volts, 1 million cycles. Additionally, programming typicals assumes a checkerboard pattern.

2. Under worst-case conditions of 90° C, V_{CC} = 1.65 volt, 1 million cycles.

3. The typical chip programming time is considerable less than the maximum chip programming time listed.

4. In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.

5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command.

6. The device has a minimum erase and program cycle endurance of 100,000 cycles.

In the example above, maximum values are much longer than typical values because of the different operational conditions (temperature, voltage, etc.) that are used for typical and maximum value testing.

Note the chip programming time. The *typical* chip programming time is calculated as 9 µs multiplied by 8 Mwords (1 Mword = 1,048,576 words, not 1,000,000 words), resulting in a typical chip programming time of 75.5 seconds.

The *maximum* chip programming time, however, is calculated slightly differently. It is not calculated simply as 210 µs, multiplied by 8-Mwords, equaling 1,761.6 seconds; rather, the maximum chip programming time is 226.5 seconds. Due to the silicon manufacturing process and statistics, maximum chip programming time is not calculated simply by multiplying the maximum word programming time by the number of words in the device.

When flash memory cells are manufactured, the individual cells in the array program and erase at slightly different rates following a Gaussian-like distribution. A very high percentage of cells program and erase around the typical value. Each time a cell is programmed or erased, the measured timing difference is very slight (on the order of picoseconds). Sometimes the cell programs faster and sometimes it programs slower, trending toward a higher probability of programming more slowly, the more times it is erased. The maximum program/erase times listed in Table 1 specify the slowest-performing cell in the device, after the listed number of erase cycles and under worst-case conditions.

Given this data, application engineers attempt to answer the following question:

- In this example, do all cells of the device take the maximum time to program/erase after one million cycles?

  In short, the answer to this question is no. Based on experiments, an absolute worst-case program specification is calculated to have approximately 10% of the words programming at the maximum time, while the other 90% program at the typical rate (also assuming 90° C, V_{CC} = 1.65 volts after 1,000,000 cycles, in the case of the example from Table 1).

4 System Performance

When evaluating system performance, the sustained transfer rate measured in bytes per second (or bits per second) is typically the key benchmark. For normal operating voltage and temperature, the device described in Table 1 can be programmed at over 220 Kb/s (2 bytes/9 µs) or 1.78 MB/s.

Many designers develop for the worst case, and use the 2 bytes/210 µs (9.5 Kb/s) to calculate the worst-case transfer rate. As illustrated in the previous section, this is inaccurate, because at most, only 10% of the words program at 210 µs. The true worst-case transfer rate would be 1,048,576 * 16 bytes/226.5 s, (74.1 Kb/s) which is nearly eight times the performance of the first calculation.

In addition, using the worst-case approach to calculate system performance is not realistic. It assumes that the device is at the end of its life, having been cycled 1,000,000 times (in the example device shown in Table 1). Using typical timing, achieving this would take over five and a half years, require low V_{CC} voltages, and operate at 90° C for the entire duration (a temperature well above what most systems can tolerate).

Watchdog timers for individual program/erase cycles should be set to the *maximum* time listed, not the *typical* time. The typical values are the mean of the operational time at 25° C, not the maximum.

5 Conclusion

The maximum values provided in the data sheet are true absolute worst-case operations under worst-case conditions, and are not indicative of performance in most applications. Most systems can expect typical program/erase times on the flash for the life of the system.

Maximum values cannot be relied upon for calculating system performance or estimating the *age* of a part. Finally, the typical values are the mean values in a Gaussian-like distribution over the life of the part, which must not be confused with the initial device timing or the maximum timing under typical operating conditions.

Document History Page

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