Cypress Semiconductor
Package Qualification Report

QTP# 151404 VERSION**
October 2015

99-Ball Wafer Level Chip Scale Package (WLCSP), 5.19 x x5.94 x 0.6 mm
MSL1, 260C
Deca Technologies (DT) - Philippines

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PACKAGE QUALIFICATION HISTORY

QTP Number	DESCRIPTION OF QUALIFICATION PURPOSE	Date
112201	Qualify WLCSP assembly in Deca Technologies (DT) Philippines for Wafer Processing and Die Finishing Steps using SAC 405 Solder Finish, at MSL1, 260C	Oct 2011
151404	Qualify 99-Ball WLCSP (5.19x5.94x0.6mm) Package at Deca Technologies (DT) using SAC405 Solder Finish at MSL1,260C	Oct 2015

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	FN81B,FN60B
Package Outline, Type, or Name:	81-Ball Wafer Level Chip Scale Package (WLCSP) (3.9 x 3.9 x 0.55mm) 99-Ball Wafer Level Chip Scale Package (WLCSP) (5.19 x 5.94 x 0.6 mm)
Die Backside Preparation Method:	Backgrind
Die Separation Method:	Saw
Solder Ball/Bump Material:	SAC405
Bonding Method:	Bump/ RDL
Bond Diagram Designation:	001-69859, 001-88811
Thermal Resistance Theta JA °C/W:	24°C/W , 16.55°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-69882
Name/Location of Assembly (prime) facility:	DT-Philippines
MSL Level	1
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	DT-Philippines

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Constructional Analysis	Criteria: Meet external and internal characteristics of Cypress package	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500 JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V/2,200V/3,300V JEDEC EIA/JESD22-A114	P
External Visual	MIL-PRF-38535, MIL-STD-883, METHOD 2009	P
Final Visual	JESD22-B101	P
Functional Board Level Reliability Test (FBLRT)	Temperature Cycle, -40°C to 85°C	P
High Accelerated Saturation Test (HAST) – No Bias	JEDEC STD 22-A110: 130C, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 1 (168 Hrs.,85°C, 85%RH, 260°C Reflow)	P
Highly Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130C, 85%RH, 1.98V Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs.,85°C, 85%RH, 260°C Reflow)	P
High Temperature Storage	150°C, no bias	P
Internal Visual	MIL-STD-883-2014	P
Soft Error Test	Vcc nom, room temperature, JESD89	P
Physical Dimension	MIL-STD-1835, JESD22-B100	P
Pressure Cooker Test	JESD22-A102:121°C /100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs.,85°C, 85%RH, 260°C Reflow)	P
Solder Ball/Bump Shear	JESD22-B117	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition B, -55°C to 125°C Precondition: JESD22 Moisture Sensitivity MSL 1 (168 Hrs.,85°C, 85%RH, 260°C Reflow)	P
Thermal Shock	MIL-STD-883, Method 1011, Condition B, -55 C to 125C and JESD22-A106, Condition C, -55 C to 125C	P

Reliability Test Data

QTP #: 112201

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: CONSTRUCTIONAL ANALYSIS							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	COMP	5	0	
STRESS: EXTERNAL VISUAL							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	COMP	1558	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	COMP	1621	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	COMP	1356	0	
STRESS: ELECTRICAL CHARACTERIZATION							
CYWB0226ABSX (7C071011C)	4046829	404682925	DT-PHIL	COMP	1 wafer	0	
STRESS: INTERNAL VISUAL							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	COMP	5	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	COMP	5	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 1.98V, PRE COND 168 HR 85C/85%RH, MSL1							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	96	67	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	96	72	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	500	79	0	
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	1000	77	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 168 HR 85C/85%RH, MSL1							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	96	77	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	96	76	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	96	78	0	
STRESS: PHYSICAL DIMENSION							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	COMP	30	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	COMP	30	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	COMP	30	0	

Reliability Test Data

QTP #: 112201

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SOLDER BALL/BUMP SHEAR							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	COMP	30	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	COMP	30	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	COMP	30	0	
STRESS: TC COND. B -55C TO 125C, PRE COND 168 HRS 85C/85%RH, MSL1							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	500	78	0	
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	1000	78	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	500	78	0	
CYWB0226ABSX (7C071011C)	4024545	402454505	DT-PHIL	1000	78	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	500	79	0	
CYWB0226ABSX (7C071011C)	4024545	402454507	DT-PHIL	1000	79	0	
STRESS: THERMAL SHOCK							
CYWB0226ABSX (7C071011C)	4024545	402454503	DT-PHIL	200	80	0	

Reliability Test Data

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Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: CONSTRUCTIONAL ANALYSIS							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	COMP	5	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	500	9	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1000	3	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1100	3	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	2200	8	0	
STRESS: INTERNAL VISUAL							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	COMP	5	0	
STRESS: FINAL VISUAL							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	COMP	654	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	COMP	608	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	COMP	1338	0	
STRESS: FUNCTIONAL BOARD LEVEL RELIABILITY TEST, TC COND.N -40C TO 85C							
CY8C5888FNI (8C561001A)	N/A	N/A	DT-Phils	256	460	0	
STRESS: PHYSICAL DIMENSION							
CY8C5888FNI (8F561001AC)	4438064	611528220	DT-Phils	COMP	30	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 168 HR 85C/85%RH, MSL1							
CY8C5888FNI (8F56000AC)	4429807	4429807	DT-Phils	96	80	0	
CY8C5888FNI (8F561001AC)	4503922	611514039A	DT-Phils	96	80	0	
CY8C5888FNI (8F561001AC)	4503922	611514039A	DT-Phils	168	80	0	
CY8C5888FNI (8F561001AC)	4503922	611514039B	DT-Phils	96	80	0	
CY8C5888FNI (8F561001AC)	4519077	611525393	DT-Phils	96	80	0	

Reliability Test Data

QTP #: 151404

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. B -55C TO 125C, PRE COND 168 HRS 85C/85%RH, MSL1							
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	500	80	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1000	80	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	500	79	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1000	79	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	500	79	0	
CY8C5888FNI (8C561001A)	4333263	4333263	DT-Phils	1000	79	0	

Document History Page

Document Title: QTP#151404: 99-BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP), 5.19 X X5.94 X 0.6 MM MSL1, 260C DECA TECHNOLOGIES (DT) - PHILIPPINES
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Rev.	ECN No.	Orig. of Change	Description of Change
**	4991755	HSTO	Initial spec release.