AN98561

Interfacing i.MX3x to S29GL MirrorBit® NOR Flash

AN98561 highlights the i.MX3x device features, like the WEIM for interfacing external memories like the S29GL NOR flash.

1 Abstract

The Freescale™ i.MX3x Multimedia Applications processors and Cypress® MirrorBit® Flash Technology are utilized extensively in today's embedded applications. The product families covered by this application note provide solutions for consumer, industrial, networking, and automotive markets. The application note will highlight the i.MX3x device features, like the WEIM for interfacing external memories like the S29GL NOR flash. Section 3, *i.MX3x and S29GL Interface Considerations* on page 5 highlights the basic interface and setup consideration when interfacing the i.MX3x SOC to access the S29GL NOR flash.

2 Overview and Background

2.1 Introduction

The initial discussion provides a very brief overview of the Freescale i.MX31 and i.MX35x Multimedia Applications Processor and Cypress S29GL-S MirrorBit Flash Family. The intent is to introduce the i.MX3x processor Wireless External Interface Module (WEIM) which handles the interface to external memory devices like the Cypress's S29GL NOR flash.

2.2 Freescale i.MX3x Multimedia Applications Processor

The i.MX3x Multimedia Applications Processors based on an ARM11™ microprocessor core running up to 532 MHz, provide the performance, power consumption, connectivity, and media capabilities to drive multimedia applications for a broad range of consumer, industrial and automotive applications.

Freescale highlights the i.MX3x multimedia applications processor as ideal for computationally-intensive applications such as automotive entertainment systems, video and audio media players, mobile gaming consoles and GPS systems, as well as smart phones, PDAs, ultra-portable handheld computers and other devices. The i.MX3x processor includes leading power management, security management, digital rights management and image processing technology – a formidable combination of features that OEMs desire to drive high-performance video, audio, and 3D gaming content on wireless mobile devices. The processors are designed with Freescale's Smart Speed Technology that enables ultra low power consumption.

The i.MX3x processor's Wireless External Interface Module (WEIM) provides the flexibility to interface a wide range of memories. WEIM includes generation and control for chip selects, clock and control signals for external peripherals and memory (NAND, NOR, SRAM, and others). The i.MX3x can access SRAM and NOR flash devices using asynchronous, synchronous, multiplex, or non-multiplex accesses. The configuration of the memory subsystem depends on factors such as system performance, storage size requirements, power consumption, and expected product life cycles.

WEIM Supports Six Chip Selects for external devices

- CS0 and CS1 each covering a range of 128 Mbytes
- CS2 - CS5, each covering a range of 32 Mbytes
- CS0 range can be extended to 256 Mbytes when merged with CS1
- Selectable Protection for each Chip Select, Programmable Data Port Size for each Chip Select
- Asynchronous accesses with programmable setup and hold times for control signals
- Synchronous Memory Burst Read Mode support for Cypress, and Numonyx (Micron®) burst flash memory

- Synchronous Memory Burst Write Mode support for PSRAM
- Support for multiplexed address / data bus operation
- Programmable Wait-State generator for each Chip Select
- Support for Big Endian and Little Endian modes of operation per access

Figure 1. i..MX35x Block Diagram

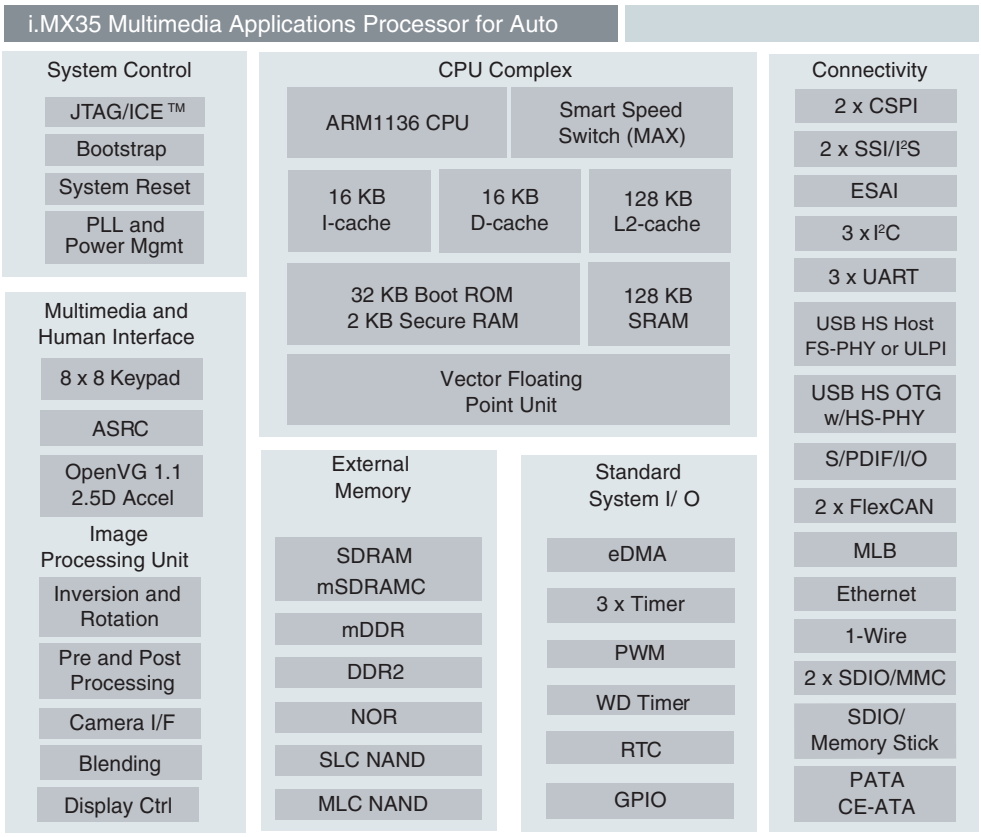
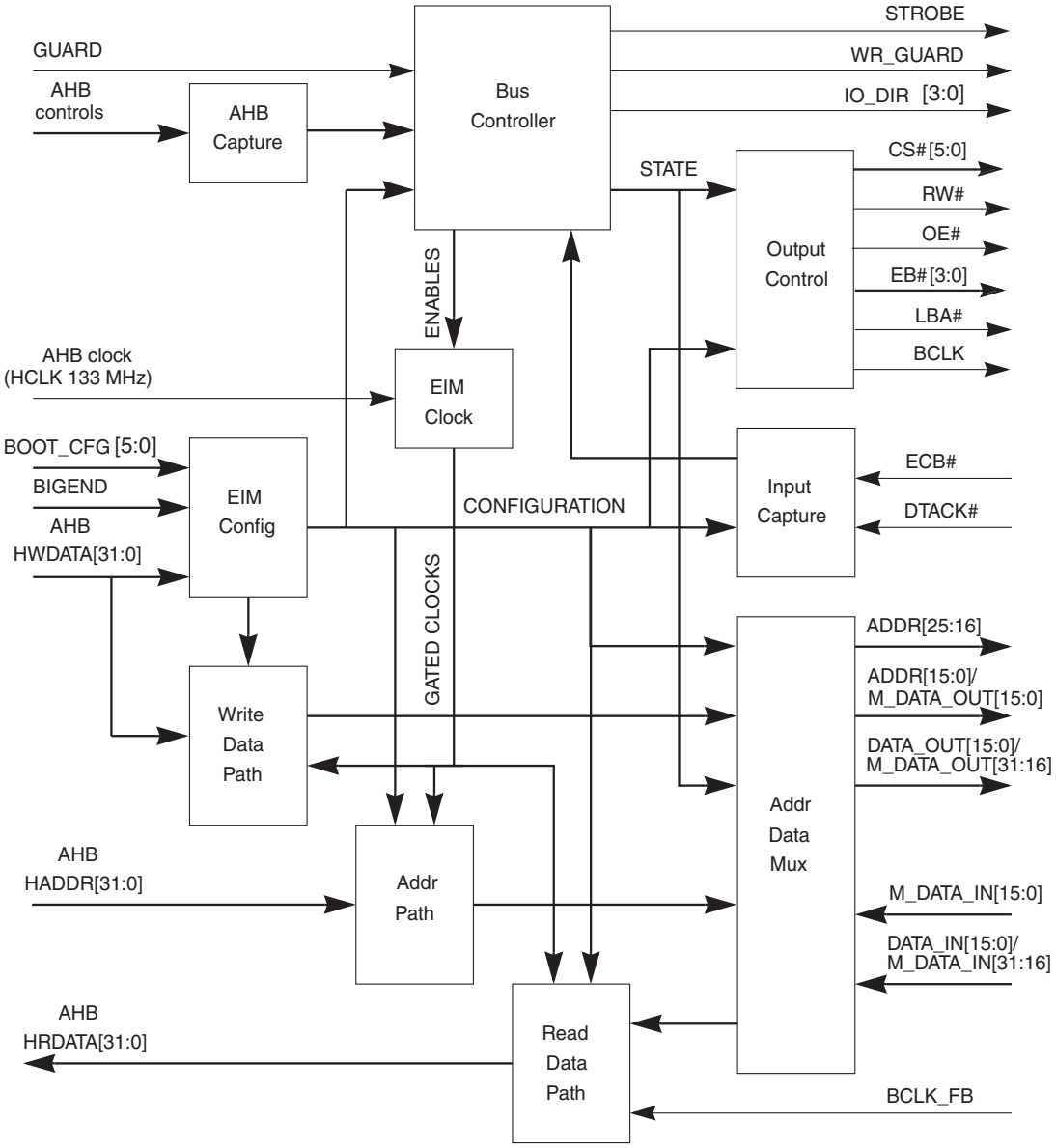


Figure 2. WEIM Block Diagram



2.3 Cypress S29GL MirrorBit NOR Flash Family

Cypress S29GL MirrorBit Flash Families are the leading price-performance flash memory technology for embedded applications. The S29GL MirrorBit technology enables designers to create innovative and cost-effective solutions. This product family offers densities from 32 Mb (4 MB) to 2 Gb (256 MB) with option to support 3.3V or 1.8V interfaces. The S29GL offers a V_{IO} option separating the I/O from the main V_{CC} power supply which enables a direct interface with the i.MX3x family configured for 1.8V I/O. The S29GL family is characterized by extensive longevity and maintaining compatibility of new products with the previous generations. The S29GL also features a universal package footprint across devices densities for both BGA and TSOP packages. These features can be leveraged across a product line offering reduced cost and time-to-market. Other Cypress 1.8V S29WS/VS and MCP families can be adopted in the i.MX3x platforms.

Cypress's latest S29GL-S Family offers the new Eclipse™ architecture fabricated on 65 nm process technology. These devices offer a fast page access time of 15 ns and random access times that are comparable with previous generations. The MirrorBit Eclipse architecture enables high bandwidth programming up to 1.5 MB/s approximately 11x faster than previous generation NOR flash technologies. This makes these devices ideal for today's embedded applications requiring high density, and improved read / program performance. Table 1 summarizes the feature comparison between the Eclipse S29GL-S and previous generations of S29GL MirrorBit products.

Table 1. Feature Comparison for S29GL MirrorBit Family

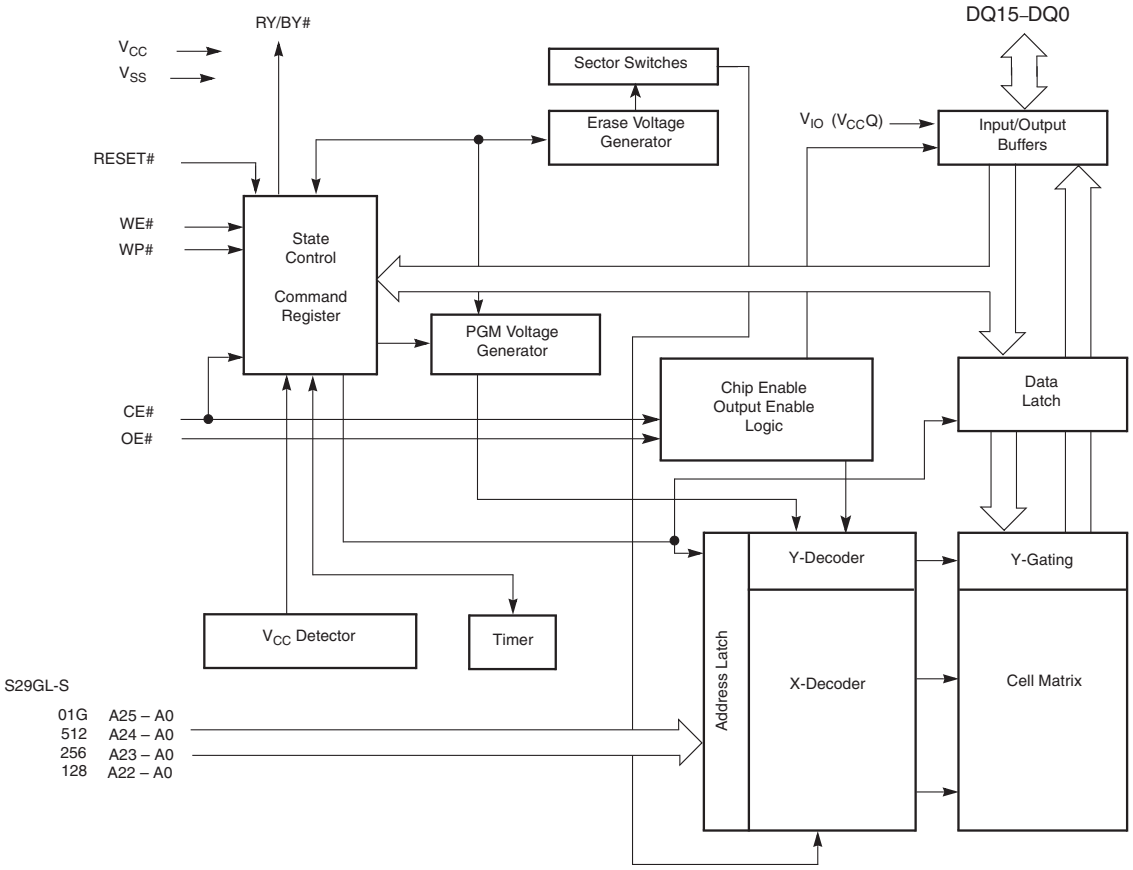
Feature	S29GL-N 110 nm (1)	S29GL-P 90 nm (2)	S29GL-S Eclipse 65nm
Density	32 Mb - 512 Mb	128 Mb - 1 Gb	128 Mb to 1 Gb
V_{CC}	2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V
Temperature Range	-40 to 85°C -40 to 105°C (Read)	-40 to 85°C	-40 to 85°C -40 to 105°C
Common Flash Interface (CFI)	Yes	Yes	Yes
Lithography Node	110 nm	90 nm	65 nm
Page Read/Write Buffer	8 / 16 word	8 / 32 word	16 / 256 word
Program/ Erase BW	~133 kB/s / 250 kB/s	~133 kB/s/ 250 kB/s	~1.5 MB/s / 655 kB/s
Secure Silicon Sector (OTP)	256 byte OTP	256 byte OTP	1024 byte:2x512 byte OTP
Security	ASP	ASP	ASP; Write and Read protect
Software Command Set	Yes	GL-N Compatible	GL-P Compatible
Power-on Reset	500 ns	~35 µs	~300 µs
Bus Width	x8 or x16	x8 or x16	x16 only
Embedded Operation Status	Data Polling	Data Polling	Data Polling / Status Register
Erase Sector size	128 kB (3)	128 kB	128 kB

Notes:

1. *GL-N information is provided for reference only.*
2. *GL-P is not recommended for new designs.*
3. *The Sector Size for the GL032N and GL064N is 64 kB.*

Figure 3 is a typical Block Diagram for an S29GL Asynchronous / Page Mode access MirrorBit Flash.

Figure 3. S29GL Asynchronous/Page Mode Block Diagram



3 i.MX3x and S29GL Interface Considerations

This section considers the interface requirements for an i.MX35 and S29GL256S. Note the i.MX31 and i.MX35 each use the WEIM controller to interface to external memory devices. Note a particular i.MX3x device data sheet or reference manual should be referenced to determine the detailed interface options offered for that device.

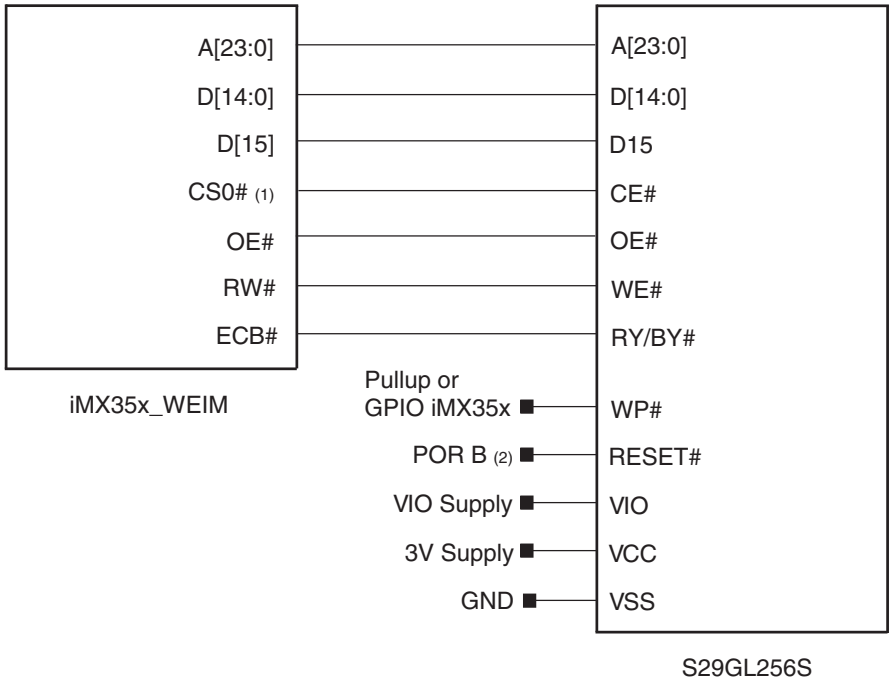
3.1 Hardware Interface

As stated earlier, the i.MX3x WEIM is capable of supporting asynchronous, page, synchronous, multiplexed address/data and non-multiplex modes. This section discusses details for interfacing the i.MX35 and S29GL256S to support asynchronous/page non-muxed accesses.

3.1.1 High Level i.MX35x to S29GL256S Interface

Figure 4 shows the signal interface from the i.MX35x WEIM bus to a S29GL256S 32-Mbyte NOR flash. The i.MX35 NVCC_NAND, NVCC_EMI3, and NVCC_EMIx can be configured to support 3.3V or 1.8V interface options and the S29GL-S Family also supports V_{IO} option also enable interfacing to 3.3V or 1.8V bus.

Figure 4 .Interface Diagram for i.MX35 to S29GL256S



Notes:

1. *CS0 required for boot.*
2. *RESET should be connected to same POR_B as i.MX35 (driven by external device).*

3.1.2 Interface Diagram for i.MX35 to S29GL256S

The i.MX3x EMI I/O interface power supply should be set up according to external memory requirements. Reference the iMX3x data sheet for additional details.

3.1.3 i.MX35x Detailed Connections to S29GL256S

Table 2 below shows detailed iMX35 to the S29GL256S signal interface and descriptions.

Table 2,. Detailed Signal Interface i.MX35x to S29GL256S

i.MX35x Signals	S29GL256S	Description/Remarks
A23-A0	A23-A0	Word Access for 256 Mbit: S29GL256S
CS[0]	CE#	Additional GL flash memories can be connected to any of the WEIM chip-selects lines CS[0:5], sharing the other control signals, addresses and data. The following address space limitation should be considered for the chip-select line. CS[0] and CS[1] 1 Gbit/128 MBytes each CS[2] … CS[5] 256 Mb/32 MBytes each
DATA_IN[15:0]	DQ15-DQ0	I/O Data Lines. The S29GL-S flash family are word mode accesses(X16).
OE#	OE#	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH}, causes outputs to be high impedance (High-Z).
RW#	WE#	Read/Write signal. It is active low during a write cycle, active high during a read cycle.
	WP#	Write Protect Signal. It can be connected either to a jumper or to a GPIO of the i.MX35. When it is asserted low, either the highest or lowest sector is protected from undesired erase/program operations.
POR#	RESET#	The reset signal is active low and it can be generated using several techniques from the i.MX reset module (e.g. POR# pin). The user needs to make sure that from the reset signal going low to the first valid access (CS# low) the reset timings meet data sheet specification.
ECB#	RY/BY#	The S29GL-S RY/BY# pin indicates if an embedded flash operation is in progress.

Table 3. S29GL-S Signal Description

Symbol	Typ	Description
A26-A0	Input	Address Inputs A25-A0 for S29GL01GS A24-A0 for S29GL512S A23-A0 for S29GL256S A22-A0 for S29GL128S
DQ15-DQ0	Input/Output	Data Inputs and Outputs
CE#	Input	Chip Enable. At V_{IL}, selects the device for data transfer with the host memory controller.
OE#	Input	Output Enable. At V_{IL}, causes outputs to be actively driven. At V_{IH}, causes outputs to be high impedance (High-Z).
WE#	Input	Write Enable. At V_{IL}, indicates data transfer from host to device. At V_{IH}, indicates data transfer is from device to host.
RESET#	Input	Hardware Reset. At V_{IL}, causes the device to reset control logic to its standby state, ready for reading array data.
WP#	Input	Write Protect. At V_{IL}, disables program and erase functions in the lowest or highest address 64 kword (128 kB) sector of the device. At V_{IH}, the sector is not protected. WP# has an internal pull up; When unconnected WP# is at V_{IH}.
RY/BY#	Output	Read/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively engaged in an Embedded Algorithm such as erasing or programming. At High-Z, the device is ready for read or a new command write – requires external pull-up resistor to detect the High-Z state. Multiple devices may have their RY/BY# outputs tied together to detect when all devices are ready.
V_{CC}	Input	Core Power Supply.
V_{IO}	Input	Versatile IO power supply.
V_{SS}	Input	Power supplies ground.

3.2 i.MX3X Configuration Register Considerations

3.2.1 Assumptions and General Setup

- i.MX35x AHB Clock Frequency ≥ 133 MHz
- i.MX35x Boot Configuration ≥ External non-muxed 16-bits wide data bus mode on CS0#
- S29GL256S device has an initial access time between 90 and 110 ns

The WEIM boot configuration is determined based on inputs to the device at power on reset and fuse settings. The main boot modes are controlled by dedicated boot pins, BOOT_MODE0 and BOOT_MODE1. The device also uses a number of eFUSEs during the boot process to further determine specific boot mode and boot path. The fuse value can be determined by IIM or GPIO pins with the control of GPIO_BT_SEL fuse. When the GPIO_BT_SEL fuse is cleared, the boot configuration fuse value is determined by GPIO pins as follows.

Upon power-on reset (POR_B) the i.MX35x processor samples the boot mode pins BMOD[1:0] as well as the state of internal boot mode fuses to determine the type of boot. In order to boot from the S29GL256S, the i.MX35 must be set to external boot - BMOD[1:0] - and the fuses must reflect boot from WEIM in 16 bit mode. See “Chapter 7 - Boot” in the i.MX35x Reference Manual for detailed description of the fuse settings.

Pin Name	eFUSE Name	Setting at Boot
BOOT_MODE0	N/A	0 (External boot)
BOOT_MODE1	N/A	1
CSI_D8 INPUT	BT_MEM_CTRL[0]	0 (WEIM)
CSI_D9 INPUT	BT_MEM_CTRL[1]	0
CSI_D10 INPUT	BT_MEM_TYPE[0]	0 (NOR)
CSI_D11 INPUT	BT_MEM_TYPE[1]	0
CSI_VSYNC	BT_BUS_WIDTH	0 (16 bit)

There are four WIEM configuration registers that directly affect WEIM access for CS0. The WEIM Control Register, the Upper and Lower Chip Select 0 Control Registers, and the Chip Select 0 Additional Control register. All four registers are highlighted in the following sections.

The first register to take into consideration is the WCR. WCR defines the burst clock operations. The S29GL256S flash does not require a burst clock. The WCR also defines if CS0 and CS1 address space merged. For a S29GL256S the default settings are appropriate.

CS configuration register are divided into three “Chip Select Configuration Registers” (CSCR) called “Upper”, “Lower” and “Additional” of 32 bits each. The CSCR0-Upper register contains parameters of the burst/page mode read access and the wait-states to match the page access and initial random access time. The duration of one wait state is related to the i.MX3x AHB clock frequency (typ. 133 MHz, T_{CK} = 7.52 ns). Note the S29GL-S supports both asynchronous and 16-word page read accesses. The write cycle time duration is less critical than the read access time. No additional wait-states are required for the write cycle. In order to have a relaxed negation time of CS0# during back-to-back read and write, a negation time of 30 ns is recommended. The CSCR0-Lower register contains parameters to define the OE# and CS0# assertion and negation during a cycle. The CS0# can be activated at the beginning of the read/write cycle and negated at the end. OE# can be asserted at the beginning of the read cycle and negated at the end as well. The register also contains the memory bank activation and the port size (data bus width) definition. The desired configuration is non-A/D mux 16-bit port. The CSCR0-Additional contains a definition of the A/D mux/demux bus configuration, too. It also defines the WE assertion/negation timings. No special settings are required. WE# can be asserted at the beginning of the write cycle and negated at the end. Similar approaches can be extended to other i.MX processors. Refer to the related user manuals for additional information.

Freescale offers i.MX3x evaluation kits already contain sample software providing examples for proper register configurations. Some changes may be required to match or optimize the S29GL256S timings
read/write access timings.

3.2.2 Example Setup

The following provide a simple configuration setting setup for the i.MX35x and S29GL256S Configuration Registers to enable asynchronous non-multiplexed flash accesses. Note the user may desire to modify these settings to optimize access times or to perform additional access modes such as Page Read Mode access.

3.2.2.1 i.MX35x WEIM Configuration Register

The WCR contains two parameters that define the burst clock operation and merged address operation.

Bit	**MSB**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Value	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	1	RSVD	0

3.2.2.2 i.MX35x Chip Select 0 Upper Control Register

Bit	**MSB**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Value	0	0	00		0000				00		0	0	0000			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	10		01_011						0	000			0000			

3.2.2.3 i.MX35x Chip Select 0 Lower Control Register

Bit	**MSB**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Value	0	0	00		0000				00		0	0	0000			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	0000				0	101			0000				0	0	0	0

3.2.2.4 i.MX35x Chip Select 0 Additional Control Register

As stated earlier, the default reset values for CSCR0A are appropriate to make non-multiplexed asynchronous accesses.

Bit	MSB	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value	EBRA				EBRN				RWA				RWN			
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	MUM	LAH			LBN			LBA	DWW		DCT		WWU	AGE	CNC2	FCE

4 Support Tools

Freescale and Cypress each offer extensive support for their product portfolios.

Freescale offers substantial product documentation and a number of i.MX3x Product Development Kits (PDK), which provide a functional hardware platform and software solution to enable engineers to develop with the i.MX3x processor.

Check Cypress web site for Cypress's Tool support including Product Documentation, SW Drivers, Simulation Models, Hardware Development Tools, and other support items.

5 Conclusion

Freescale's i.MX3x Multimedia Applications processors and Cypress's S29GL-S MirrorBit Flash Technology are utilized extensively in today's embedded applications. The product families covered by this application note provide solutions for consumer, industrial, networking, and automotive markets. This application note provides a brief highlight of some of the devices key product features and outlines an example case illustrating the hardware and configuration consideration when interfacing i.MX35x SOC to the S29GL256S flash. The S29GL-S MirrorBit NOR flash family continues to provide cost effective innovative solutions while maintaining product compatibility and long term supporting strategy.

6 References

- Freescale Data Sheet: MCIMX35 “MCIMX35 Datasheet”
- Freescale Application Note: MCIMX35RM “MCIMX35 Multimedia Applications Processor Reference Manual”
- i.MX35 Board Initialization and Memory Mapping Using the Linux Target Image Builder (LTIB)
- Cypress S29GL-S Data Sheet

Document History Page

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**	–	–	01/12/2011	Initial version
*A	–	–	05/19/2011	Updated for latest S29GL-S data sheet
*B	4981031	MSWI	10/22/2015	Updated in Cypress template
*C	5827529	AESATMP8	07/21/2017	Updated logo and Copyright.

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