Cypress Roadmap: USB

Q4 2018
## USB Portfolio

<table>
<thead>
<tr>
<th>Device</th>
<th>Hub</th>
<th>Bridge</th>
<th>Storage</th>
<th>Type-C</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYUSB301x</td>
<td>CYUSB33xx</td>
<td>CYUSB306x</td>
<td>CYUSB303x</td>
<td>CYPD1xxx</td>
</tr>
<tr>
<td>FX3</td>
<td>HX3</td>
<td>CX3</td>
<td>FX3S</td>
<td>CCG1</td>
</tr>
<tr>
<td>32-Bit Bus to USB 3.1 Gen 1 ARM9, 512KB RAM</td>
<td>USB 3.1 Gen 1, Shared Link™, BC 1.2™, Ghost Charge™</td>
<td>CSI to USB 3.1 Gen 1</td>
<td>16-Bit Bus to USB 3.1 Gen 1 RAID®, Dual SDXC/eMMC®</td>
<td>USB Type-C Port Controller 1 PD Port, Profilets, 100 W</td>
</tr>
<tr>
<td>FX3Gen2</td>
<td>CYUSB333x</td>
<td>CYUSB385x</td>
<td>CYUSB302x</td>
<td>CYPD2xxx</td>
</tr>
<tr>
<td>USB 3.1 Gen 2 Peripheral Controller Contact Sales</td>
<td>4 Ports: 1 Type-C, 3 Type-A</td>
<td>USB 3.1 Gen 1 to GigE</td>
<td>SD3</td>
<td>CCG2</td>
</tr>
<tr>
<td></td>
<td>HX3C</td>
<td>Energy Efficient Ethernet</td>
<td></td>
<td>USB Type-C Cable Controller 1 PD Port, Termination, ESD</td>
</tr>
<tr>
<td>CY7C6801x/53</td>
<td>CYUSB43xx</td>
<td>CYWB0x16xBB</td>
<td>CYPD3xxx</td>
<td>CYPD317x</td>
</tr>
<tr>
<td>FX2LP</td>
<td>HX3PD</td>
<td>Bay™, Astoria™</td>
<td>CCG3</td>
<td>CCG3PA</td>
</tr>
<tr>
<td>16-Bit Bus to USB 2.0 8051, 16KB RAM</td>
<td>USB 3.1 Gen 2 Type-C Hub 7 Ports, PD, Board, 10 Gbps</td>
<td>16-Bit Bus to USB 2.0 8051</td>
<td>Dual SD/eMMC</td>
<td>USB Type-C Port Controller 30V, PPS, QC4, 64KB Flash</td>
</tr>
<tr>
<td>CYUSB331x</td>
<td>CY7C6556x4</td>
<td>CYWB016xBB</td>
<td>CYPD4xxx</td>
<td>CYPD277x</td>
</tr>
<tr>
<td>FX2G</td>
<td>HX2VL</td>
<td>Bay™</td>
<td>CCG4/CCG4M</td>
<td>USB Type-C EMCA Controller PD 3.0, Vbus short protection</td>
</tr>
<tr>
<td>32-Bit Bus to USB 2.0 ARM9 512KB RAM</td>
<td>4 Ports, 4 Transaction Protocols</td>
<td>HS USB OTG</td>
<td>USB Type-C Port Controller 2 PD Ports, 128KB Flash, Mux</td>
<td>Secondary-side Controller Contact Sales</td>
</tr>
<tr>
<td>CY7C6803x/3xx</td>
<td>CY7C655x1</td>
<td>CYWB016xBB</td>
<td>CYPD5xxx</td>
<td>CYPAP1xx</td>
</tr>
<tr>
<td>enCoRe™ III/IV/MIC MCU, GPIOs SPI, Flash</td>
<td>HX2LP</td>
<td>Bay™</td>
<td>CCG5/CCG5C</td>
<td>USB Type-C Port Controller 2 PD Ports, Vbus short protection</td>
</tr>
<tr>
<td>CY7C65210/7</td>
<td>CY7C6521x</td>
<td>CYWB016xBB</td>
<td>CYPD612x</td>
<td>CYPAP1xx</td>
</tr>
<tr>
<td>USB Billboard ARM Cortex M0 1 or 2 UART/SPi/VC channels</td>
<td>USB-Serial UART/SPi/VC to USB 2 Channels, CapSense®</td>
<td>Bay™</td>
<td>CC06</td>
<td>USB Type-C Port Controller Contact Sales</td>
</tr>
<tr>
<td>SL811HS</td>
<td>USB-to-UART (Gen 2) 3 Mbps, 8 GPIOs</td>
<td></td>
<td></td>
<td>Primary-side Start-up Controller Contact Sales</td>
</tr>
<tr>
<td>CY7C67300/200</td>
<td>CY7C6521x</td>
<td>USB Host/EZ-OTG™</td>
<td>CYPD612x</td>
<td>CYC1xxx</td>
</tr>
<tr>
<td>EZ-Host/EZ-OTG™ 4/2 Ports, FS USB OTG GPIOs</td>
<td>USB-to-UART (Gen 2) 3 Mbps, 8 GPIOs</td>
<td></td>
<td>CC06</td>
<td>USB Type-C Port Controller Contact Sales</td>
</tr>
<tr>
<td></td>
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</tbody>
</table>

**Notes:**
- **1**: Simultaneous USB 2.0 and SuperSpeed traffic on the same port
- **2**: Battery Charging specification v1.2
- **3**: Enables USB charging without host connection
- **4**: Camera Serial Interface v2.0
- **5**: Redundant array of independent disks
- **6**: SD extended capacity
- **7**: Embedded Multimedia Card

**Status Availability:**
- **Concept:**
- **Development:**
- **Sampling:**
- **Production:**

**Type-C products apply to any USB speed**
EZ-PD CMG1
USB Type-C Passive EMCA Controller

Applications
USB-C EMCA

Features
- USB-C PD Controller, PD 3.0 Transceiver
- \( V_{\text{BUS}} \)-to-CC Short Protection
- \( V_{\text{BUS}} \)-to-\( V_{\text{CONN}} \) Short Protection
- Power from \( V_{\text{CONN}} \) range 3.0 to 5.5-V
- Termination Resistor \( R_A \)
- Supports \( R_A \) Weakening to Reduce Power Consumption
- Configurable 32-byte Storage for Configuration Over Type-C Interface
- Integrated oscillator eliminating the need for external clock
- Power Operation
  - 2.7-V to 5.5-V operation (\( V_{\text{CONN}} \) pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, \( V_{\text{CONN}} \) Pins
  - \( \pm 6 \)-kV contact, \( \pm 15 \)-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm\(^2\))
  - Supports industrial temperature range (-40°C to +85°C)

Collateral
Preliminary Datasheet: CMG1 Datasheet

CMG1: USB Type-C Passive EMCA Controller

USB PD Subsystem
- \( V_{\text{BUS}} \)-to-CC Short Protection
- \( V_{\text{BUS}} \)-to-\( V_{\text{CONN}} \) Short Protection, \( R_A \)
- \( V_{\text{BUS}} \)-to-\( V_{\text{CONN}} \) Short Protection, \( R_A \)

EMCA Protocol Engine
- USB PD & Type-C PHY

Storage
- 32-Byte Storage for Configuration

System Resources
- Oscillator
- VREF
- IREF

Availability
- Samples: Now
- Production: Q4 2018
CCG6
Single-Port USB Type-C and PD Port Controller

Applications
Thunderbolt / non-Thunderbolt Desktop, Notebook

Features
- Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode and USB platforms
- $V_{BUS}$ to CC/SBU short protection
- Integrated high-voltage 20V-regulator to power CCG6
- Integrated Analog Blocks
  2x1 SBU analog mux, 2x2 USB analog mux
  Configurable $V_{BUS}$ over-voltage protection and over-current protection
  High-side current sense amplifier across 5Mohms
  Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- Integrated Digital Blocks
  Two timers, counters and pulse-width modulators, 17x GPIOs
  Four SCBs for configurable master/slave I2C, SPI or UART
- ARM® Cortex®-M0 with MCU Subsystem and 128KB flash
- Power System
  High-voltage (4 - 21.5 V, 26 V Max) $V_{BUS}$ voltage inputs
  2x $V_{CONN}$ FETs supporting up to 500 mA, Supports Dead Battery mode operation
  Integrated PFET gate drivers and Slew Rate Control
  $V_{BUS}$ Over Voltage Protection and Reverse Current Protection on provider path
- Packages
  96 BGA (6x6 mm)

Collateral
Preliminary Datasheet: Contact Sales

Availability
Sampling: Now, Production: Q1 2019

1 Serial communication block configurable as UART, SPI or I2C
2 Analog feedback control circuit to regulate $V_{BUS}$
3 Circuit to measure the current flowing on the $V_{BUS}$
4 Timer/counter/pulse-width modulator block
5 Termination resistors: $R_P$ as a DFP, $R_D$ as a UFP
**EZ-USB HX3PD**

**USB 3.1 Gen 2 Type-C Hub with Power Delivery**

**Applications**
- Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

**Features**
- **USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD**
  - Upstream (US) ports:
    - 10 Gbps; Type-A or Type-C plus PD (UFP)
  - Downstream (DS) ports:
    - 7 ports: 5x 10 Gbps, 2x 480 Mbps
    - 3 Type-C ports: 1 PD port (DFP), 2 Type-C only
- **Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction**
  - Integrated termination resistors (R_T and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\), USB Type-C Bridge Controller
  - Integrated VCONN FETs and ADC for overvoltage and overcurrent protection
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- **Ghost Charge™**: Charging DS without US connection
- **Dock Management Controller for secured firmware download**
  - Firmware upgradable over USB
- **System-Level ESD on Configuration Channel (CC) Pins**: 8 kV Contact, 15 kV Air
- **Package**: 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

**Datasheet**:
- HX3PD Datasheet

**Kit**:
- HX3PD Evaluation Kit

\(1\) Termination resistors: \(R_T\) read as a DFP, \(R_D\) as a UFP

\(2\) A USB Device controller that is used to implement the USB Billboard Device Class

**Routing Logic**
- Translates the USB 3.1 Gen 2 signals to USB 2.0 signals
- Provides signal integrity and EMI/RFI protection

**Collateral**

**Availability**

**Samples**: Now

**Production**: Q1 2019

1. Termination resistors: \(R_T\) read as a DFP, \(R_D\) as a UFP
2. A USB Device controller that is used to implement the USB Billboard Device Class
3. Transaction Translator
**EZ-PD CCG2**
**USB Type-C and PD Port Controller**

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**Applications**
USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

**Features**

- **32-bit MCU Subsystem**
  - 48-MHz ARM® Cortex®-M0 CPU with 32KB Flash and 4KB SRAM

- **Integrated Digital Blocks**
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs¹ configurable to I²C, SPI or UART modes

- **Type-C Support**
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (R_P, R_D, R_A)²

- **Power Delivery (PD) Support**
  - Standard power profiles

- **Low-Power Operation**
  - Two independent V_CONN rails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation; Sleep: 2.0 mA; Deep Sleep: 2.5 µA

- **System-Level ESD on CC and VDD Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C

- **Packages**
  - 20-ball CSP (3.3 mm²) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm²) with 0.55-mm pin pitch

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**Collateral**

- **Datasheet:** [CCG2 Datasheet](#)
- **Reference Design Kit:** [CCG2 RDK](#)
- **Evaluation Kit:** [CCG3 EVK](#)

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**Availability**

**Production:** Now

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¹ Serial communication block configurable as UART, SPI or I²C
² Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA
### EZ-PD CCG3
USB Type-C and PD Port Controller

#### Applications
- Accessories and power adapters

#### Features
- One Type-C Port with Integrated Transceiver
  - Alternate Modes\(^1\), Crypto Engine\(^2\) for USB Authentication\(^3\)
- Power Delivery (PD) Support for Standard Power Profiles
- Integrated Digital Blocks for \(V_{BUS}\) Power and MUX Interface
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave \(\text{i}^{2}\text{C}\), SPI or UART
  - USB Billboard Controller\(^4\) with Billboard Device Class\(^5\) support
- Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - 21.5-V OVP and OCP; 2:2 cross-bar switch
- 32-bit ARM® Cortex®-M0 CPU with MCU Subsystem
  - 2x64KB Flash for fail-safe updates over CC, \(\text{i}^{2}\text{C}\) or USB interfaces
- Low-Power Operation
  - 2x \(V_{BUS}\) Gate Drivers\(^6\), for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) \(V_{BUS}\) voltage inputs
  - Sleep: 2.0 mA; Deep Sleep: 2.5 \(\mu\)A with wake-on-\(\text{i}^{2}\text{C}\) or wake-on-CC
- System-Level ESD on \(\text{CC}/V_{CONN}\), \(V_{BUS}\), and SBU Pins
  - \(\pm 8\)-kV Contact, \(\pm 15\)-kV Air Gap IEC61000-4-2 Level 4C
- Packages
  - 42-ball (8.38 mm\(^2\)) CSP, 40-pin (36 mm\(^2\)) QFN and 32-pin (25 mm\(^2\)) QFN

#### Collateral
**Datasheet:** [CCG3 Datasheet]

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### CCG3: USB Type-C Port Controller

#### MCU Subsystem
- **Arm Cortex-M0**
- 48 MHz
- Flash (64KB)
- SRAM (8KB)
- Advanced High-Performance Bus (AHB)

#### System Resources
- Full-Speed USB Billboard Controller
- Baseband PHY
- 21.5-V Regulator
- 2x \(V_{CONN}\) FETs
- OCP
- 2x 20V \(V_{BUS}\) FET Gate Drivers

#### USB PD Subsystem
- CC
- 2x 6-bit SAR ADC
- 2x 24x GPIO Ports

#### Integrated Digital Blocks
- 4x TCPWM
- 4x SCB (\(\text{i}^{2}\text{C}, \text{SPI}, \text{UART}\))
- Crypto Engine

#### I/O Subsystem
- Programmable I/O Matrix

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### Availability
**Production:** Now

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1. Mode of operation in which the data lines are repurposed to transmit non-USB data
2. The encryption hardware and software required to implement USB Authentication
3. A specification that defines the method for a USB Device to communicate the supported Alternate Modes
4. Circuits to control the gates of external power Field-Effect Transistors (FETs) on \(V_{BUS}\) (5–20 V)
5. A USB-IF specification that defines the authentication protocol for Type-C accessories
6. A USB Device controller that informs the USB Host of the supported Alternate Modes
7. Termination resistors: \(R_{P}\) read as a DFP, \(R_{D}\) as a UFP, \(R_{A}\) as an EMCA
EZ-PD CCG4/4M
Dual-Port USB Type-C and PD Port Controller

Applications
Notebooks, tablets, monitors, docking stations

Features
- Integrated USB Type-C Transceivers Support Two Type-C Ports
  - Integrated 2x 1-W VCONN FETs and 2x FET control signals, per port programmable Rp¹ and removable Rp, and Rp² terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- Increased Flash Enables Fail-Safe Bootup
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- Integrated Digital Blocks for Inter-Chip Communications
  - Four serial communication blocks (SCBs) master or slave configurable to I2C, SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- Low-Power Operation
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA;
    Deep Sleep: 2.5 µA with wake-on-I²C or wake-on-configuration channel (CC)
- System-Level ESD on CC Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- 32-bit ARM® Cortex®-M0 CPU with MCU Subsystem
  - 128KB Flash, upgradable over CC lines or I²C interface
- Packages
  - 40-pin QFN, 96-ball BGA (CCG4M)

Collateral
- Datasheet: CCG4 Datasheet

Availability
Production: Now

¹ Termination resistor read as a DFP
² Termination resistor read as a UFP
**EZ-PD CCG3PA**

**USB Type-C and PD Port Controller**

### Applications
- Power adapters, chargers, power banks

### Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable VBUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for VBUS control
  - Low side current sense² capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)
- **32-bit ARM Cortex®-M0 CPU with 64KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) VBUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / VCONN, VBUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 24-QFN (16 mm²), 16-SOIC (60 mm²)

### Collateral
- Datasheet: Contact Sales

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¹ Analog feedback voltage control circuit to control VBUS
² Circuit to measure the current flowing on the VBUS
³ Adaptive Fast Charging
⁴ Termination resistors: R_P read as a DFP, R_D as a UFP, R_A as an EMCA

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**Availability**

- Production: Now

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**CCG3PA: USB Type-C Port Controller**

- **MCU Subsystem**
  - arm Cortex®-M0 48 MHz
- **Integrated Digital Blocks**
  - 4x TCPWM
  - 2x SCB (I²C, SPI, UART)
- **I/O Subsystem**
  - Programmable I/O Matrix
  - 14x GPIO Ports
- **USB PD Subsystem**
  - Baseband PHY
  - Baseband MAC
  - 30-V Regulator
  - 2x VCONN FETs
  - OCP and VOP
  - Low-Side Current Sense
- **System Resources**
  - 1x 9-bit SAR ADC
  - SRAM (4KB)
  - Flash (64KB)
  - Programmable I/O Matrix

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**Notes:**
- C handmade in the USA
EZ-PD CCG3PA2
USB Type-C and PD Port Controller

Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable VBUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for VBUS control
  - Low side current sense² capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)
- **32-bit ARM® Cortex®-M0 CPU with 128KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) VBUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / VCONN, VBUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm²), 30-ball CSP (7.5 mm²)

Collateral
- Datasheet: [Contact Sales]

Availability
- Production: Now

¹ Analog feedback voltage control circuit to control VBUS
² Circuit to measure the current flowing on the VBUS
³ Adaptive Fast Charging
⁴ Termination resistors: R_P as a DFP, R_D as a UFP, R_A as an EMCA
## EZ-PD CCG3PA2
### USB Type-C and PD Port Controller

#### Applications
- Power adapters, chargers, power banks

#### Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART
- **Integrated Analog**
  - Configurable $V_{BUS}$ overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier\(^1\) with analog out for $V_{BUS}$ control
  - Low side current sense\(^2\) capable of detecting 100mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC\(^3\))
- **32-bit ARM\(^{®}\) Cortex\(^{®}-\)M0 CPU with 64KB Flash**
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) $V_{BUS}$ voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC
- **System-Level ESD on CC / $V_{CONN}$ $V_{BUS}$ and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Packages**
  - 32-QFN (25 mm\(^2\)), 30-ball CSP (7.5 mm\(^2\))

#### Collateral
- **Datasheet:** [Contact Sales](#)

#### Availability
- **Production:** Now

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\(^1\) Analog feedback voltage control circuit to control $V_{BUS}$
\(^2\) Circuit to measure the current flowing on the $V_{BUS}$
\(^3\) Adaptive Fast Charging
\(^4\) Termination resistors: $R_p$ read as a DFP, $R_o$ as a UFP, $R_a$ as an EMCA
EZ-PD CCG5
Dual-Port USB Type-C and PD Port Controller

**Applications**
- Notebooks, docks, Thunderbolt devices

**Features**
- Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI\(^1\)-compliant Interface with WHQL\(^2\)-certified driver
  - Support for UEFI\(^3\) driver with Microsoft capsule firmware download
- Integrated Analog
  - Integrated high-voltage LDO and 4x \(V_{\text{CONN}}\) FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC\(^4\))
  - Integrated Type-C termination resistors (\(R_p\), \(R_o\) \(R_{\text{DB}}\))\(^5\)
  - 25-V tolerance on CC1/2 and SBU pins
- ARM\(^®\) Cortex\(^®\)-M0 CPU with 128KB Flash and 12KB SRAM
  - 4x serial communication blocks (SCB) - I\(^2\)C, SPI or UART
  - Firmware upgradable over SWD/I\(^2\)C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2µs response time; Integrated \(V_{\text{BUS}}/V_{\text{CONN}}\) overcurrent protection (OCP)
- System-Level ESD on CC/\(V_{\text{CONN}}\), \(V_{\text{BUS}}\), and SBU Pins
  - \(\pm8\)-kV Contact, \(\pm15\)-kV Air Discharge IEC61000-4-2 Level 4C
- Packages
  - 2-Port in 96-BGA (6 mm\(^2\)), 1-Port in 40-QFN (6 mm\(^2\))

**Collateral**
- **Datasheet:** [Contact Sales](#)

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\(^1\) USB Type-C Connector System Software Interface
\(^2\) Unified Extensible Firmware Interface
\(^3\) Termination resistors: \(R_p\) read as a DFP, \(R_o\) as a UFP, \(R_{\text{DB}}\) as UFP in Dead-Battery scenario
\(^4\) Windows Hardware Quality Labs
\(^5\) Adaptive Fast Charging

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**CCG5: USB Type-C Port Controller**

<table>
<thead>
<tr>
<th>MCU Subsystem</th>
<th>Integrated Digital Blocks</th>
<th>I/O Subsystem</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cortex(^®)-M0</strong> 48 MHz</td>
<td>2x TCPWM</td>
<td><strong>V_{\text{BUS}} / V_{\text{CONN}} OCP</strong></td>
</tr>
<tr>
<td><strong>Flash</strong> (128KB)</td>
<td>SCB (I(^2)C, SPI, UART)</td>
<td><strong>V_{\text{CONN}}</strong></td>
</tr>
<tr>
<td><strong>SRAM</strong> (12KB)</td>
<td>SCB (I(^2)C, SPI, UART)</td>
<td><strong>Hi-Voltage LDO (21.5V)</strong></td>
</tr>
<tr>
<td><strong>Advanced High-Performance Bus (AHB)</strong></td>
<td>SCB (I(^2)C, SPI, UART)</td>
<td><strong>4x 8-bit SAR ADC</strong></td>
</tr>
<tr>
<td><strong>Programmable I/O Matrix</strong></td>
<td>2x V_{\text{CONN}} FETs</td>
<td><strong>2x PFETs Gate Driver</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>System Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x SBU Analog Pass through / Mux</td>
</tr>
<tr>
<td>2x2 USB Analog Switch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>USB PD Subsystem x2</strong></th>
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<tbody>
<tr>
<td><strong>Baseband MAC</strong></td>
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<tr>
<td><strong>Baseband PHY</strong></td>
</tr>
<tr>
<td><strong>Hi-Voltage LDO (21.5V)</strong></td>
</tr>
<tr>
<td>4x 8-bit SAR ADC</td>
</tr>
<tr>
<td><strong>V_{\text{BUS}} OVP</strong></td>
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</tbody>
</table>

**Availability**
- **Production:** Now
EZ-USB FX3
USB 3.1 Gen 1 Peripheral Controller

Applications
Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras, document and fingerprint scanners, videoconferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core
  - 512KB of embedded SRAM for code space and buffers
- 32-bit, 100-MHz, flexible GPIF II Interface
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
Datasheet: [FX3 Datasheet](#)
Development Kit: [FX3 SuperSpeed Explorer Kit](#)
Software Development Kit: [EZ-USB FX3 SDK](#)

Availability
Production: Now

USB 3.1 Gen 1 Host

FX3: USB 3.1 Gen 1 Peripheral Controller

- JTAG
- 512KB RAM
- Image Sensor, FPGA or ASIC
- USB 3.1 Gen 1
- I²C
- UART
- SPI
- GPIO
- 32-bit, 100-MHz, flexible GPIF II Interface
- Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
- Unused I/O pins can be used as GPIOs
- 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)
**EZ-USB FX3S**

**USB 3.1 Gen 1 RAID¹-on-Chip**

### Applications

Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders and data logging devices

### Features

- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints

- **Fully Accessible 32-bit, 200-MHz ARM® 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers

- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs

- **Two SDXC², eMMC³ 4.4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations

- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input

- **Packages**
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

### Collateral

- **Datasheet:** [FX3S Datasheet](#)
- **Kit:** [FX3S RAID¹-on-Chip Boot Disk Kit](#)
- **Software Development Kit:** [EZ-USB FX3 SDK](#)

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¹ Redundant array of independent disks
² SD extended capacity
³ Embedded Multimedia Card

**Availability**

**Production:** Now

**FX3S: RAID¹-on-Chip**

- 512KB RAM (RAID¹ Firmware)
- SD Card, eMMC³ NAND, SDIO Device
- USB 3.1 Gen 1 Host

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**Cypress Confidential Roadmap: USB**
EZ-USB CX3
MIPI\textsuperscript{1} CSI-2 to USB 3.1 Gen 1 Bridge

Applications
Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz ARM\textsuperscript{®} 926EJ core
  - 512KB of embedded SRAM for code space and buffers
- Four-Lane MIPI\textsuperscript{1} Camera Serial Interface v2.0 (CSI-2) Input
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I\textsuperscript{2}C, UART, SPI and 12 GPIOs
- Supports Industry-Standard Video Data Formats
  - RAW8/10/12/14\textsuperscript{2}, YUV422/444\textsuperscript{3}, RGB888/666/565\textsuperscript{4}
- Supports Uncompressed Streaming Video
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- Packages
  - 121-ball BGA (10 x 10 x 1.7 mm)

Collateral
Datasheet: [CX3 Datasheet](#)
Reference Design Kit: [CX3 Reference Design Kit](#)
Software Development Kit: [EZ-USB FX3 SDK](#)

1 Mobile Industry Processor Interface
2 Video format for raw video data
3 Video format for luminance and chrominance components
4 Video format for red, green and blue pixel components

Availability
Production: Now

15 Cypress Confidential Roadmap: USB
EZ-USB GX3
USB 3.1 Gen 1 to GigE¹ Bridge

Applications
USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs and other embedded systems

Features
- One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC²
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- IEEE 802.3az³ Support for Low-Power Idle State
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN⁴ features
- Supports Optional EEPROM to Store USB Descriptors
  - Integrates on-chip power-on-reset (POR) circuitry
- Packages
  - 68-QFN (8 x 8 x 0.85 mm)

Collateral
Datasheet: GX3 Datasheet
Reference Design Kit: GX3 Reference Design Kit
Software & Drivers: GX3 Drivers

Availability
Production: Now

¹ Gigabit Ethernet
² Media access controller that provides the address to an Ethernet node
³ A new-energy efficient Ethernet standard
⁴ An Ethernet standard that allows a computer to be turned on by a network message
EZ-USB HX3
USB 3.1 Gen 1 Hub

Applications
Docking stations for notebook PCs and tablets, PC motherboards, servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

Features
- USB 3.1 Gen 1-Compliant Four-Port Hub Controller
  - USB-IF certified (Test ID: 330000047)
  - WHQL certified for Windows 7, Windows 8, Windows 8.1
- Shared Link™
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- Ghost Charge™
  - Enables USB charging while the hub is disconnected from a USB Host
- Charging Standard support
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- Programming of External EEPROM via USB
- Configurable USB SS and USB 2.0 PHY (drives 11” trace)
- Packages
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Collateral
Datasheet: HX3 Datasheet
Kit: CY4609, CY4603, CY4613
Configuration Utility: Blaster Plus¹
App Notes: HX3 Hardware Design Guide (AN91378)

Availability
Production: Now

¹ A Cypress GUI-based PC application for setting HX3 configuration parameters
² Transaction translator
EZ-USB HX3C
USB 3.1 Gen 1 Type-C PD Hub

Applications
USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features
- USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- Integrated Type-C Transceivers, Supporting Two Type-C Ports
  - Integrated termination resistors ($R_P$ and $R_D$)\(^1\)
  - Integrated USB Billboard Controller\(^2\)
- Charging Support
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- Ghost Charge™
  - Charging DS without US connection
- Firmware Upgradable Over USB
- System-Level ESD on Configuration Channel (CC) Pins
  - 8 kV Contact, 15 kV Air
- Configurable USB SS and USB 2.0 PHY (drives 11" trace)
- Packages
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral
Datasheet: HX3C Datasheet
Reference Design: HX3C Type-C Monitor/Dock Reference Design

HX3C: USB 3.1 Gen 1 Type-C PD Hub

Availability
Production: Now

\(^1\) Termination resistors: $R_P$ read as a DFP, $R_D$ as a UFP
\(^2\) A USB Device controller that is used to implement the USB Billboard Device Class
\(^3\) Transaction Translator