## USB Portfolio

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### Status

* NEW: Q1 2020
* Q4 2019
* Q3 2019
* Q2 2019
* Q1 2019
* Q4 2018
* Q3 2018
* Q2 2018

### Availability

* Production
* Sampling
* Development
* Concept

### USB Products

1. Simultaneous USB 2.0 and SuperSpeed traffic on the same port
2. Battery Charging specification v1.2
3. Enables USB charging without host connection
4. Camera Serial Interface v2.0
5. Redundant array of independent disks
6. SD extended capacity
7. Embedded Multimedia Card

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Cypress Confidential Roadmap: USB
EZ-PD ACG1F
Single Port Type-C controller with BC1.2, Load Switch

Applications
Desksops, Notebooks

Features
- Type-C 1.2 Controller
- VBUS to CC/SBU short protection
- Integrated Analog Blocks
  Configurable VBUS over-voltage protection and over-current protection
  High-side current sense amplifier across 5mohms
  Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
  VCONN FET per CC with VCONN OCP limit of up to 550 mA
- Integrated Digital Blocks
  4x GPIOs
  One SCB\(^1\) for configurable master/slave I2C, SPI, or UART
- Arm\(^\circledast\) Cortex\(^\circledast\)-M0 with MCU Subsystem and 16KB flash
- Power System
  Integrated 15-W provider load switch capable of 5 V, 3A
  VBUS over-voltage protection and Reverse Current Protection on provider path
- Packages
  24-QFN (4x4 mm)

Collateral
Datasheet: [ACG1F Datasheet](#)

Availability
Sampling: Now  
Production: Q4 2019

Datasheet: [ACG1F Datasheet](#)
**PAG1S**

**USB-C Power Delivery Secondary-Side Controller**

**Applications**
- USB PD chargers, power adapters

**Features**
- PPS/PD3.0/QC4.0 integrated flyback controller for mobile chargers
- Works with both primary side-controlled and secondary-side-controlled flyback designs
- Integrated secondary-side regulation, synchronous rectifier, and charging port controller offering a single-chip secondary-side controller
- Supports Quasi-Resonant (QR)/Critical Conduction (CrCM), valley switching, discontinuous conduction (DCM), and Burst Modes
- Integrated digital blocks
  - One timer/counter/pulse-width modulator (TCPWM) block, 6x GPIOs
- Integrated analog blocks
  - Configurable $V_{BUS}$ overvoltage protection (OVP), overcurrent (OCP) protection, undervoltage protection (UVP), and short-circuit protection (SCP)
  - Integrated 2xVBUS discharge FETs and a NFET gate driver to drive the load switch
  - Low-side current sense capable of detecting 100-mA change
  - One legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC)
- Low-Power Operation
  - High-voltage (3–30 V, 30-V maximum) $V_{BUS}$ voltage inputs
  - No load power consumption of less than 20 mW
- Package
  - 24 QFN (16 mm$^2$)

**Collateral**
- Preliminary Datasheet: [PAG1S Datasheet](#)

**Availability**
- Sampling: Now

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1. Circuit to measure the current flowing on the $V_{BUS}$
2. Adaptive Fast Charging
3. Termination resistors: $R_P$ read as a DFP, $R_D$ as a UFP
4. Termination resistors: $R_P$, $R_D$
PAG1P
USB-C Power Delivery Primary Start Up Controller

Applications
USB PD chargers, power adapters

Features
- Works across universal AC mains input 85 VAC to 265 VAC
- Operates with PWM inputs from a secondary-side controller
- Low-side gate driver to drive primary FET (1-A Source)
- Soft-start with duty-cycle clamping
- Integrates high-voltage start-up and shunt regulator
- Line undervoltage and overvoltage protection
- Overcurrent protection against load short-circuit
- Operates over a temperature range of -40 ºC to 105 ºC
- Package
  - 10-pin SOIC (4.9 x 3.9 mm²)

Collateral
Preliminary Datasheet: PAG1S Datasheet

Availability
Sampling: Now  Production: Q4 2019
**EZ-USB HX3PD**

**USB 3.1 Gen 2 Type-C Hub with Power Delivery**

### Features

- **USB 3.1 Gen 2-Compliant Hub Controller with Type-C and PD**
  - Upstream (US) ports:
    - 10 Gbps; Type-A or Type-C plus PD (UFP)
  - Downstream (DS) ports:
    - 7 ports: 5x 10 Gbps, 2x 480 Mbps
    - 3 Type-C ports: 1 PD port (DFP), 2 Type-C only
- **Integrated Type-C Transceivers and Dual-PHY for Type-C plug orientation correction**
  - Integrated termination resistors (R_P and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\), USB Type-C Bridge Controller
  - Integrated VCONN FETs and ADC for overvoltage and overcurrent protection
- **Charging Support**
  - USB PD, BC v1.2, Apple Charging Standard, QC 4.0, Samsung AFC
  - USB PD policy engine configures power profiles dynamically
- **Ghost Charge™**: Charging DS without US connection
- **Dock Management Controller** for secured firmware download
  - Firmware upgradable over USB
- **System-Level ESD on Configuration Channel (CC) Pins**: 8 kV Contact, 15 kV Air
- **Package**: 192-ball BGA (12 mm x 12 mm x 1 mm, 0.8-mm ball-pitch)

### Applications

- Notebook/tablet docking stations, monitor docks, multi-function USB Type-C peripherals

### Collateral

- **Datasheet**: [HX3PD Datasheet](#)
- **Kit**: [HX3PD Evaluation Kit](#)

### Availability

- **Samples**: Now
- **Production**: Q1 2020

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1. Termination resistors: R_P read as a DFP, R_D as a UFP
2. A USB Device controller that is used to implement the USB Billboard Device Class
3. Transaction Translator informs the USB Host of the supported Alternate Modes as well as any failures
EZ-PD BCR
USB Type-C Power-Sink Port Controller

Applications
Portable electronics – cameras, camcorders, smart speakers, toys, gaming, shavers, powered tools and any battery-powered devices.
Industrial – LED lighting, scanner, printer, drones, IoT
Any electronics device consuming less than 100W

Features
- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power the BCR controller
  - One serial communication blocks (SCB) for slave I2C
- **Integrated Analog**
  - $V_{BUS}$ overvoltage (OVP) and undervoltage (UVP) protection
  - Fault detection for PDO mismatch
  - Slow rate-controlled PMOS FET gate driver
  - Minimum 25-V–tolerant CC pins and FET control pins
- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) $V_{BUS}$ voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I2C or CC
- **System-Level ESD on CC, and $V_{BUS}$**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- **Package**
  - 24-QFN (16 mm²), supporting extended Industrial temp (-40 °C to 105 °C)

Collateral
- **Datasheet**: CY3177 Datasheet
- **Evaluation Kit**: CY4533 Kit
- **Product Brochure**: EZ-PD Barrel Connector Replacement Product Overview

1 Analog feedback voltage control circuit to control $V_{BUS}$
2 Circuit to measure the current flowing on the $V_{BUS}$
3 Termination resistors: $R_D$ as a UFP, $R_{DB}$ as a UFP supporting dead battery

Availability
Production: Now

EZ-PD BCR: USB Type-C Power-Sink Port Controller

I/O Subsystem
- CC
- 1x SCB (I2C)
- Fault Detection

USB PD Subsystem
- Baseband MAC
- Baseband PHY
- 30-V Regulator
- Integrated Resistors ($R_D, R_{DB}$)
- OVP and UVP
- 1x 9-bit SAR ADC
- VBus-CC Short Protection
- VBus Discharge

Production: Now
EZ-PD CCG6
Single-Port USB Type-C Port Controller With PD

Applications
Thunderbolt / USB-C Notebook, Desktop PCs

Features
- USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode and USB platforms
- \( V_{BUS} \) to CC/SBU short protection
- Integrated high-voltage 20V-regulator to power CCG6
- Integrated Analog Blocks
  1x SBU analog mux, 2x2 USB analog mux
  Configurable \( V_{BUS} \) over-voltage protection and over-current protection
  High-side current sense amplifier across 5 mΩ
  Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- Integrated Digital Blocks
  Two timers, counters, and pulse-width modulators, 17x GPIOs
  Four SCBs\(^1\) for configurable master/slave I2C, SPI, or UART
- Arm® Cortex®-M0 with MCU Subsystem and 128KB flash
- Power System
  High-voltage (4 - 21.5 V, 26 V Max) \( V_{BUS} \) voltage inputs
  2x \( V_{CONN} \) FETs supporting up to 500 mA, Supports Dead Battery mode operation
  Integrated PFET gate drivers and Slew Rate Control
  \( V_{BUS} \) over-voltage protection and Reverse Current Protection on provider path
- Packages
  40 QFN (6x6 mm)

Collateral
Datasheet: CCG6 Datasheet

Availability
Production: Now

\(^1\) Serial communication block configurable as UART, SPI or PC
# EZ-PD CCG6F

## Single-Port USB Type-C Port Controller With PD

### Applications

Thunderbolt / USB-C Notebook, Desktop PCs

### Features

- **USB Type-C/Power Delivery 3.0 transceiver and TBT, DP Alt Mode, and USB platforms**
- 
- **V\textsubscript{BUS} to CC/SBU short protection**
- **Integrated high-voltage 20V-regulator to power CCG6**
- **Integrated Analog Blocks**
  - 2x1 SBU analog mux, 2x2 USB analog mux
  - Configurable \( V\textsubscript{BUS} \) over-voltage protection and over-current protection
  - High-side current sense amplifier across 5 m\( \Omega \)
  - Legacy charge-detect block (BC v1.2, QC3.0, AFC, Apple Charging)
- **Integrated Digital Blocks**
  - Two timers, counters, and pulse-width modulators, 17x GPIOs
  - Four SCBs\(^1\) for configurable master/slave I2C, SPI, or UART
- **Arm\textsuperscript{®} Cortex\textsuperscript{®}-M0 with MCU Subsystem and 128KB flash**
- **Power System**
  - High-voltage (4 - 21.5 V, 26 V Max) \( V\textsubscript{BUS} \) voltage inputs
  - 2x \( V\textsubscript{CONN} \) FETs supporting up to 500 mA, Supports Dead Battery mode operation
  - Integrated PFETs for provider path
  - \( V\textsubscript{BUS} \) over-voltage protection and Reverse Current Protection on provider path
- **Packages**
  - 96 BGA (6x6 mm)

### Collateral

**Datasheet:** [CCG6F Datasheet](#)

1 Serial communication block configurable as UART, SPI or I2C

### Availability

**Production:** Now

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1. [CCG6F Datasheet](#)

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**Datasheet:** CCG6F Datasheet

1 Serial communication block configurable as UART, SPI or I2C
EZ-PD CMG1
USB Type-C Passive EMCA Controller

**Applications**
- USB-C EMCA

**Features**
- USB-C PD Controller, PD 3.0 Transceiver
- \( V_{BUS}\)-to-CC Short Protection
- \( V_{BUS}\)-to-\( V_{CONN}\) Short Protection
- Power from \( V_{CONN}\) range 3.0 to 5.5-V
- Termination Resistor \( R_A \)
- Supports \( R_A \) Weakening to Reduce Power Consumption
- Configurable 32-byte Storage for Configuration Over Type-C Interface
- Integrated oscillator eliminating the need for external clock
- **Power Operation**
  - 2.7-V to 5.5-V operation (\( V_{CONN}\) pin)
  - Active: 7.5 mA
  - Sleep: 1 mA
- System-Level ESD on CC, \( V_{CONN}\) Pins
  - ±8-kV contact, ±15-kV Air Gap IEC61000-4-2 level 4C
- Packages
  - 9-ball WLCSP (1.95 mm\(^2\))
  - Supports industrial temperature range (-40°C to +85°C)

**Collateral**
- Preliminary Datasheet: [CMG1 Datasheet](#)

**Availability**
- Production: Now

**CMG1: USB Type-C Passive EMCA Controller**
- **USB PD Subsystem**
  - \( V_{BUS}\)-to-CC Short Protection
- **Storage**
  - 32-Byte Storage for Configuration
- **System Resources**
  - Oscillator
  - Reset
  - VREF
  - IREF
- **EMCA Protocol Engine**
EZ-PD CCG3PA2
USB Type-C and PD Port Controller

**Applications**

Power adapters, chargers, power banks

**Features**

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART

- **Integrated Analog**
  - Configurable V_BUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for V_BUS control
  - Low side current sense² capable of detecting 100-mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)

- **32-bit Arm® Cortex®-M0 CPU with 128KB Flash**

- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_BUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC

- **System-Level ESD on CC / V_CONN, V_BUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C

- **Packages**
  - 32-QFN (25 mm²), 30-ball CSP (7.5 mm²)

**Collateral**

Datasheet: [Contact Sales](#)

**Availability**

Production: Now

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¹ Analog feedback voltage control circuit to control V_BUS
² Circuit to measure the current flowing on the V_BUS
³ Adaptive Fast Charging
⁴ Termination resistors: R_P as a DFP, R_D as a UFP, R_A as an EMCA

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**CCG3PA2: USB Type-C Port Controller**

**MCU Subsystem**

- arm Cortex®-M0
- 48 MHz
- 128KB Flash

**Integrated Digital Blocks**

- 4x TCPWM
- 2x SCB (I²C, SPI, UART)

**I/O Subsystem**

- Programmable I/O Matrix
- CC

**USB PD Subsystem**

- Baseband PHY
- 2x V_CONN FETs
- Low-Side Current Sense
- 2x Charge-Detect (BC v1.2, AC, QC, AFC)
- Integrated Resistors (R_P, R_D, R_A)

**System Resources**

- SRAM (8KB)
- Advanced High-Performance Bus (AHB)
- 14x GPIO Ports

---

**Flash**

(128KB)

**SRAM**

(8KB)

---

1 Cypress Confidential Roadmap: USB
EZ-PD CCG3PA
USB Type-C and PD Port Controller

Applications
Power adapters, chargers, power banks

Features

- **Integrated Type-C and Power Delivery (PD) Transceiver**
  - Integrated high-voltage 30-V–tolerant LDO to power CCG3PA
  - Four timers/counters/pulse-width modulators (TCPWMs), 12x GPIOs
  - Two serial communication blocks (SCBs) for configurable master/slave I²C, SPI or UART

- **Integrated Analog**
  - Configurable V_BUS overvoltage (OVP) and overcurrent (OCP) protection
  - Integrated error amplifier¹ with analog out for V_BUS control
  - Low side current sense² capable of detecting 100-mA change
  - Minimum 25-V–tolerant CC pins and FET control GPIOs
  - Two legacy charge-detect block (BC 1.2, Apple Charging 2.4A, QC 4.0 and Samsung AFC³)

- **32-bit Arm® Cortex®-M0 CPU with 64KB Flash**

- **Low-Power Operation**
  - High-voltage (5–30 V, 30 V maximum) V_BUS voltage inputs
  - Sleep: ~3.5 mA; Deep Sleep: 50 µA with wake-on-I²C or CC

- **System-Level ESD on CC / V_CONN, V_BUS, and SBU Pins**
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C

- **Packages**
  - 24-QFN (16 mm²), 16-SOIC (60 mm²)

Collateral

- **Datasheet:** CCG3PA Datasheet

Availability

- **Production:** Now

¹ Analog feedback voltage control circuit to control V_BUS
² Circuit to measure the current flowing on the V_BUS
³ Adaptive Fast Charging
⁴ Termination resistors: R_P as a DFP, R_D as a UFP, R_A as an EMCA
EZ-PD CCG5
Dual-Port USB Type-C and PD Port Controller

Applications
Notebooks, docks, Thunderbolt devices

Features
- Integrated Type-C Transceiver for Two Type-C USB PD 3.0-Compliant Ports
  - Support for Thunderbolt, DisplayPort (DP), HDMI Alt Mode and USB platforms
  - USCI\(^1\)-compliant Interface with WHQL\(^2\)-certified driver
  - Support for UEFI\(^3\) driver with Microsoft capsule firmware download
- Integrated Analog
  - Integrated high-voltage LDO and 4x \(V_{CONN}\) FETs supporting up to 500 mA
  - Integrated 2x2 USB analog switch; integrated SBU analog pass with high-voltage tolerance
  - Integrated 2x USB Charger Detect (BC 1.2, Apple Charging, QC 4.0 and Samsung AFC\(^4\))
  - Integrated Type-C termination resistors (\(R_P\), \(R_D\), \(R_{DB}\))\(^5\)
  - 25-V tolerance on CC1/2 and SBU pins
- Arm\(^\circledR\) Cortex\(^\circledR\)-M0 CPU with 128KB Flash and 12KB SRAM
  - 4x serial communication blocks (SCB) - I\(^2\)C, SPI or UART
  - Firmware upgradable over SWD/I\(^2\)C interfaces
  - Supports Dead Battery mode operation
  - Overvoltage protection (OVP) with 2µs response time; integrated \(V_{BUS}/V_{CONN}\) overcurrent protection (OCP)
- System-Level ESD on CC/V\(_{CONN}\), \(V_{BUS}\), and SBU Pins
  - \(\pm8\)-kV Contact, \(\pm15\)-kV Air Discharge IEC61000-4-4 Level 4C
- Packages
  - 2-Port in 96-BGA (6 mm\(^2\)), 1-Port in 40-QFN (6 mm\(^2\))

Collateral
Datasheet: [CCG5 Datasheet](#)

### CCG5: USB Type-C Port Controller

- **MCU Subsystem**
  - Arm Cortex-M0 48 MHz
  - Flash (128KB)
  - SRAM (12KB)

- **Integrated Digital Blocks**
  - 2x TCPWM
  - SCB (I\(^2\)C, SPI, UART)
  - SCB (I\(^2\)C, SPI, UART)

- **2x USB Analog Switch**
  - 2x2 USB Analog Switch

- **System Resources**
  - Baseband PHY
  - 2x2 SBU Analog
  - 2x SBU Analog
  - 2x V\(_{CONN}\) FETs
  - 4x 8-bit SAR ADC
  - 2x TCPWM

- **I/O Subsystem**
  - CC
  - V\(_{CONN}\)
  - V\(_{BUS}\)

- **USB PD Subsystem x2**
  - Baseband MAC
  - Hi-Voltage LDO (21.5V)
  - 2x V\(_{CONN}\) OCP
  - 2x PFETs Gate Driver

### Availability
Production: Now

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1 USB Type-C Connector System Software Interface
2 Unified Extensible Firmware Interface
3 Windows Hardware Quality Labs
4 Adaptive Fast Charging
5 Termination resistors: \(R_P\) read as a DFP, \(R_D\) as a UFP, \(R_{DB}\) as UFP in Dead-Battery scenario
EZ-PD CCG4/4M
Dual-Port USB Type-C and PD Port Controller

Features
- Integrated USB Type-C Transceivers Support Two Type-C Ports
  - Integrated 2x 1-W $V_{CONN}$ FETs and 2x FET control signals, per port programmable $R_p$\(^1\) and removable $R_p$ and $R_R$\(^2\) terminations
  - Supports dead battery mode operation
  - Integrated SuperSpeed USB/DisplayPort (DP) Mux (CCG4M)
- Increased Flash Enables Fail-Safe Bootup
  - Integrates 128KB Flash to store dual FW images for fail-safe boot
- Integrated Digital Blocks for Inter-Chip Communications
  - Four serial communication blocks (SCBs) master or slave configurable to I²C, SPI or UART
  - SCBs interconnect CCG4 with embedded controller, two alternate muxes and Thunderbolt controller (optional)
- Integrated Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - Four 8-bit SAR ADCs configurable for OVP and OCP
- Low-Power Operation
  - 2.7–V to 5.5-V operation and independent supply voltage for GPIO; Sleep: 2.0 mA; Deep Sleep: 2.5 μA with wake-on-I²C or wake-on-configuration channel (CC)
- System-Level ESD on CC Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- 32-bit Arm® Cortex®-M0 CPU with MCU Subsystem
  - 128KB Flash, upgradable over CC lines or I²C interface
- Packages
  - 40-pin QFN, 96-ball BGA (CCG4M)

Collateral
- Datasheet: [CCG4 Datasheet](#)

Availability
- Production: Now

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1 Termination resistor read as a DFP
2 Termination resistor read as a UFP

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Cypress Confidential Roadmap: USB
EZ-PD CCG3
USB Type-C and PD Port Controller

**Applications**
- Accessories and power adapters

**Features**
- One Type-C Port with Integrated Transceiver
  - Alternate Modes: for USB Authentication
- Power Delivery (PD) Support for Standard Power Profiles
- Integrated Digital Blocks for \( V_{BUS} \) Power and MUX Interface
  - 4 timers/counters/pulse-width modulators (TCPWM), 24x GPIOs
  - 4 serial communication blocks (SCBs) configurable as master/slave \( I^2C \), SPI or UART
  - USB Billboard Controller with Billboard Device Class support
- Integrated Analog Blocks for Overvoltage (OVP) and Overcurrent Protection (OCP)
  - 21.5-V OVP and OCP; 2.2 cross-bar switch
- 32-bit Arm® Cortex®-M0 CPU with MCU Subsystem
  - 2x64KB Flash for fail-safe updates over CC, \( I^2C \) or USB interfaces
- Low-Power Operation
  - 2x \( V_{BUS} \) Gate Drivers, for consumer and provider power paths
  - 2x high-voltage (5–21.5 V, 25 V, maximum) \( V_{BUS} \) voltage inputs
  - Sleep: 2.0 \( \mu A \); Deep Sleep: 2.5 \( \mu A \) with wake-on-\( I^2C \) or wake-on-CC
- System-Level ESD on CC/\( V_{CONN} \), \( V_{BUS} \), and SBU Pins
  - \( \pm 8-kV \) Contact, \( \pm 15-kV \) Air Gap IEC61000-4-2 Level 4C
- Packages
  - 42-ball (8.38 mm\(^2\)) CSP, 40-pin (36 mm\(^2\)) QFN and 32-pin (25 mm\(^2\)) QFN

**Collateral**
- Datasheet: CCG3 Datasheet

**Availability**
- Production: Now

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1 Mode of operation in which the data lines are repurposed to transmit non-USB data
2 The encryption hardware and software required to implement USB Authentication
3 A USB-F is a USB De-Facto standard that defines the authentication protocol for Type-C accessories
4 A USB Device controller that informs the USB Host of the supported Alternate Modes
5 A specification that defines the method for a USB Device to communicate the supported Alternate Modes
6 Circuits to control the gates of external power Field-Effect Transistors (FETs) on \( V_{BUS} \) (5-20 V)
7 Termination resistors: \( R_P \) as a DFP, \( R_D \) as a UFP, \( R_A \) as an EMCA
EZ-PD CCG2
USB Type-C and PD Port Controller

Applications
USB Type-C Electronically Marked Cabled Assembly (EMCA) and powered accessories

Features
- 32-bit MCU Subsystem
  - 48-MHz Arm® Cortex®-M0 CPU with 32KB Flash and 4KB SRAM
- Integrated Digital Blocks
  - Integrated timer/counter/pulse-width modulators (TCPWMs)
  - Two SCBs\(^1\) configurable to I2C, SPI or UART modes
- Type-C Support
  - Integrated transceiver, supporting one Type-C port
  - Integrated termination resistors (R\(_P\), R\(_D\), R\(_A\))\(^2\)
- Power Delivery (PD) Support
  - Standard power profiles
- Low-Power Operation
  - Two independent V\(_{CONN}\) rails with integrated isolation
  - Independent supply voltage pin for GPIO
  - 2.7–5.5-V operation; Sleep: 2.0 mA; Deep Sleep: 2.5 \(\mu\)A
- System-Level ESD on CC and VDD Pins
  - ±8-kV Contact, ±15-kV Air Gap IEC61000-4-2 Level 4C
- Packages
  - 20-ball CSP (3.3 mm\(^2\)) with 0.4-mm ball pitch, 14-pin DFN (2.5 x 3.5 mm) with 0.6-mm pin pitch and 24-pin QFN (4 mm\(^2\)) with 0.55-mm pin pitch

Collateral
Datasheet: [CCG2 Datasheet](#)
Reference Design Kit: [CCG2 RDK](#)
Evaluation Kit: [CCG3 EVK](#)

CCG2: USB Type-C Port Controller With PD

Available Collateral
- Datasheet: [CCG2 Datasheet](#)
- Reference Design Kit: [CCG2 RDK](#)
- Evaluation Kit: [CCG3 EVK](#)

Production: Now

1. Serial communication block configurable as UART, SPI or I2C
2. Termination resistors: R\(_P\) read as a DFP, R\(_D\) as a UFP, R\(_A\) as an EMCA
EZ-USB FX3
USB 3.1 Gen 1 Peripheral Controller

Applications
Industrial cameras, medical and machine vision cameras, 3-D and 1080p full HD and 4K Ultra HD (UHD) cameras, document and fingerprint scanners, videoconferencing and data acquisition systems, video capture cards and HDMI converters, protocol and logic analyzers, USB test tools and software-designed radios (SDRs)

Features
- USB 3.1 Gen 1-Compliant Peripheral Controller
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- Fully Accessible 32-bit, 200-MHz Arm® 926EJ Core
  - 512KB of embedded SRAM for code space and buffers
- 32-bit, 100-MHz, flexible GPIF II Interface
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- Flexible Clock Options
- Packages
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
Datasheet: [FX3 Datasheet](#)
Development Kit: [FX3 SuperSpeed Explorer Kit](#)
Software Development Kit: [EZ-USB FX3 SDK](#)

Availability
Production: Now
EZ-USB FX3S
USB 3.1 Gen 1 RAID¹-on-Chip

Applications
Servers, routers, mobile storage, USB Flash drives, POS terminals, automatic teller machines (ATM), SDIO expanders, and data logging devices

Features
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - USB-IF-certified (TID: 340800007)
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz Arm® 926EJ Core**
  - 512KB of embedded SRAM for code space and buffers
- **32-bit, 100-MHz, Flexible GPIF II Interface**
  - Other peripheral interfaces such as I²C, I²S, UART, SPI and 12 GPIOs
  - Unused I/O pins can be used as GPIOs
- **Two SDXC², eMMC³ 4, 4, or SDIO 3.0 Interfaces**
  - Support RAID0 or RAID1 configurations
- **Flexible Clock Options**
  - 19.2-MHz crystal or 19.2-MHz, 26-MHz, 38.4-MHz and 52-MHz clock input
- **Packages**
  - 121-ball BGA (10 mm²), 131-ball WLCSP (4.7 x 5.1 mm)

Collateral
- Datasheet: [FX3S Datasheet](#)
- Kit: [FX3S RAID¹-on-Chip Boot Disk Kit](#)
- Software Development Kit: [EZ-USB FX3 SDK](#)

Availability
Production: Now

¹ Redundant array of independent disks
² SD extended capacity
³ Embedded Multimedia Card
**EZ-USB CX3**

**MIPI\(^1\) CSI-2 to USB 3.1 Gen 1 Bridge**

### Applications
- Industrial, medical and machine vision cameras, 1080p full HD and 4K Ultra HD (UHD) cameras, document scanners, fingerprint scanners, game consoles, videoconferencing systems, notebook PCs, tablets and image acquisition systems

### Features
- **USB 3.1 Gen 1-Compliant Peripheral Controller**
  - Up to 32 USB endpoints
- **Fully Accessible 32-bit, 200-MHz Arm\(^9\) 926EJ core**
  - 512KB of embedded SRAM for code space and buffers
- **Four-Lane MIPI\(^1\) Camera Serial Interface v2.0 (CSI-2) Input**
  - Camera Control Interface (CCI) for image sensor configuration
  - Other peripheral interfaces such as I\(^2\)C, UART, SPI, and 12 GPIOs
- **Supports Industry-Standard Video Data Formats**
  - RAW8/10/12/14\(^2\), YUV422/444\(^3\), RGB888/666/565\(^4\)
- **Supports Uncompressed Streaming Video**
  - 4K UHD at 15 fps, 1080p at 30 fps, 720p at 60 fps
- **Packages**
  - 121-ball BGA (10 x 10 x 1.7 mm)

### Collateral
- **Datasheet:** [CX3 Datasheet](#)
- **Reference Design Kit:** [CX3 Reference Design Kit](#)
- **Software Development Kit:** [EZ-USB FX3 SDK](#)

### Availability
- **Production:** Now

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1 Mobile Industry Processor Interface  
2 Video format for luminance and chrominance components  
3 Video format for raw video data  
4 Video format for red, green and blue pixel components
**EZ-USB GX3**

**USB 3.1 Gen 1 to GigE¹ Bridge**

### Applications
USB dongles, docking stations and port replicators, network printers and security cameras, ultrabooks and home gateways, game consoles and portable media players, DVRs, IP set-top boxes and IP TVs, and other embedded systems

### Features
- **One-Chip USB 3.1 Gen 1 to 10/100/1000M GigE Bridge**
  - Integrates USB 3.1 Gen 1 PHY and GigE PHY
  - Integrates USB 3.1 Gen 1 Controller and GigE MAC²
  - Needs only a 25-MHz crystal to drive both USB and GigE1 PHY
- **IEEE 802.3az³ Support for Low-Power Idle State**
  - Supports dynamic cable length and power adjustment
  - Offers multiple power management wake-on-LAN⁴ features
- **Supports Optional EEPROM to Store USB Descriptors**
  - Integrates on-chip power-on-reset (POR) circuitry
- **Packages**
  - 68-QFN (8 x 8 x 0.85 mm)

### Collateral
- **Datasheet:** [GX3 Datasheet](#)
- **Reference Design Kit:** [GX3 Reference Design Kit](#)
- **Software & Drivers:** [GX3 Drivers](#)

### Availability
**Production:** Now

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¹ Gigabit Ethernet
² Media access controller that provides the address to an Ethernet node
³ A new-energy efficient Ethernet standard
⁴ An Ethernet standard that allows a computer to be turned on by a network message
EZ-USB HX3
USB 3.1 Gen 1 Hub

Applications
Docking stations for notebook PCs and tablets, PC motherboards, servers, televisions and monitors, retail hub boxes, printers and scanners, set-top boxes, home gateways, routers and game consoles

Features
- USB 3.1 Gen 1-Compliant Four-Port Hub Controller
  - USB-IF certified (Test ID: 330000047)
  - WHQL certified for Windows 7, Window 8, Windows 8.1
- Shared Link™
  - Supports simultaneous USB 2.0 and USB SuperSpeed (SS) devices on the same port
- Ghost Charge™
  - Enables USB charging while the hub is disconnected from a USB Host
- Charging Standard support
  - USB-IF Battery Charging (BC) v1.2, Apple Charging Standard
  - Charging an OTG Host in an ACA-Dock
- Programming of External EEPROM via USB
- Configurable USB SS and USB 2.0 PHY (drives 11” trace)
- Packages
  - 68-QFN (8 x 8 x 1.0 mm), 88-QFN (10 x 10 x 1.0 mm), 100-BGA (6 x 6 x 1.0 mm)

Datasheet: HX3 Datasheet
Kit: CY4609, CY4603, CY4613
Configuration Utility: Blaster Plus¹
App Notes: HX3 Hardware Design Guide (AN91378)

¹ A Cypress GUI-based PC application for setting HX3 configuration parameters
² Transaction translator

Availability
Production: Now
EZ-USB HX3C
USB 3.1 Gen 1 Type-C PD Hub

Applications
USB Type-C charging hubs, adapters and accessories, docking stations for notebook PCs and tablets, televisions and monitors, PC motherboards and servers, set-top boxes, home gateways and routers

Features
- USB 3.1 Gen 1-Compliant Hub Controller with Type-C and PD
  - Upstream (US): Type-C, Downstream (DS): 1 Type-C and 2 Type-A ports
- Integrated Type-C Transceivers, Supporting Two Type-C Ports
  - Integrated termination resistors (R_P and R_D)\(^1\)
  - Integrated USB Billboard Controller\(^2\)
- Charging Support
  - USB PD, BC v1.2, Apple Charging Standard
  - PD policy engine configures power profiles dynamically
- Ghost Charge™
  - Charging DS without US connection
- Firmware Upgradable Over USB
- System-Level ESD on Configuration Channel (CC) Pins
  - 8 kV Contact, 15 kV Air
- Configurable USB SS and USB 2.0 PHY (drives 11" trace)
- Packages
  - 121-ball BGA (10 mm x 100 mm, 0.8 mm ball-pitch)

Collateral
Datasheet: HX3C Datasheet
Reference Design: HX3C Type-C Monitor/Dock Reference Design

Availability
Production: Now

HX3C: USB 3.1 Gen 1 Type-C PD Hub

^1 Termination resistors: R_P read as a DFP, R_D as a UFP
^2 A USB Device controller that is used to implement the USB Billboard Device Class Informs the USB Host of the supported Alternate Modes as well as any failures
^3 Transaction Translator