AN99123

Reset Voltage and Timing Requirements for MirrorBit® Flash

AN99123 describes the considerations of reset control signal timing when using MirrorBit NOR flash devices in an application.

1 Synopsis

MirrorBit NOR flash has several unique reset control signal timing requirements. Timing requirements vary by MirrorBit processes and families. System designers must accommodate these requirements for reliable operation.

2 Applicable Device Families

- 90 nm MirrorBit Process: S29GLxxxP, S29WSxxxP
- 65 nm MirrorBit Process: S29VS/XSxxxR
- 65 nm MirrorBit Eclipse™ Process: S29GLxxxS (≤ 1 GBit), S70GL02GS
- 45 nm MirrorBit Eclipse™ Process: S29GLxxxT (≤ 1 GBit), S70GL02GT

3 Parameters of Interest

V_{LKO}	Low V_{CC} Lock-Out Voltage
t_{VCS}	V_{CC} > V_{CC-MIN} setup requirement prior to RESET# negation or CE# assertion
t_{VIOS}	V_{IO} > V_{IO-MIN} setup requirement prior to RESET# negation or CE# assertion
t_{RP}	RESET# pulse width (assertion period)
t_{RH}	RESET# high requirement prior to CE# assertion
t_{READY}	Period from RESET# assertion to RY/BY# negation
t_{RB}	PERIOD from RY/BY# negation to CE# assertion

4 Reset Requirements - 90 nm Process Node Products

Reset conditions are required for the 90 nm MirrorBit devices because of circuit changes implemented to reduce die size and to improve endurance of Advanced Sector Protection PPB bits. The Power-On-Reset and Warm Reset requirements for these new device families are reviewed in this section.

4.1 Power-On-Reset Requirements

During Power-On, V_{CC} should rise monotonically and must remain greater than V_{LKO} during all reset operations. V_{IO} can either be tied to V_{CC} or can be driven to a different voltage level. In the latter case, V_{IO} must exceed V_{IO_MIN} before RESET# is negated and must be maintained between V_{IO_MIN} and V_{CC} +100 mV.

During V_{CC} ramp-up, RESET# must be asserted (low). From the time when V_{CC} exceeds V_{CC_MIN}, RESET# must remain asserted for a period of t_{VCS}) prior to negation (see Figure 1). Control signal transitions can be initiated t_{RH} following RESET# negation.

4.1.1 Power-On-Reset Timing

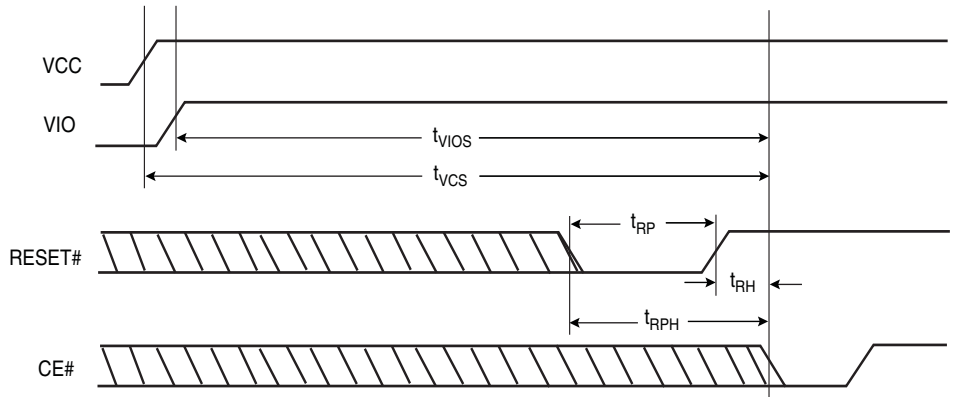
Table 1. 90 nm Process Node Products - Power-On-Reset Timing

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{VCS}	V_{CC} Setup Time to CE# assertion (min)	30 µs	35 µs
t_{VIOS}	V_{IO} Setup Time to CE# assertion (min)	30 µs	35 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

Notes:

1. *For S29WSxxxP, V_{CC} ramp rate must exceed 1V/400 µs otherwise a hardware reset would be required.*
2. *For S29WSxxxP, VIO pin is named $V_{CC}Q$.*
3. *V_{CC} and V_{IO} (resp. $V_{CC}Q$) must be ramped up simultaneously for proper power-up.*
4. *If RESET# is not stable for t_{VCS} or t_{VIOS}: The device does not permit any read and write operations, a valid read operation returns FFh and a hardware reset is required.*

Figure 1. 90 nm Process Node Products- Power-On Reset Timing



4.2 Warm-Reset Requirements

Warm-Reset, also known as Hard Reset, requires RESET# to pulse from high to low to high. Timing requirements vary by the state of the device prior to RESET# assertion, specifically whether or not the device is performing an embedded operation (program or erase operation in progress).

During Warm-Reset operations, V_{CC} must be maintained greater than V_{LKO}.

4.2.1 Warm-Reset Timing While Embedded Operation Not In Progress

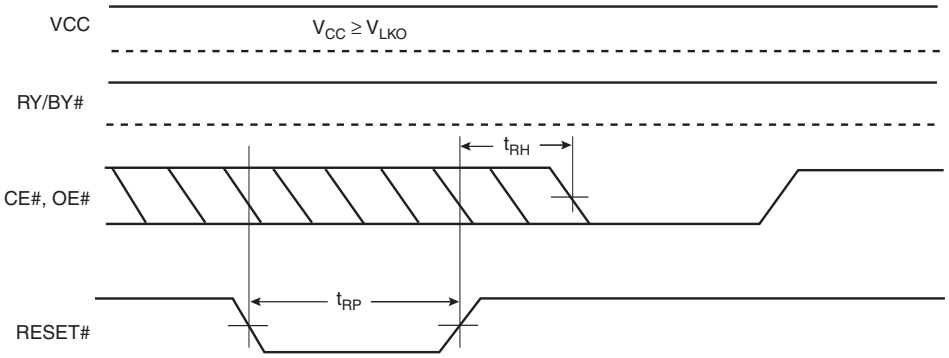
In the event of the Warm-Reset being initiated when an embedded operation is not in progress (see Figure 2), the internal reset operation requires t_{RP} to be completed. Control signal transitions can be initiated t_{RH} following internal reset operation completion. RY/BY# will stay in the ready state as the device operates during non-embedded operations.

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

Table 2. 90 nm Process Node Products - Warm Reset Timing - Embedded Operation Not in Progress

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{RP}	RESET# Pulse Width (min)	30 µs	35 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

Figure 2. 90 nm Process Node Products– Warm Reset Timing – Embedded Operation Not In Progress



4.2.2 Warm-Reset Timing While Embedded Operation In Progress

In the event of the Warm-Reset being initiated when an embedded operation is in progress (see Figure 3), the internal reset operation requires t_{READY} to be completed. t_{READY} is comprised of the time required to gracefully exit an embedded programming operation, followed by the standard internal reset operation and the set-up time from reset operation completion until a control signal transition detection can be guaranteed.

The complete reset operation is triggered by the falling edge of RESET#. RESET# must remain asserted for a period of t_{RP}. Control signals transition can be initiated by t_{READY} after the falling edge of RESET#.

Table 3. 90 nm Process Node Products - Warm Reset Timing - Embedded Operation in Progress

Parameter	Description	S29WSxxxP	S29GLxxxP
t_{READY}	RESET# assertion to RY/BY# negation (min)	30.2 µs	35.2 µs
t_{RB}	RY/BY# high to CE# assertion (min)	0 ns	0 ns
t_{RP}	RESET# Pulse Width (min)	30 µs	35 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns	200 ns

Notes:

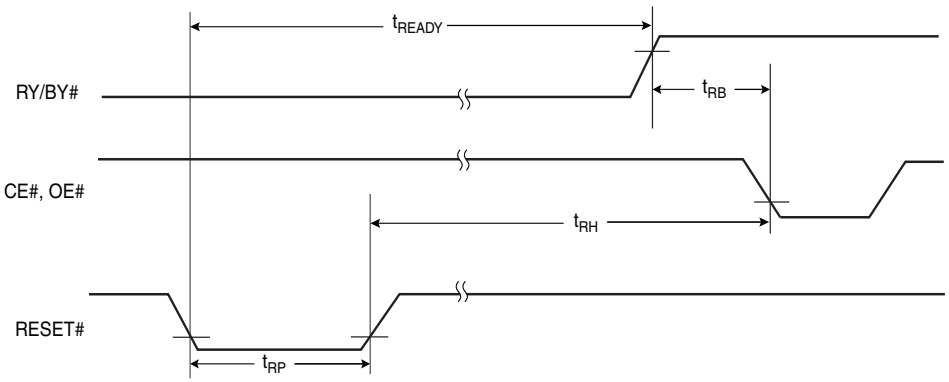
1. *For S29WSxxxP and S29GLxxxP, $t_{READY} = t_{RP} + t_{RH}$. No additional waiting time is required.*

A typical implementation would have RESET# asserted a period of t_{READY} with a short delay from RESET# negation before asserting CE# and initiating a read operation.

An alternate implementation is asserting RESET# for a shorter period of t_{RP} and employing a delay loop to prevent flash control signal accesses for t_{READY} from the assertion of RESET#.

An additional option is to monitor RY/BY# following the rising edge of a RESET# pulse at least t_{RP} in duration. When RY/BY# is detected high, control signal transitions can be initiated.

Figure 3. 90 nm Process Node Products - Warm Reset Timing – Embedded Operation In Progress



5 Reset Requirements - 65 nm Process Node Products

Reset conditions are required for the 65 nm MirrorBit devices because of circuit changes implemented to reduce die size. The Power-On-Reset and Warm Reset requirements for these new device families are reviewed in this section.

5.1 Power-On-Reset Requirements

During Power-On, the V_{CC} and V_{IO} ramp rate could be non-linear. However, V_{CC} and V_{IO} must remain greater than V_{LKO} during all reset operations. It is also recommended to ramp up those two signals simultaneously.

5.1.1 Power-On-Reset Timing

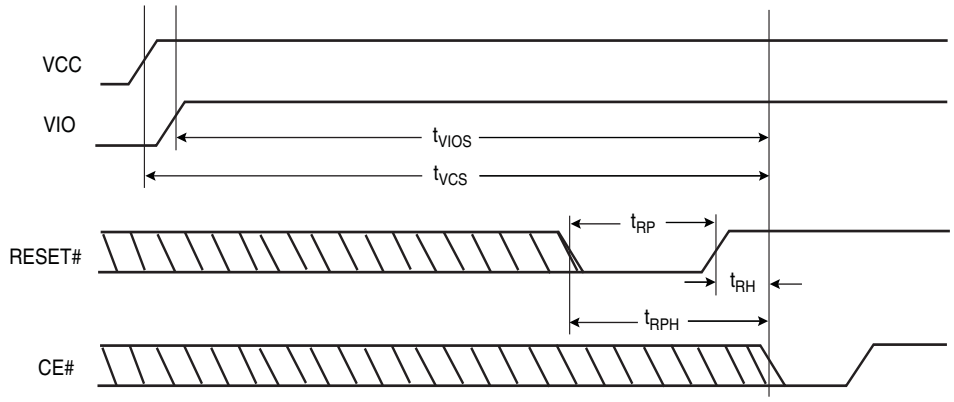
Table 4. 65 nm Process Node Products - Power-On-Reset Timing

Parameter	Description	S29VS/XSxxxR
t_{VCS}	V_{CC} Setup Time to CE# assertion (min)	300 µs
t_{VIOS}	V_{IO} Setup Time to CE# assertion (min)	300 µs
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns
t_{RP}	RESET# Pulse Width (min)	50 ns
t_{RPH}	RESET# Low to CE# Low (min)	10 µs

Notes:

1. *V_{CC} and V_{IO} ramp rate could be non-linear.*
2. *RESET# must be high after V_{CC} and V_{IO} are higher than V_{CC} minimum.*
3. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*

Figure 4. 65 nm Process Node Products - Power-On Reset Timing



5.2 Warm-Reset Requirements

Warm-Reset, also known as Hard Reset, requires RESET# to pulse from high to low to high. Starting from the 65 nm MirrorBit products, the warm reset timing requirements will be totally independent from the state of the device prior to RESET# assertion, namely whether an embedded operation was in progress or not.

During Warm-Reset operations, V_{CC} must be maintained greater than V_{LKO}.

During Warm-Reset (see Figure 5), the internal reset operation requires t_{RP} to be completed. Control signal transitions may be initiated t_{RH} following RESET# negation.

5.2.1 Warm-Reset Timing

Table 5. 65 nm Process Node Products - Warm Reset Timing

Parameter	Description	S29VS/XSxxxR
t_{RPH}	RESET# Low to CE# Low (min)	10 µs
t_{RP}	RESET# Pulse Width (min)	50 ns
t_{RH}	RESET# high prior to CE# assertion (min)	200 ns

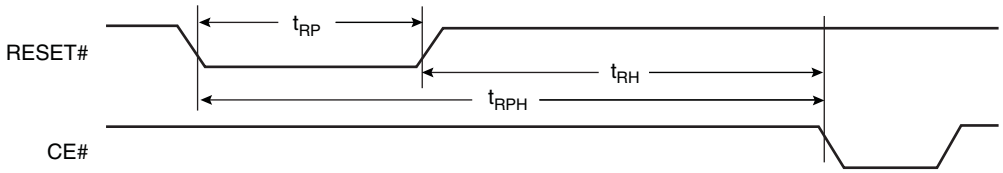
Notes:

1. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
2. *CE#, OE# and WE# must be at logic high during Reset Time.*

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

An equally effective and alternate implementation for the 65 nm MirrorBit devices is asserting RESET# for a short period followed by a long delay to allow the completion of the internal reset operation prior to initiating control signal transitions.

Figure 5. 65 nm Process Node Products – Warm Reset Timing



6 Reset Requirements - 65 nm / 45 nm Eclipse MirrorBit Products

Reset conditions are required for the 65 nm and 45 nm Eclipse MirrorBit devices because of circuit changes implemented to reduce die size. The Power-On-Reset and Warm Reset requirements for these new device families are reviewed in this section.

6.1 Power-On-Reset Requirements

During Power-On, V_{CC} and V_{IO} ramp rate could be non-linear. However, V_{CC} and V_{IO} must remain greater than V_{LKO} during all reset operations. It is also recommended to ramp up those two signals simultaneously.

6.1.1 Power-Up Sequencing

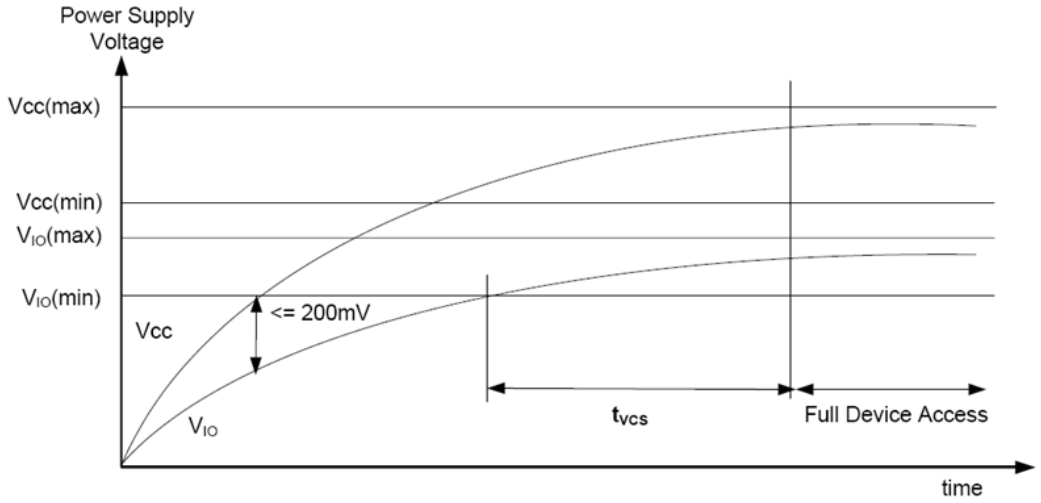
V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$). V_{IO} must track the rise and fall of V_{CC} within 200 mV ($V_{IO} \geq V_{CC}$ - 200 mV) when V_{IO} is below the V_{IO} minimum.

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above, the minimum V_{CC} and V_{IO} thresholds. During t_{VCS} the device is performing power on reset operations.

Table 6. 65 nm / 45 nm Eclipse Products - Power-Up Timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{VCS}	V_{CC} Setup Time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{VIOS}	V_{IO} Setup Time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs

Figure 6. 65 nm /45 nm Eclipse Products - Power-up Timing



6.1.2 Power-On-Reset Timing

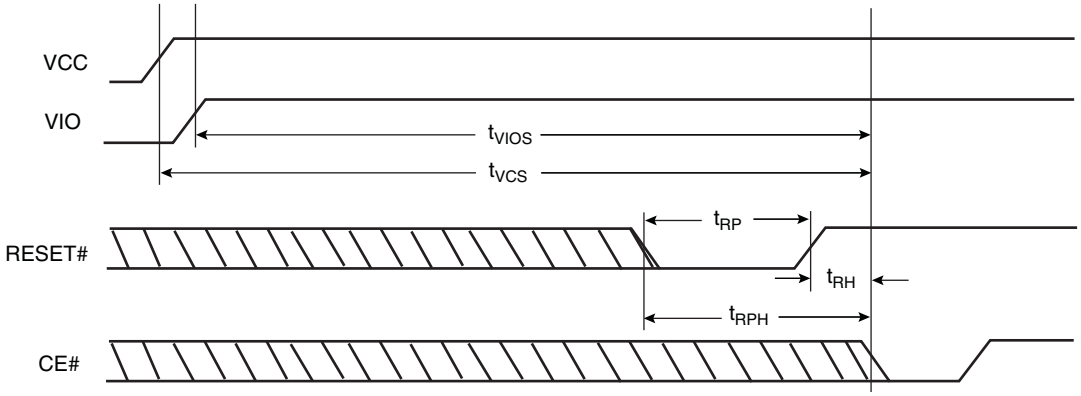
Table 7. 65 nm / 45 nm Eclipse Products - Power-On-Reset Timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{VCS}	V_{CC} Setup Time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{VIOS}	V_{IO} Setup Time to CE# assertion (min)	300 µs	600 µs	300 µs	600 µs
t_{RH}	RESET# high prior to CE# assertion (min)	50 ns	50 ns	50 ns	50 ns
t_{RP}	RESET# Pulse Width (min)	200 ns	200 ns	200 ns	200 ns
t_{RPH}	RESET# Low to CE# Low (min)	35 µs	70 µs	35 µs	70 µs

Notes:

1. *V_{CC} and V_{IO} ramp rate could be non-linear.*
2. *RESET# Low is optional during POR. If RESET# is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CE# may go Low. If RESET# remains low after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET# must also be high t_{RH} before CE# goes low.*
3. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
4. *RY/BY# pin is low during power-up.*

Figure 7. 65 nm / 45 nm Eclipse Products - Power On Reset Timing



6.2 Warm-Reset Requirements

Warm-Reset, also known as Hard Reset, requires RESET# to pulse from high to low to high. For the 65 nm and 45 nm MirrorBit Eclipse products, the warm reset timing requirements will be also totally independent from the state of the device prior to RESET# assertion, namely whether an embedded operation was in progress or not.

During Warm-Reset operations, V_{CC} must be maintained greater than V_{LKO}.

During Warm-Reset (see Figure 8), the internal reset operation requires t_{RP} to be completed. Control signal transitions may be initiated t_{RH} following RESET# negation.

6.2.1 Warm-Reset Timing

Table 8. 65 nm / 45 nm Eclipse Products - Warm Reset Timing

Parameter	Description	S29GLxxxS ≤ 1 Gbit	S70GL02GS	S29GLxxxT ≤ 1 Gbit	S70GL02GT
t_{RPH}	RESET# Low to CE# Low (min)	35 µs	70 µs	35 µs	70 µs
t_{RP}	RESET# Pulse Width (min)	200 ns	200 ns	200 ns	200 ns
t_{RH}	RESET# high prior to CE# assertion (min)	50 ns	50 ns	50 ns	50 ns

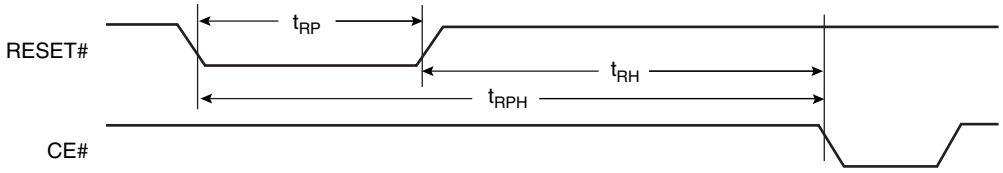
Notes:

1. *The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
2. *CE#, OE# and WE# are recommended to be at logic high during Reset Time.*

The typical implementation would have RESET# asserted for at least the time required to complete the internal reset operation and a short delay following RESET# negation prior to initiating control signal transitions.

An equally effective and alternate implementation for the 65 nm and 45 nm MirrorBit Eclipse devices is asserting RESET# for a short period followed by a long delay to allow the completion of the internal reset operation prior to initiating control signal transitions.

Figure 8. 65 nm / 45 nm Eclipse Products - Warm Reset Timing



Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	11/14/2006 to 10/04/2010	Initial version Updated document format Removed all references to AM29LVxxxM, MBM29PLxxxM, S29GLxxxM, S29PLxxxP and S29GLxxxA Added POR and Reset requirements for 90 nm, 65 nm and 65 nm Eclipse products
*A	4980968	MSWI	10/22/2015	Updated in Cypress template
*B	5872180	AESATMP8	09/05/2017	Updated logo and Copyright.
*C	6353923	BACD	10/17/2018	Removed references to 110nm products Removed references to S29NSxxxP, S29GLxxxR, S29WSxxxR and S29NSxxxR Updated with the 45nm products requirements

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