Migrating from S29JL-H (32-64 Mb) to S29JL-J

AN98587 discusses the specification differences that must be considered when migrating from a S29JL-H NOR flash device to a S29JL-J NOR flash device.

1 Introduction

The 32 and 64 Mbit S29JL-H NOR flash was made on the Cypress 130 nm floating gate NOR technology process node. Viable long term replacements for the S29JL032H and S29JL064H are the S29JL032J and S29JL064J, respectively. The 32 and 64 Mbit S29JL-J NOR flash are made on Cypress's 110 nm floating gate NOR technology process node. This application note discusses the specification differences that must be considered when migrating from a S29JL-H NOR flash device to a S29JL-J NOR flash device.

2 Feature Comparison and Differences

The S29JL-H and S29JL-J flash families have feature sets that are predominantly compatible. Table 1 lists the similarities and differences of features and architectures offered in these two families. As a result of the minimal differences, many S29JL-H applications will directly support S29JL-J flash devices with only minor or no hardware or software modifications.

Table 1. High Level Feature Comparison (Sheet 1 of 2)

Feature	S29JL032H	S29JL032J	S29JL064H	S29JL064J
NOR Technology	Floating Gate	Floating Gate	Floating Gate	Floating Gate
Process Node	130 nm	110 nm	130 nm	110 nm
Array Size	4,194,304 bytes	4,194,304 bytes	8,368,608 bytes	8,368,608 bytes
Data Bus	x8/x16	x8/x16	x8/x16	x8/x16
Boot Sector Model Architecture	8-8 kB, 63-64 kB	8-8 kB, 63-64 kB	8-8 kB, 126-64 kB, 8-8 kB	8-8 kB, 126-64 kB, 8-8 kB
Sector Banks	2 or 4 (1)	2 or 4 (1)	4	4
Simultaneous Read-while-Write	yes	yes	yes	yes
Asynchronous Read &/or Write	yes	yes	yes	yes
Synchronous Read &/or Write	no	no	no	no
Speed Grade Options (TACC/TRC/TWC)	60, 70, 90 ns	60, 70 ns	55, 60, 70, 90 ns	55, 60, 70 ns
Total Secured Silicon Sector (OTP) Size	256 bytes	256 bytes	256 bytes	256 bytes
User Lockable Secured Silicon Sector (OTP Size)	256 bytes	256 bytes	256 bytes	256 bytes
Factory- vs. Customer- vs. Not-Locked Unique Indicator for Secure Silicon Sector	no	yes	no	yes
JEDEC-compatible pin out	yes	yes	yes	yes
Ready/Busy output (RY/BY#)	yes	yes	yes	yes
Hardware Reset input (RESET#)	yes	yes	yes	yes
Accelerated Program input (WP#/ACC)	yes	yes	yes	yes
Write Protect input (WP#/ACC)	yes	yes	yes	yes
High Voltage Sector Protection	yes	yes	yes	yes

Table 1. High Level Feature Comparison (Sheet 2 of 2)

Feature	S29JL032H	S29JL032J	S29JL064H	S29JL064J
Autoselect/Sector Protection Voltage (V_{ID})	8.5-12.5V	8.5-12.5V	11.5-12.5V	11.5-12.5V
Accelerated Programming Voltage (V_{HH})	8.5-9.5V	8.5-9.5V	8.5-9.5V	8.5-9.5V
JEDEC-compatible software command set	yes	yes	yes	yes
Autoselect Device ID read cycles	1 or 3 cycles (2)	1 or 3 cycles (2)	3 cycles	3 cycles
Common Flash Interface (CFI)	yes	yes	yes	yes
Unlock Bypass Program command	yes	yes	yes	yes
Erase Suspend/Resume commands	yes	yes	yes	yes
Program Suspend/Resume commands	no	no	no	no
Industrial Temperature (-40°C to +85°C)	yes	yes	yes	yes
Extended Temperature (-40°C to +125°C)	no	no	no	no
Program/Erase Cycle Endurance (typical)	1,000,000	1,000,000	1,000,000	1,000,000
Data Retention (typical)	20 years	20 years	20 years	20 years
TSOP Package Option: 48-pin TS048	yes	yes	yes	yes
BGA Package Option: 48-ball VBK048	yes	yes	no	yes
BGA Package Option: 63-ball FBE063	no	no	yes	no

Notes:

1. *S29JL032H and S29JL032J models 01 and 02 have four banks, all other models have two banks.*
2. *Device ID reads for S29JL032H and S29JL032J models 01 and 02 require three cycles, all other models require one cycle.*

Primary differences between these two flash families are related to: Secure Silicon Sector (OTP) Lock Status indication, CFI register values, DC and AC parameters including Speed Grade options and packaging options. Details of all relevant differences will be highlighted and discussed in subsequent sections.

2.1 Bank and Sector Architectural Options

As illustrated in Table 2, the S29JL-H and S29JL-J devices are offered in a variety of bank and sector architecture options.

The S29JL032H and S29JL032J are available with dual or quad bank boot sector architecture which enables zero latency simultaneous read-while-write operation. All models feature a user configurable x8 or x16 data bus. Dual bank devices (21, 22, 31, 32, 41, 42) are available with several bank size options, 4/28 Mbit, 8/24 Mbit or 16/16 Mbit, along with a hybrid sector array architecture consisting of 8 - 8 kB boot sectors and 64 kB uniform sectors. The boot sectors occupying either the top or bottom 64 kB of the flash array. Quad bank devices (models 01, 02) feature two 12 Mbit banks with 64 kB uniform sectors and two 4 Mbit banks, one with 64 kB uniform sectors and the other with a hybrid sector architecture consisting of 8 kB boot sectors and 64 kB uniform sectors.

The S29JL064H and S29JL064J are offered in a single model with identical quad bank boot sector architectures. These devices feature two 24 Mbit banks with 64 kB uniform sectors and two 8 Mbit banks, each with a hybrid sector architecture consisting of 8 kB boot sectors and 64 kB uniform sectors. The boot sectors are located at both the top and bottom of the flash array.

Table 2. Comparative Bus, Bank and Sector Architectures

Base Device	Model	Data Bus Width	Bank Quantity	Bank Size & Orientation (Mbit)	Sector Architecture (SA0 - SAmax)
S29JL032	01	x8 or x16	4	4 / 12 / 12 / 4	8-64 kB / 24-64 kB / 24-64 kB / 7-64 kB, 8-8 kB
S29JL032	02	x8 or x16	4	4 / 12 / 12 / 4	8-8 kB, 7-64 kB / 24-64 kB / 24-64 kB / 8-64 kB
S29JL032	21	x8 or x16	2	28 / 4	56-64 kB / 7-64 kB, 8-8 kB
S29JL032	22	x8 or x16	2	4 / 28	8-8 kB, 7-64 kB / 56-64 kB
S29JL032	31	x8 or x16	2	24 / 8	48-64 kB / 15-64 kB, 8-8 kB
S29JL032	32	x8 or x16	2	8 / 24	8-8 kB, 15-64 kB / 48-64 kB
S29JL032	41	x8 or x16	2	16 / 16	32-64 kB / 31-64 kB, 8-8 kB
S29JL032	42	x8 or x16	2	16 / 16	8-8 kB, 31-64 kB / 32-64 kB
S29JL064	00	x8 or x16	4	8 / 24 / 24 / 8	8-8 kB, 15-64 kB / 48-64 kB / 48-64 kB / 15-64 kB, 8-8 kB

2.2 Autoselect and CFI Registers

Autoselect and CFI registers can be used for in-system identification of flash devices and dynamic software driver configuration. Each S29JL model has a unique Autoselect Device ID. The Device IDs are identical for corresponding S29JL-H and S29JL-J models to simplify migrations.

Table 3 lists the differences between corresponding models of S29JL-H and S29JL-J. Refer to data sheets for complete Autoselect register and CFI register listings.

Table 3. Autoselect and CFI Related Differences

Feature	S29JL032H	S29JL032J	S29JL064H	S29JL064J
Autoselect Secure Silicon Sector Region - Factory Locked Code (DQ[7:0])	82h	82h	81h	81h
Autoselect Secure Silicon Sector Region - Customer Locked Code (DQ[7:0])	42h	42h	01h	41h
Autoselect Secure Silicon Sector Region - Default Not Locked Code (DQ[7:0])	82h	02h	01h	01h
CFI @ 44h (byte address): Typical timeout for chip erase	0000h	000Fh	0000h	000Fh
CFI @ 46h (byte address): Maximum timeout for single byte/word write	0005h	0004h	0005h	0004h
CFI @ A0h (byte address): Program Suspend Support	0001h	0000h	0001h	0000h

2.2.1 Secure Silicon OTP Region Lock Indication

The S29JL032H and S29JL064J had different Secure Silicon Sector lock indication schemes. In the S29JL-H devices, the Secure Silicon Sector lock status is assessed by entering Autoselect Mode and performing a read at offset 0x06 (x8 address reference).

For the S29JL032H, if the Secure Silicon Sector was Factory Locked or is in the default Unlocked state, the returned value will be 82h. If the Secure Silicon Sector was Customer Locked, the returned value will be 42h.

For the S29JL064H, if the Secure Silicon Sector was Factory Locked, the returned value will be 81h. If the Secure Silicon Sector was Customer Locked or is in the default Unlocked state, the returned value will be 01h.

The S29JL032J and S29JL064J have a consistent and finer granularity Secure Silicon Region lock indication scheme. Secure Silicon Sector lock status is assessed in the same manner as in the S29JL-H, by entering Autoselect Mode and performing a read at offset 0x06 (x8 address reference). If the Secure Silicon Sector was Factory Locked, the returned value will be 81h. If the Secure Silicon Sector was Customer Locked, the returned value will be 41h. If the Secure Silicon Sector is in the default Unlocked state, the returned value will be 01h.

When migrating from S29JL-H to S29JL-J, system software may require modification if the application evaluates Secure Silicon Sector lock status. If the Secure Silicon Sector is not locked, either by factory or customer, then no system software modifications are required due to this feature difference.

2.2.2 CFI Register Differences

There are three differences in CFI register values between like-models of S29JL-H and S29JL-J. Two are related to erase and programming performance and one is related to feature support indication.

The CFI register value at x8 offset 0x44 provides typical chip erase operation timeout guidance. For the S29JL-H devices, this value was 0000h, indicating no guidance was provided for typical chip erase performance. For the S29JL-J, this value is 000Fh, indicating a typical chip erase should complete in 2^{15} ms. This CFI register value change will not impact migrations from S29JL-H to S29JL-J. Existing system software could not make erase operation watchdog period decisions based on the returned value from the S29JL-H.

The CFI register value at x8 offset 0x46 provides typical single byte/word programming timeout guidance. For the S29JL-H devices, this value was 0005h, indicating the typical program operation would complete within 2^5 µs. For the S29JL-J, this value is 0004h, indicating the typical program operation would complete within 2^4 µs. This CFI register value change will not impact migrations from S29JL-H to S29JL-J.

The CFI register value at x8 offset 0xA0 provides awareness that program suspend and resume commands are supported. For the S29JL-H devices, this value was 0001h, while for the S29JL-J, this value is 0000h. The 0000h value indicates program suspend and resume commands are not supported. This CFI register value difference will not impact migrations from S29JL-H to S29JL-J because neither device family supports program suspend and resume commands. Existing system software could not make program suspend and resume command support decisions based on the returned value from the S29JL-H.

2.3 DC and AC Specification Differences

The S29JL-J was designed to be DC and AC parameter compatible with S29JL-H to facilitate migrations. Some minor differences in these parameters exist which must be reviewed for each application to assure migrations from S29JL-H to S29JL-J can be supported without system or firmware modification. All pertinent DC and AC specification differences will be discussed in this section.

Table 4 summarizes all differences in the DC specifications for like density S29JL-H and S29JL-J devices. None of the DC parameter differences will prevent migration from S29JL-H to S29JL-J. There is no negative system impact to lower standby, reset, and sleep mode current consumption. There is no negative impact of a marginally higher low V_{CC} lockout voltage in an application designed to comply with the 2.7V minimum V_{CC} voltage applicable to all S29JL-H and S29JL-J devices.

Table 4. DC Specification Differences

Parameter	Description		S29JL032H	S29JL032J	S29JL064H	S29JL064J
I_{CC3}	V_{CC} Standby Current	Max	10 µA	5 µA	5 µA	5 µA
I_{CC4}	V_{CC} Reset Current	Max	10 µA	5 µA	5 µA	5 µA
I_{CC5}	V_{CC} Automatic Sleep Mode Current	Max	10 µA	5 µA	5 µA	5 µA
V_{LKO}	Low V_{CC} Lockout Voltage	Max	2.3V	2.5V	2.3V	2.5V

The S29JL-032H was available in three speed grades ranging from 60 to 90 ns. The S29JL064H was available in four speed grades ranging from 55 to 90 ns. The S29JL032J is available in two speed grades ranging from 60 to 70 ns. The S29JL064J is available in three speed grades ranging from 55 to 70 ns. Specific speed grade options are listed in Table 1. The lack of a 90 ns speed grade option for S29JL-J will not impact migration from the S29JL-H because there are no timing differences that will prevent the use of
70 ns or faster speed grade S29JL-H or S29JL-J devices in applications qualified for use with a 90 ns speed grade S29JL-H device.

Table 5 details the difference in the AC specifications for 70 ns speed grade S29JL-H and S29JL-J devices. Several of the timing parameter differences could cause migration issues and are discussed below.

Table 5. AC Specification Differences (Sheet 1 of 2)

Parameter	Description		S29JL032H	S29JL032J	S29JL064H	S29JL064J
t_{READY}	RESET# Low during embedded algorithm to Read Mode (CE# low)	Max	20 µs	35 µs	20 µs	35 µs
t_{RPD}	RESET# Low to Standby Mode	Min	20 µs	35 µs	20 µs	35 µs

Table 5. AC Specification Differences (Sheet 2 of 2)

Parameter	Description		S29JL032H	S29JL032J	S29JL064H	S29JL064J
t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	12 ns	12 ns	15 ns	15 ns
t_{AH}	Address Hold Time [WE#-controlled Write Cycle] (2)	Min	40 ns	35 ns	40 ns	40 ns
t_{AH}	Address Hold Time [CE#-controlled Write Cycle] (2)	Min	40 ns	35 ns	40 ns	40 ns
t_{DS}	Data Set Up Time [CE#-controlled Write Cycle] (2)	Min	40 ns	30 ns	40 ns	40 ns
t_{CP}	E# Pulse Width [CE#-controlled Write Cycle] (2)	Min	30 ns	35 ns	40 ns	40 ns
t_{ESL}	Erase Suspend Latency	Min	n/s (1)	35 µs	n/s	35 µs
t_{WHWH1}	Byte Program Time (3)	Typ	4 µs	6 µs	5 µs	6 µs
t_{WHWH1}	Byte Program Time (4)	Max	80 µs	80 µs	150 µs	80 µs
t_{WHWH1}	Word Program Time (3)	Typ	6 µs	6 µs	7 µs	6 µs
t_{WHWH1}	Word Program Time (4)	Max	100 µs	80 µs	210 µs	80 µs
t_{WHWH1}	Accelerated Byte/Word Program Time (4)	Max	70 µs	70 µs	120 µs	70 µs
t_{WHWH2}	64 kB Sector Erase Time (3)	Typ	0.4 s	0.5 s	0.4 s	0.5 s
	Chip Erase Time (3)	Typ	28 s	39 s	56 s	71 s

Notes:

1. *n/s = Not Specified*
2. *AC specification comparison shown at 70 ns speed grade.*
3. *Typical program and erase time conditions: 25°C, V_{CC} = 3.0V, 100,000 cycles, checkerboard data pattern.*
4. *Maximum program and erase time conditions: 90°C, V_{CC} = 2.7V, 1,000,000 cycles.*

The S29JL-J family requires a longer period to terminate an embedded algorithm than the S29JL-H. For this reason, t_{READY} has increased to 35 µs minimum from 20 µs minimum. This timing specification difference must be accommodated when migrating from S29JL-H to S29JL-J. CE# assertion must be held off for at least 35 µs from RESET# assertion during a HW Reset when an embedded programming or erase operation is in progress. No change to the RESET# assertion period, t_{RP}, is required, although common practice is to hold RESET# in the asserted state for t_{READY} to assure CE# assertion is delayed adequately.

The S29JL-J family requires a longer period to terminate an embedded algorithm than the S29JL-H. For this reason, t_{RDS} has increased to 35 µs maximum from 20 µs maximum. The implication of this change is the S29JL-J will enter standby mode following RESET# assertion during an embedded operation no more than 15 µs later than the S29JL-H would in the case when CE# is not subsequently asserted. This timing specification difference will not impact migration from S29JL-H to S29JL-J.

The S29JL064H and S29JL064J require address set up to OE# assertion during data polling, t_{ASO}, of 15 ns minimum. The S29JL032H and S29JL032J require address set up to OE# assertion during data polling of 12 ns minimum. This timing specification difference will not impact migration from S29JL032H to S29JL032J or from S29JL064H to S29JL064J. When migrating from S29JL032H to S29JL064J, this timing increase must be accommodated.

The S29JL032J requires write cycle Address hold time from the first falling edge of either WE# or CE#, t_{AH}, of 35 ns minimum. The S29JL032H, S29JL064H and S29JL064J all require a write cycle Address hold time of 40 ns minimum. This timing specification difference will not impact migration from S29JL-H to S29JL-J.

The S29JL032J requires CE#-controlled write cycle data set up to CE# rising edge, t_{DS}, of 30 ns minimum. The S29JL032H, S29JL064H and S29JL064J all require CE#- controlled write cycle data set up of 40 ns minimum. This timing specification difference will not impact migrations from S29JL-H to S29JL-J.

The 32 Mbit S29JL032J requires CE#-controlled write cycle CE# pulse width, t_{CP}, of 35 ns minimum. The 32 Mbit S29JL032H requires CE#-controlled write cycle CE# pulse width of 30 ns minimum. Both the S29JL064H and S29JL064J require CE#-controlled write cycle CE# pulse width of 40 ns minimum. When migrating from

S29JL032H to S29JL032J or to S29JL064J, the increase in minimum CE# pulse width during CE# controlled write cycles must be accommodated. This timing difference will not impact migrations from S29JL064H to S29JL064J.

The S29JL-J requires that system software does not issue non-data polling commands for a period of time, t_{ESL}, of 35 µs minimum following issuance of an Erase Suspend command. The suspend operation takes a finite period of time, during which the flash remains in data polling mode and ignores additional commands. The S29JL-H also required some period of time to complete a suspend operation; however, that period was not specified. For applications that utilize the Erase Suspend feature, this timing parameter must be verified and accommodated when migrating from S29JL-H to S29JL-J.

The S29JL-H and S29JL-J have different program and erase characteristics, as illustrated in Table 5. The differences in typical program and erase specifications will not impact migrations from S29JL032H to S29JL032J or from S29JL064H to S29JL064J; however, they may cause production efficiency related concerns due to increases in average program and/or erase times.

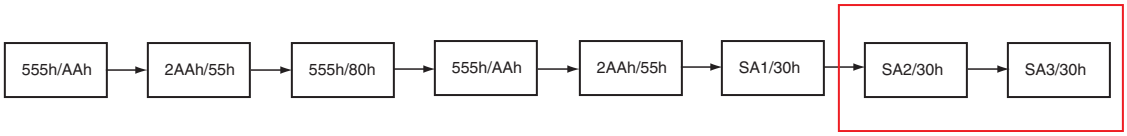
When migrating from S29JL032H to S29JL064J, the impact of the difference in both typical and maximum program and erase timing must be assessed and accommodated.

There are no maximum program or erase performance specification differences that will impact migration from S29JL032H to S29JL032J or from S29JL064H to S29JL064J.

2.4 Multiple Sector Erase

In JL-H or JL-J devices, multiple sectors can be erased together by entering additional sector erase commands before the Sector Erase Timer expires (50 µs from the last Sector Erase Command). However, there is a slight difference on the command sequence requirement between the JL-H and JL-J devices.

As indicated in the JL-J data sheet, the correct command sequence for doing multi-sector erase is shown in Address/Data format:



In this example, two additional sectors, SA2 and SA3 will be erased along with SA1.

When migrating from software that does multi-sector erase on JL-H devices, the software may have two unlock cycles before the red box in the above sequence. Any additional command cycle may cause the multi-sector erase malfunction in JL-J devices.

If no multi-sector erase function is used in JL-H software, no changes are required.

Note that multi-sector erase does not significantly improve the system performance because the actual erase time will be the sum of each individual sector erase time. The time saved by omitting a few command sequences are insignificant compared to the sector erase time.

2.5 Packaging Differences

S29JL032H and S29JL064H can migrate to like models of the S29JL032J and S29JL-J in the TSOP 48-pin TS048 package with no board layout or assembly changes due to the use of identical package and pin outs.

S29JL032H in the VBK048 48-ball fine pitch BGA package can migrate to the S29JL032J in the VBK048 48-ball fine pitch BGA package without layout changes.

S29JL064H in the FBE063 12.0 x 11.0 mm 63-ball fine pitch BGA package can migrate to the S29JL064J in the VBK048 8.15 x 6.15 mm 48-ball fine pitch BGA package without layout changes. These BGA packages share common 48-ball core and signal placement to facilitate migration with only a change in pick and place machine programming to accommodate the different package outside dimensions. Refer to Figure 1, Figure 2, and Table 6 for a comparison of the specifications for these JEDEC standard packages.

Figure 1. VBK048 Drawing (S29JL032H, S29JL032J and S29JL064J)

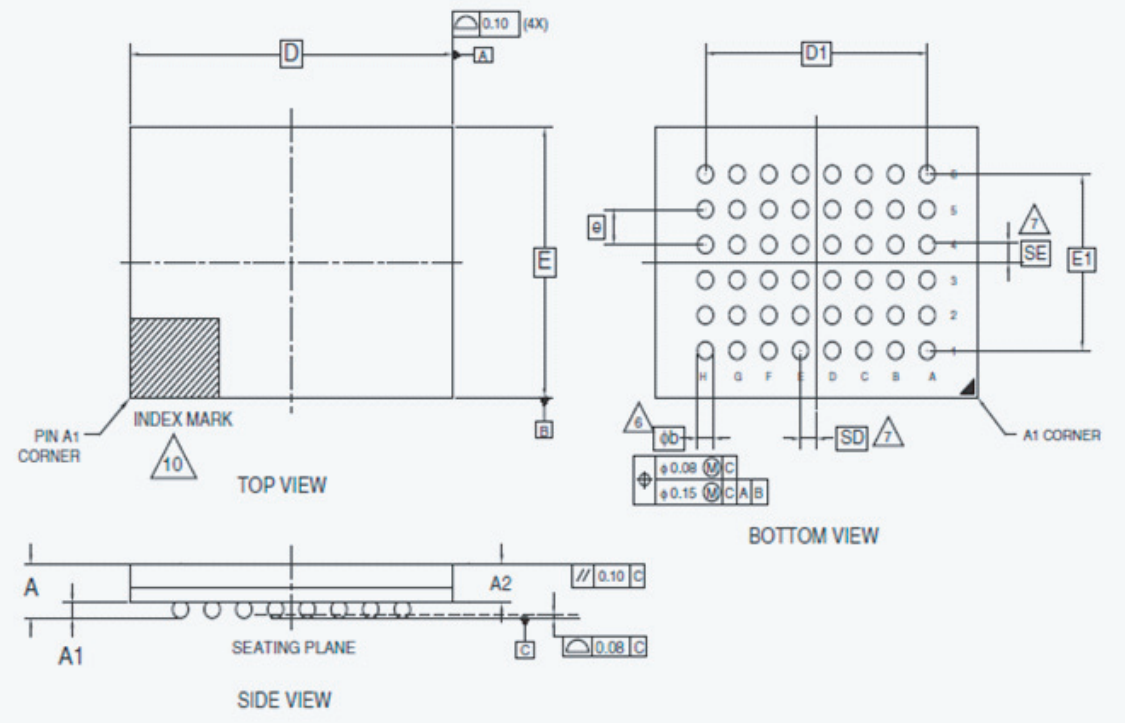


Figure 2. FBE063 Drawing (S29JL064H)

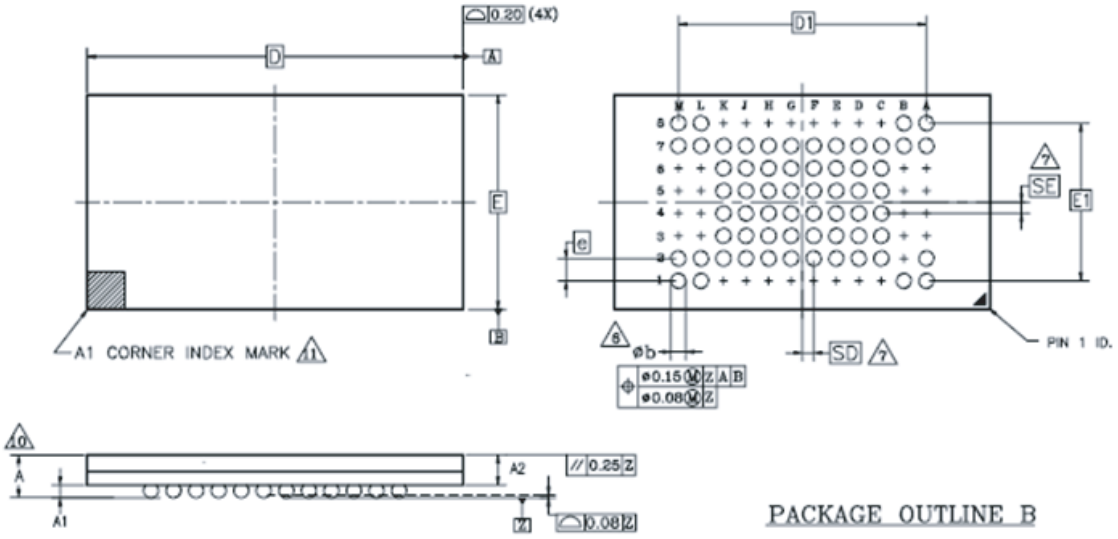


Table 6. VBN048 and VBK048 Package Dimensions

JEDEC Symbol	Parameter	VBK048 (S29JL032H, S29JL032J, S29JL064J)	FBE063 (S29JL064H)
A	Overall Thickness (max)	1.00 mm	1.20 mm
A1	Ball Height (min)	0.18 mm	0.20 mm
A2	Body Thickness (min)	0.62 mm	0.84 mm
A2	Body Thickness (max)	0.76 mm	0.94 mm
D	Body Length (BCS.)	8.15 mm	12.00 mm
E	Body Width (BCS.)	6.15 mm	11.00 mm
D1	Ball Footprint length (BCS.)	5.60 mm	8.80 mm
E1	Ball Footprint Width (BCS.)	4.00 mm	5.60 mm
MD	Row Matrix In D Dimension	8	12
ME	Column Matrix In E Dimension	6	8
N	Total Ball Count	48	63
fb	Ball Diameter (min)	0.35 mm	0.30 mm
fb	Ball Diameter (max)	0.43 mm	0.40 mm
e	Ball Pitch (BCS.)	0.80 mm	0.80 mm
SD / SE	Solder Ball Placement (BCS.)	0.40 mm	0.40 mm
	Depopulated Solder Balls	none	A3-A6, B2-B6, L3-L6, M3-M6, C1-K1, C8-K8

3. Conclusion

S29JL032H and S29JL064H can be replaced with architecturally compatible S29JL032J and S29JL064J models in most applications with minimal hardware, firmware, or software modifications. It is important that careful examination of the impact of all feature implementation, DC and AC specification, and mechanical differences be reviewed for each application when considering the impact of migration.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	08/13/2010	Initial version
*A	–	–	12/03/2010	Feature Comparison and Differences: High Level Feature Comparison table: Corrected VID entries. First Read after Power Reset: Added this section for CE# control during power up guidance.
*B	–	–	08/23/2011	Updated table: AC Specification Differences. Updated the Byte Program Time and Word Program Time for S29JL064J. First Read after Power Reset: Removed section. Multiple Sector Erase: Added new section.
*C	–	–	12/16/2011	Multiple Sector Erase: Corrected the sector erase time-out period from 80 µs to 50 µs.
*D	4981066	MSWI	12/22/2015	Updated in Cypress template

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