AN98584

Migration from Numonyx™ P33 to Cypress S29GL-S

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AN98584 describes how to convert a system design from Numonyx P33 to Cypress S29GL-P and S29GL-S.

Contents

1 Introduction

This application note describes how to convert a system design from Numonyx P33 to Cypress S29GL-P and S29GL-S. Understanding the basic difference of devices provides greater insight about the kinds of compatibility issues to consider when using Cypress devices to replace Numonyx devices.

This document assumes that customer is familiar with Cypress and Numonyx flash. It is based on information available in data sheet and other sources. Any specification changes to either device may not be reflected in this document.

2 Feature Comparison

Table 1 shows key parameter comparisons between P33 and S29GL-P/S.

Table 1. General Feature Comparison (Sheet 1 of 2)

Products	P33	S29GL-P	S29GL-S
Process Node	65 nm	90 nm	65 nm
Density			
128 Mbit	—	X	X
256 Mbit	—	X	X
512 Mbit	X	X	X
1024 Mbit	X	X	X
2048 Mbit	X (Multi-die)	X (Multi-die)	X (Multi-die)
Sector Architecture			
Boot (32 kB)	X	—	—
Uniform (128 kB)	X	X	X
Data Size	—	—	—
Bus Width	x16	x8/x16	x16

Table 1. General Feature Comparison (Sheet 2 of 2)

Products	P33	S29GL-P	S29GL-S
Read Page	32 Byte	16 Byte	32 Byte
Write Buffer	1024 Byte	64 Byte	512 Byte
Packaging			
56-TSOP	X	X	X
64-BGA	Easy BGA	LAA064	LAE064
Other			
Synchronous	X	—	—
Asynchronous	X	X	X
OTP Area	2112 Bits	256 Byte	1024 Byte
Write Protect	X	X	X
Read Protect	X	—	X
Erase Suspend/Resume	X	X	X
Data Polling	X	X	X
Status Register	X	—	X
Accelerated Programming	X	X	—
Write Buffer Programming	X	X	X
Absolute write protection: $V_{PP}=V_{SS}$	X	—	—
Power-Transition erase/ program lockout	X	—	—
Individual zero-latency block locking	X	—	—
Individual block lock-down capability	X	—	—
Password access feature	X	X	X
EFI (Extended Function Interface)	X	—	—

2.1 Density

The P33 family is available in monolithic 512 and 1024 Mb only; 2048 Mb is two 1024 Mb dies. The S29GL-P/GL-S family is available in monolithic 128, 256, 512, and 1024 Mb densities; 2048 Mb density is a same-die-stack package consisting of two 1024 die whose access is controlled by address input A27.

2.2 Sector Architecture

The GL-P and GL-S families have 128 kB uniform sectors while the P33 family has 128 kB uniform and 4 kB boot sectors. Modifications are required if software was structured to the P33 boot sector architecture.

2.3 Data Bus Width

S29GL-P has x8/x16 selectable data bus width. BYTE# input is pulled high, the device will operate with a 16-bit wide data bus. When BYTE# is pulled low, the device will operate with an 8-bit data bus. If the device is always used in Byte mode, it is recommended to pull the unused data bus I/O (DQ[15:8]) to high or low via a resistor on the PCB, to minimize noise injection and power consumption on the unused inputs.

The S29GL-S only supports x16 data bus width. The BYTE# input on previous generations of MirrorBit® GL devices (pin 53 on 56-TSOP and pad F7 on 64-BGA) will be reserved for future use on the S29GL-S. The BYTE# input on existing designs should be pulled high to force operation in x16 data mode to enable migration to the S29GL-S.

The P33 has the same data bus width as GL-S.

2.4 Read Page Size

The S29GL-S has a 32-byte (16 words) read page buffer, which is double the depth of S29GL-P to facilitate larger processor cache line fill operations. No software modifications are required to operate with 16-byte maximum page transfers supported by S29GL-P. Software can be modified to take advantage of the deeper read page buffer on the S29GL-S by querying the CFI programming buffer depth register at address 4Ch (x16 address bus reference) and configuring software to perform additional page read cycles.

The P33 has the same read page buffer as GL-S.

2.5 Write Buffer Size

The S29GL-S has a 512-byte (256 words) write buffer, eight times the depth of the existing S29GL-P. No software modifications are required to continue use of a 64-byte write buffer fill supported by the S29GL-P. Software can be modified to take advantage of the deeper write buffers by querying the CFI programming buffer depth register at address 2Ah (x16 address bus reference) and configuring software to perform larger buffer fills.

The P33 has a 1024-byte (512 words), two times the depth of the existing GL-S. Software modifications might be required to replace P33 with GL-S.

2.6 Synchronous Mode

The GL-P and GL-S devices do not support the synchronous mode operation while the P33 does.

2.7 Asynchronous Mode

All the devices support asynchronous mode. The S29GL-S supports asynchronous single and page read modes, consistent with the S29GL-P. Software can be modified to take advantage of the wider read page buffer on the S29GL-S by querying the CFI programming buffer depth register at address 98h (x8 address bus reference) or 4Ch (x16 address bus reference) and configuring software to perform additional page read cycles.

2.8 OTP Area

The GL-P has 256-byte one time programmable Secure Silicon areas and GL-S has 1024-byte. The P33 has 2112 bits.

2.9 Write and Erase Protection

The P33 supports Write Protection through block locking that has a different method than the GL-P/GL-S. The S29GL-S supports Advanced Sector Protection (ASP) program and erase protection via single voltage, password, non-volatile and volatile control, consistent with S29GL-P. Details of ASP program and erase protection implementations can be found in the S29GL-P and S29GL-S data sheets.

2.10 Read Protection

The P33 supports Read Protection through password access. The S29GL-S supports Advanced Sector Protection (ASP) read protection via a customer specific ordering option. The S29GL-P does not support read protection. Details of ASP read protection implementation can be found in the S29GL-S data sheets.

2.11 Erase Suspend and Resume

The P33 supports erase suspend and resume same as GL-S and GL-P.

2.12 Data Polling

All devices support data polling but the method is different.

The S29GL-S supports data polling to determine the status of embedded programming and erase operations; however, unlike S29GL-P, it does not support the legacy DQ3 erase time out indicator function. Applications that utilize DQ3 data polling to validate multi-sector erase command acceptance will require modification. Additionally, DQ0 now provides an indication to system software when a Write-To-Buffer-Abort-Reset command can be issued. This command can only be accepted when DQ0 is high following an incorrect write buffer load sequence or when status register bit DQ7 is high indicating no embedded algorithms are active. System software may require modification to accommodate this change.

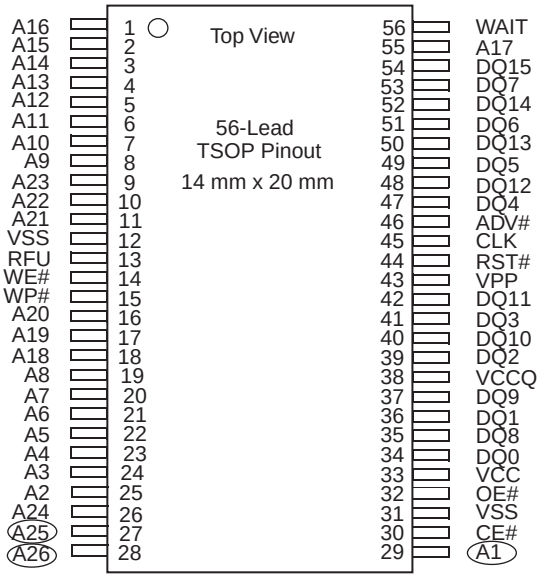
2.13 Accelerated Programming

The P33 and GL-P support accelerated programming while the GL-S does not support accelerated programming. The maximum voltage that should be applied to the WP#/(ACC) input is V_{CC} + 0.5V.

3 Package Comparison

There are different pinouts and ballouts between P33 and GL-P/GL-S regarding TSOP and BGA, as show in Figure 1 and Figure 2, and Figure 3 and Figure 4.

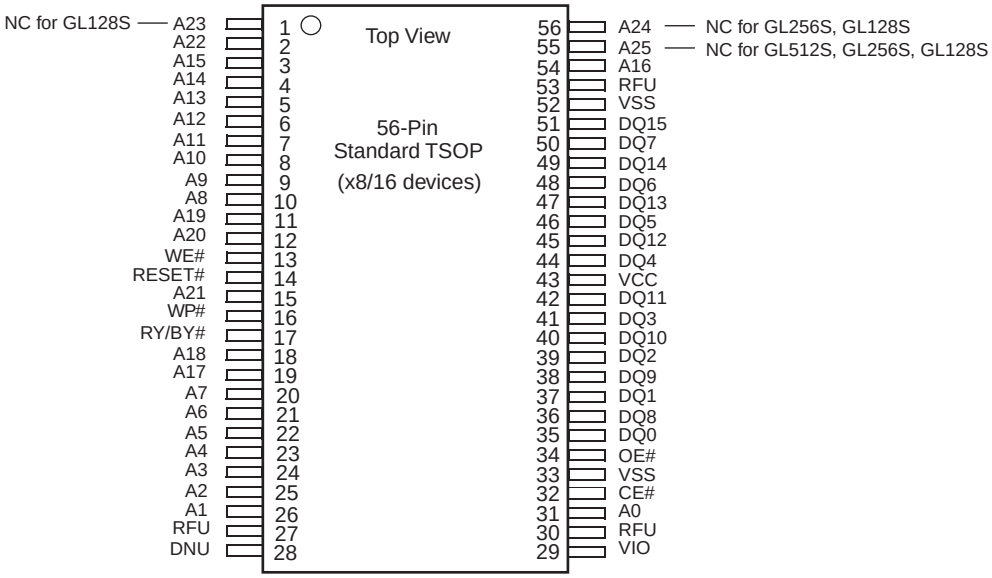
Figure 1. P33 56-Lead TSOP



Notes:

1. *A1 is the least significant address bit.*
2. *ADV# must be tied to V_{SS} or driven to low throughout the asynchronous read mode.*
3. *A25 is valid for 512-Mbit densities and above; otherwise, it is a no connect (NC).*
4. *A26 is valid for 1-Gbit density and above; otherwise, it is a no connect (NC).*
5. *One dimple on package denotes Pin 1, which will always be in the upper left corner of the package, in reference to the product mark.*

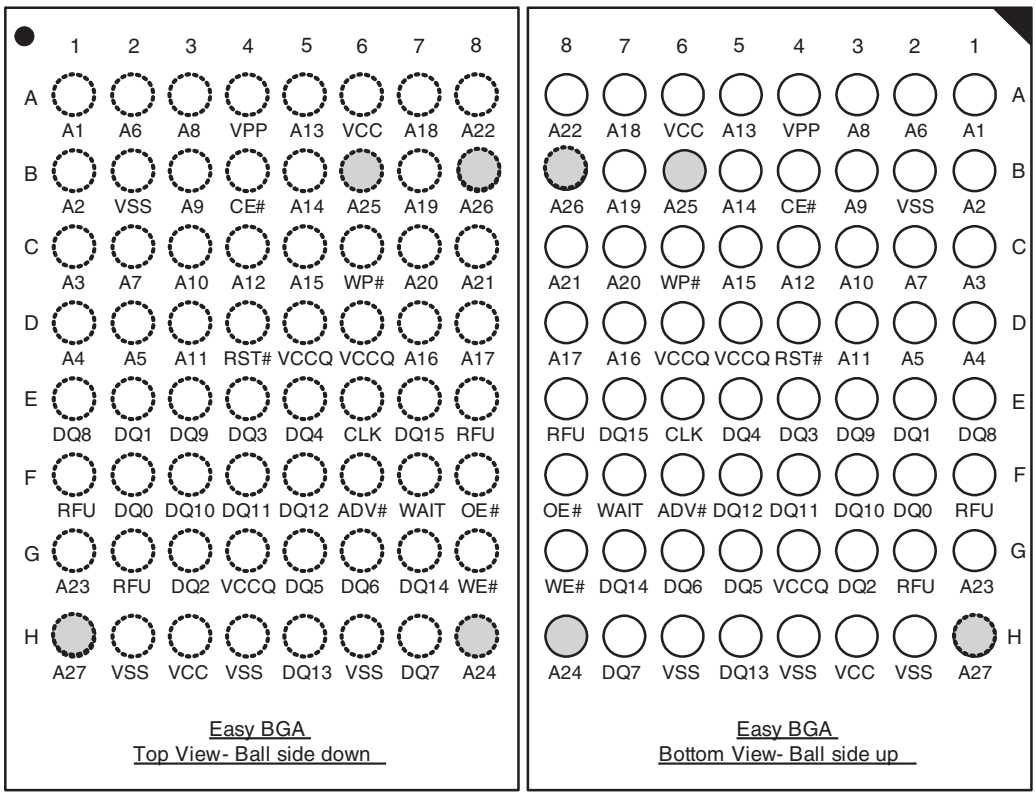
Figure 2. GL-P/GL-S 56-Lead TSOP



Notes:

1. *Pin 28 Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels.*
2. *Pins 27, 30, and 53 Reserved for Future Use (RFU).*

Figure 3. P33 64-Ball Easy BGA Ballouts

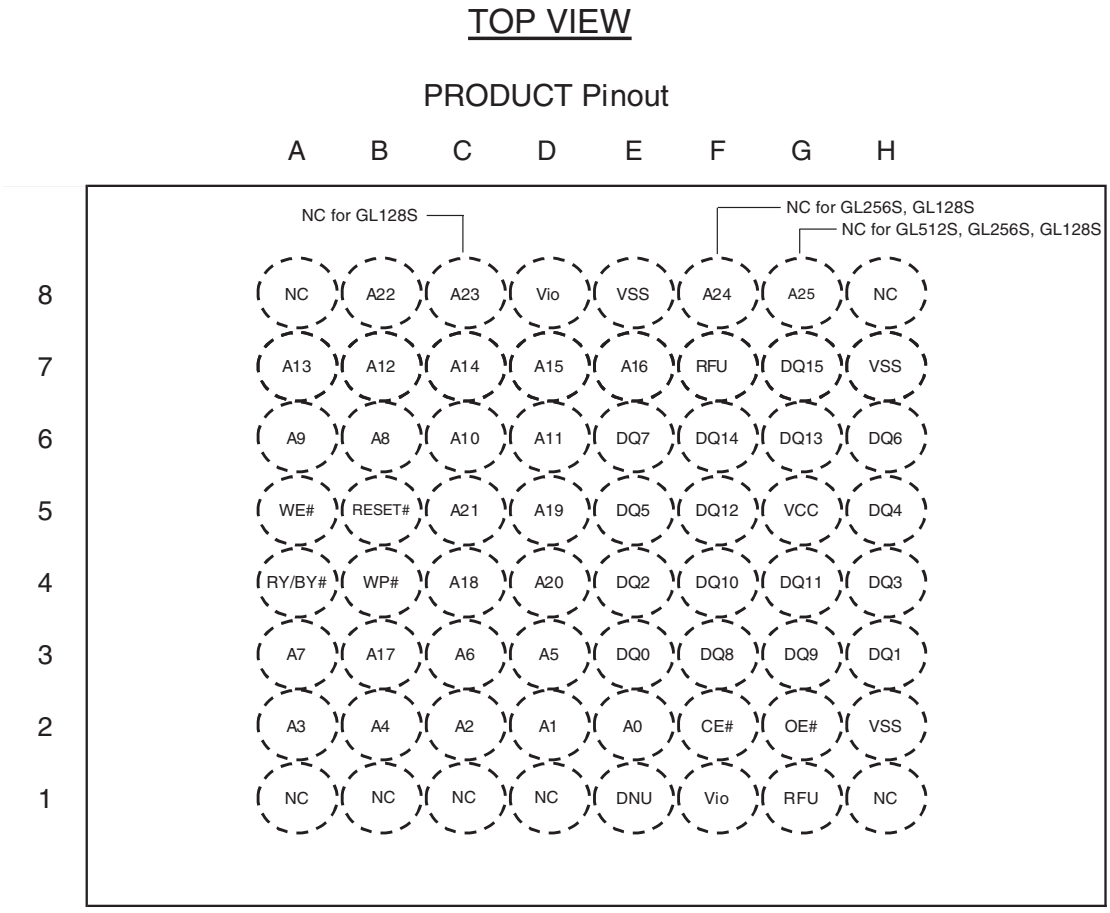


Notes:

1. *A1 is the least significant address bit.*
2. *A25 is valid for 512-Mbit densities and above; otherwise, it is a no connect (NC).*
3. *A26 is valid for 1-Gbit densities and above; otherwise, it is a no connect (NC).*

4. *A27 is valid for 2-Gbit density; otherwise, it is a no connect (NC).*
5. *One dimple on package denotes A1 Pin, which will always be in the upper left corner of the package, in reference to the product mark.*

Figure 4. GL-S 64-Ball BGA Ballouts



Notes:

1. *Ball E1, Do Not Use (DNU), a device internal signal is connected to the package connector. The connector may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Do not use these connections for PCB Signal routing channels.*
2. *Balls F7 and G1, Reserved for Future Use (RFU).*
3. *Balls A1, A8, C1, D1, H1, and H8, No Connect (NC).*

4 Signal Comparison

Cypress GL-P/S pin configuration is different from Numonyx P33, as shown in Table 2.

Table 2. Signal Comparison (Sheet 1 of 2)

P33		GL-P/GL-S	
Symbol	**Description**	**Symbol**	**Description**
A[27:1]	Address Inputs for 2048 Mb A25-A1 for 512 Mb A26-A1 for 1024 Mb	A25-A0	Address Inputs for 1024 Mb A24-A0 for 512 Mb A23-A0 for 256 Mb A22-A0 for 128 Mb
ADV#	Address Valid Input	—	—
DQ[15:0]	Data Input/Output	DQ14-DQ0	Data Lines for GL-P (GL-S: DQ15-DQ0)
—	—	DQ15/A-1	Data Lines for GL-P (GL-S: Not Support)
CLK	Clock Input	—	—

Table 2. Signal Comparison (Sheet 2 of 2)

P33		GL-P/GL-S	
Symbol	**Description**	**Symbol**	**Description**
WAIT	Wait Output	—	—
CE#	Chip Enable	CE#	Chip Enable
OE#	Output Enable	OE#	Output Enable
RST#	Reset Input	RST#	Reset Input
WE#	Write Enable	WE#	Write Enable
WP#	Write Protection	WP#	Write Protection
VPP	Erase and Program Power	ACC	Programming Acceleration (GL-S: Not Support)
VCC	Device Power Supply	VCC	Device Power Supply
VCCQ	Output Power Supply	VIO	Versatile IO Power Supply
VSS	Ground	VSS	Ground
RFU	Reserved for Further Use	RFU	Reserved for Further Use
DU	Do Not Use	DNU	Do Not Use
NC	No Connect	NC	No Connect
—	—	RY/BY#	Ready/Busy Output-Open Drain
—	—	BYTE#	Data Bus Width for GL-P (GL-S: Not Support)

5 Command Set Comparison

For comparison, Cypress device commands vary from two to six bus cycles while Numonyx's commands from one to two bus cycles, as shown in Table 3, Table 4, and Table 5.

Table 3. P33 Command Set (Sheet 1 of 2)

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	**Addr** (1)	**Data** (2)	**Oper**	**Addr** (1)	**Data** (2)
Read	Read Array	1	Write	DnA	0xFF			
	Read Device Identifier	≥ 2	Write	DnA	0x90	Read	DBA + IA	ID
	Read CFI	≥ 2	Write	DnA	0x98	Read	DBA + CFI-A	CFI-D
	Read Status Register	2	Write	DnA	0x70	Read	DnA	SRD
	Clear Status Register	1	Write	DnA	0x50			
Program	Word Program	2	Write	WA	0x40	Write	WA	WD
	Buffered Program(3)	> 2	Write	WA	0xE8	Write	WA	N - 1
	Buffered Enhanced Factory Program (BEFP) (4)	> 2	Write	WA	0x80	Write	WA	0xD0
Erase	Block Erase	2	Write	BA	0x20	Write	BA	0xD0
Suspend	Program/Erase Suspend	1	Write	DnA	0xB0			
	Program/Erase Resume	1	Write	DnA	0xD0			
Protection	Block Lock	2	Write	BA	0x60	Write	BA	0x01
	Block Unlock	2	Write	BA	0x60	Write	BA	0xD0
	Block Lock-down	2	Write	BA	0x60	Write	BA	0x2F
	Program OTP Register	2	Write	OTP-RA	0xC0	Write	OTP-RA	OTP-Data
	Program Lock Register	2	Write	LRA	0xC0	Write	LRA	LRD
Configuration	Configure Read Configuration Register	2	Write	RCD	0x60	Write	RCD	0x03

Table 3. P33 Command Set (Sheet 2 of 2)

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr (1)	Data (2)	Oper	Addr (1)	Data (2)
Blank Check	Block Blank Check	2	Write	BA	0xBC	Write	BA	D0
EFI	Extended Function Interface command (5)	>2	Write	WA	0xEB	Write	WA	Sub-Op code

Notes:

1. *First command cycle address should be the same as the operations target address.*
   DBA = Device Base Address.(needed for dual-die 2-Gbit device.)
   DnA = Address within the device.
   IA = Identification code address offset.
   CFI-A = Read CFI address offset.
   WA = Word address of memory location to be written.
   BA = Address within the block.
   OTP-RA = OTP Register address.
   LRA = Lock Register address.
   RCD = Read Configuration Register data on A[16:1].
2. *ID = Identifier data.*
   CFI-D = CFI data on DQ[15:0].
   SRD = Status Register data.
   WD = Word data.
   N = Word count of data to be loaded into the write buffer.
   OTP-D = OTP Register data.
   LRD = Lock Register data.
3. *The second cycle of the Buffered Program Command is the word count of the data to be loaded into the write buffer. This is followed by up to 512 words of data. Then the confirm command (0xD0) is issued, triggering the array programming operation.*
4. *The confirm command (0xD0) is followed by the buffer data.*
5. *The second cycle is a Sub-Op-Code, the data written on third cycle is N-1; 1 . N . 512. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved, after the data words are loaded, the final cycle is the confirm cycle 0xD0).*

Table 4. GL-P Command Set (Sheet 1 of 2)

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	6	555	AA	2AA	55	555	90	X01	227E	X0E		X0F	
	Sector Protect Verify (8)	4	555	AA	2AA	55	555	90	[SA]X02	(8)				
	Secure Device Verify (9)	4	555	AA	2AA	55	555	90	X03	(9)				
CFI Query (10)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (11)		6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
Program Buffer to Flash (Confirm)		1	SA	29										
Write-to-Buffer-Abort Reset (12)		3	555	AA	2AA	55	555	F0						
Unlock Bypass	Enter	3	555	AA	2AA	55	555	20						
	Program (13)	2	XXX	A0	PA	PD								
	Sector Erase (13)	2	XXX	80	SA	30								
	Chip Erase (13)	2	XXX	80	XXX	10								
	Reset (14)	2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30

Table 4. GL-P Command Set (Sheet 2 of 2)

Command (Notes)	Cycles	Bus Cycles (Notes 1–4)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Erase Suspend/Program Suspend (15)	1	XXX	B0										
Erase Resume/Program Resume (16)	1	XXX	30										
Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88						
Secured Silicon Sector Exit (17)	4	555	AA	2AA	55	555	90	XX	00				

Legend:

X = Don't care.

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same write buffer page as PA.

WC = Word Count is the number of write buffer locations to load minus 1.

Notes:

1. *All values are in hexadecimal.*
2. *All bus cycles are write cycles unless otherwise noted.*
3. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
4. *Address bits AMAX:A16 are don't cares for unlock and command cycles, unless SA or PA required. (AMAX is the Highest Address pin.).*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
7. *The fourth, fifth, and sixth cycles of the autoselect command sequence are read cycles.*
8. *The data is 00h for an unprotected sector and 01h for a protected sector. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
9. *The data value for DQ7 is "1" for a serialized, protected Secured Silicon Sector region and "0" for an unserialized, unprotected region.*
10. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
11. *Depending on the number of words written, the total number of cycles may be from 6 to 37.*
12. *Command sequence returns device to reading array after being placed in a Write-to-Buffer-Abort state. Full command sequence is required if resetting out of abort while in Unlock Bypass mode.*
13. *The Unlock-Bypass command is required prior to the Unlock-Bypass-Program command.*
14. *The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
15. *The system can read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
17. *The Exit command returns the device to reading the array.*

Table 5. GL-S Command Set (Sheet 1 of 3)

Command Sequence	Cycles	Bus Cycles (Notes 1-4)													
		First		Second		Third		Fourth		Fifth		Sixth		Seventh	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)	1	RA	RD												
Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												
Status Register Read	2	555	70	XXX	RD										
Status Register Clear	1	555	71												
Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)	1	SA	29												

Table 5. GL-S Command Set (Sheet 2 of 3)

Command Sequence		Cycles	Bus Cycles (Notes 1-4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Write-to-Buffer-Abort Reset (Note 10)		3	555	AA	2AA	55	555	F0								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend/Program Suspend Legacy Method (Note 8) Erase Suspend Enhanced Method		1	XXX	B0												
Erase Resume/Program Resume Legacy Method (Note 9) Erase Resume Enhanced Method		1	XXX	30												
Program Suspend Enhanced Method		1	XXX	51												
Program Resume Enhanced Method		1	XXX	50												
Blank Check		1	(SA) 555	33												
ID-CFI (Autoselect) ASO	ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90								
	CFI Enter (Note 7)	1	(SA) 55	98												
	ID-CFI Read	1	XXX	RD												
	Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												
Secure Silicon Region Command Definitions																
Secure Silicon Region (SSR) ASO	SSR Entry	3	555	AA	2AA	55	(SA) 555	88								
	Read (Note 5)	1	RA	RD												
	Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset (Note 10)	3	555	AA	2AA	55	555	F0								
	SSR Exit (Note 10)	4	555	AA	2AA	55	555	90	XX	0						
	Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												
Lock Register Command Set Definitions																
Lock Register ASO	Lock Register Entry	3	555	AA	2AA	55	555	40								
	Program (Note 14)	2	XXX	A0	XXX	PD										
	Read (Note 14)	1	0	RD												
	Command Set Exit (Notes 11, 15)	2	XXX	90	XXX	0										
	Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												

Table 5. GL-S Command Set (Sheet 3 of 3)

Command Sequence		Cycles	Bus Cycles (Notes 1-4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Password Protection Command Set Definitions																
Password ASO	Password ASO Entry	3	555	AA	2AA	55	555	60								
	Program (Note 13)	2	XXX	A0	PWAx	PWDx										
	Read (Note 12)	4	0	PWD 0	1	PWD 1	2	PWD 2	3	PWD 3						
	Unlock	7	0	25	0	3	0	PWD 0	1	PWD 1	2	PWD 2	3	PWD 3	0	29
	Command Set Exit (Notes 11, 15)	2	XXX	90	XXX	0										
	Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												
Non-Volatile Sector Protection Command Set Definitions																
PPB (Non-Volatile Sector Protection)	PPB Entry	3	555	AA	2AA	55	555	C0								
	PPB Program (Note 16)	2	XXX	A0	SA	0										
	All PPB Erase (Note 16)	2	XXX	80	0	30										
	PPB Read (Note 16)	1	SA	RD (0)												
	Command Set Exit (Notes 11, 15)	2	XXX	90	XXX	0										
	Reset/ASO Exit (Notes 6, 15)	1	XXX	F0												
Global Non-Volatile Sector Protection Freeze Command Set Definitions																
PPB Lock Bit	PPB Lock Entry	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Cleared	2	XXX	A0	XXX	0										
	PPB Lock Status Read (Note 16)	1	XXX	RD (0)												
	Command Set Exit (Notes 11, 15)	2	XXX	90	XXX	0										
	Reset/ASO Exit (Note 15)	1	XXX	F0												
Volatile Sector Protection Command Set Definitions																
DYB (Volatile Sector Protection) ASO	DYB ASO Entry	3	555	AA	2AA	55	555	E0								
	DYB Set (Note 16)	2	XXX	A0	SA	0										
	DYB Clear (Note 16)	2	XXX	A0	SA	1										
	DYB Status Read (Note 16)	1	SA	RD (0)												
	Command Set Exit (Notes 11, 15)	2	XXX	90	XXX	0										
	Reset/ASO Exit (Note 15)	1	XXX	F0												

Legend:

X = Don't care.
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed.
PD = Data to be programmed at location PA.

SA = Address of the sector selected. Address bits A_{MAX}-A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same Line.
WC = Word Count is the number of write buffer locations to load minus 1.
PWAx = Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h.
PWDx = Password data word0, word1, word2, and word3.

Notes:
1. *All values are in hexadecimal.*
2. *Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Secure Silicon Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.*
3. *Data bits DQ15-DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.*
4. *Address bits A_{MAX}-A11 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the ID-CFI (autoselect) mode, or if DQ5 goes High (while the device is providing status data).*
7. *Command is valid when device is ready to read array data or when device is in ID-CFI (autoselect) mode.*
8. *The system can read and program/program suspend in non-erasing sectors, or enter the ID-CFI ASO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
9. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
10. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. IMPORTANT: the full command sequence is required if resetting out of ABORT.*
11. *The Exit command returns the device to reading the array.*
12. *The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
13. *For PWDx, only one portion of the password can be programmed per each A0 command. Portions of the password must be programmed in sequential order (PWD0 - PWD3).*
14. *All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future use are undefined and may be 0's or 1's.*
15. *If any of the Entry commands was issued, an Exit command must be issued to reset the device into read mode.*
16. *Protected State = 00h, Unprotected State = 01h. The sector address for DYB set, DYB clear, or PPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.*

6 Device ID Comparison

Table 6 and Table 7 show the device ID of each device.

Table 6. P33 Device ID

ID Code Type	Device Density	Device Identifier Codes		
		-T (Top Parameter)	-B (Bottom Parameter)	-E (Symmetrical Blocks)
Device Code	512-Mbit	8964	8965	899E
	1-Gbit	8966	8967	899F

Note:
1. *The 2-Gbit devices do not have a unique Device ID associated with them. Each die within the stack can be identified by the ID codes.*

Table 7. GL-P/GL-S Device ID (Sheet 1 of 2)

Description	Address	Read Data (word/byte mode)
Manufacturer ID	Base + 00h	xx01h/1h
Device ID, Word 1	Base + 01h	227Eh/7Eh
Device ID, Word 2	Base + 0Eh	2248h/48h (GL02GS) 2228h/28h (GL01GP/S) 2223h/23h (GL512P/S) 2222h/22h (GL256P/S) 2221h/21h (GL128P/S)
Device ID, Word 3	Base + 0Fh	2201h/01h

Table 7. GL-P/GL-S Device ID (Sheet 2 of 2)

Description	Address	Read Data (word/byte mode)
Secure Device Verify	Base + 03h	For S29GLxxxPH: XX19h/19h = Not Factory Locked. XX99h/99h = Factory Locked For S29GLxxxPL: XX09h/09h = Not Factory Locked. XX89h/89h = Factory Locked
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

7 Status Register Comparison

Table 8 and Table 9 show the status register of each device.

Table 8. P33 Status Register

Status Register (SR)							Default Value = 0x80
Device Write Status	Erase Suspend Status	Erase Status	Program Status	VPP Status	Program Suspend Status	Block-Locked Status	BEFP Write Status
DWS	ESS	ES	PS	VPPS	PSS	BLS	BWS
7	6	5	4	3	2	1	0

Bit	Name	Description
7	Device Write Status (DWS)	0 = Device is busy; program or erase cycle in progress; SR.0 valid. 1 = Device is ready; SR[6:1] are valid.
6	Erase Suspend Status (ESS)	0 = Erase suspend not in effect. 1 = Erase suspend in effect.
5	Erase Status (ES)	SR.5 / SR.4 / Description
4	Program Status (PS)	Command Sequence Error 0 / 0 / Program or Erase operation successful. 0 / 1 / Program error - operation aborted. 1 / 0 / Erase error - operation aborted. 1 / 1 / Command sequence error - command aborted.
3	VPP Status (VPPS)	0 = V_{PP} within acceptable limits during program or erase operation. 1 = $V_{PP} \leq V_{PPLK}$ during program or erase operation.
2	Program Suspend Status (PSS)	0 = Program suspend not in effect. 1 = Program suspend in effect.
1	Block-Locked Status (BLS)	0 = Block not locked during program or erase. 1 = Block locked during program or erase; operation aborted.
0	BEFP Write Status (BWS)	After Buffered Enhanced Factory Programming (BEFP) data is loaded into the buffer: 0 = BEFP complete. 1 = BEFP in-progress.

Notes:

1. *Always clear the Status Register prior to resuming erase operations. It avoids Status Register ambiguity when issuing commands during Erase Suspend. If a command sequence error occurs during an erase-suspend state, the Status Register contains the command sequence error status (SR[7,5,4] set). When the erase operation resumes and finishes, possible errors during the erase operation cannot be detected via the Status Register because it contains the previous error status.*
2. *BEFP mode is only valid in array blocks.*

Table 9. GL-S Status Register (Sheet 1 of 2)

Bit #	15:8	7	6	5	4	3	2	1	0
Bit Description	Reserved	Device Ready Bit	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	Write Buffer Abort Status Bit	Program Suspend Status Bit	Sector Lock Status Bit	Reserved
Bit Name		DRB	ESSB	ESB	PSB	WBASB	PSSB	SLSB	
Reset Status	X	1	0	0	0	0	0	0	0

Table 9. GL-S Status Register (Sheet 2 of 2)

Bit #	15:8	7	6	5	4	3	2	1	0
Busy Status	Invalid	0	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Ready Status	X	1	0=No Erase in Suspension 1=Erase in Suspension	0=Erase successful 1=Erase fail	0=Program successful 1=Program fail	0=Program not aborted 1=Program aborted during Write to Buffer command	0=No Program in suspension 1=Program in suspension	0=Sector not locked during operation 1=Sector locked error	X

Notes:

1. *Bits 15 thru 8, and 0 are reserved for future use and may display as 0 or 1. These bits should be ignored (masked) when checking status.*
2. *Bit 7 is 1 when there is no Embedded Algorithm in progress in the device.*
3. *Bits 6 thru 1 are valid only if Bit 7 is 1.*
4. *All bits are put in their reset status by cold reset or warm reset.*
5. *Bits 5, 4, 3, and 1 are cleared to 0 by the Clear Status Register command or Reset command.*
6. *Upon issuing the Erase Suspend Command, the user must continue to read status until DRB becomes 1.*
7. *ESSB is cleared to 0 by the Erase Resume Command.*
8. *ESB reflects success or failure of the most recent erase operation.*
9. *PSB reflects success or failure of the most recent program operation.*
10. *During erase suspend, programming to the suspended sector, will cause program failure and set the Program status bit to 1.*
11. *Upon issuing the Program Suspend Command, the user must continue to read status until DRB becomes 1.*
12. *PSSB is cleared to 0 by the Program Resume Command.*
13. *SLSB indicates that a program or erase operation failed because the sector was locked.*
14. *SLSB reflects the status of the most recent program or erase operation.*

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	07/07/2011	Initial version
*A	4981010	MSWI	10/22/2015	Updated in Cypress template
*B	5840666	AESATMP8	08/01/2017	Updated logo and Copyright.

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