AN98568

Migrating from S29AL032D to S29GL032N and S29JL032J

AN98568 discusses the specification differences that must be considered when migrating from the S29AL032D to either the S29GL032N or S29JL032J.

Contents

1 Feature Comparison and Differences

The S29GL032N and S29JL032J flash devices have feature sets which are supersets of the S29AL032D flash devices, see Table 1. As a result, many S29AL032D applications will directly support S29GL032N and S29JL032J devices with only minor hardware or software modifications.

Primary differences between these three flash devices are related to: data bus width, sector architectural options, multi-bank options enabling zero latency simultaneous read-while-write, write buffer programming capability, Secure Silicon Sector implementation, sector protection schemes, accelerated programming, Device ID implementation, DC and AC parameters, temperature operating range and packaging options.

In general, S29JL032J is the recommended migration path for those applications that require high performance read or programming support and/or minimal software modification, while the S29GL032N is the recommended migration path for those applications that require the most cost effective solution where lower programming throughput and/or software modifications are tolerable.

Table 1. High-Level Feature Comparison (Sheet 1 of 2)

Feature	S29AL032D	S29GL032N	S29JL032J
NOR Technology	Floating Gate	MirrorBit	Floating Gate
Process Node	200 nm	110 nm	110 nm
Array Size	4,194,304 bytes	4,194,304 bytes	4,194,304 bytes
Data Bus	x8 only or x8/x16	x8/x16	x8/x16
Boot Sector Model Architecture	8-8 kB, 63-64 kB	8-8 kB, 63-64 kB	8-8 kB, 63-64 kB
Uniform Sector Model Architecture	64-64 kB (1)	64-64 kB	64-64 kB
Sector Banks	1	1	2 or 4
Simultaneous Read-while-Write	no	no	yes
Asynchronous Read and/or Write	yes	yes	yes
Synchronous Read and/or Write	no	no	no
Speed Grade Options (TACC/TRC/TWC)	70, 90 ns	90, 110 ns	60, 70 ns
Read Page Mode	no	yes	no
Buffer Write Mode	no	yes	no
Read Page Size (maximum)	n/a	16 bytes	n/a
Write Page Size (minimum)	n/a	1 (2)	n/a
Write Page Size (maximum)	n/a	64 bytes	n/a

Table 1. High-Level Feature Comparison (Sheet 2 of 2)

Feature	S29AL032D	S29GL032N	S29JL032J
Total Secured Silicon (OTP) Area	256 bytes	256 bytes	256 bytes
User Lockable Secured Silicon (OTP) Area	256 bytes	256 bytes	128 bytes
JEDEC-compatible pin out	yes (3)	yes	yes
Ready/Busy output (RY/BY#)	yes	yes	yes
Hardware Reset input (RESET#)	yes	yes	yes
Accelerated Program input (WP#/ACC)	yes	yes	yes
Write Protect input (WP#/ACC)	yes	yes	yes
High Voltage Sector Protection	yes	no	yes
Advance Sector Protection	no	yes	no
Separate V_{IO} Input	no	yes (3)(5)	no
Autoselect/Sector Protection Voltage (V_{ID})	11.5 - 12.5V	11.5 - 12.5V	8.5 - 12.5V
Accelerated Programming Voltage (V_{HH})	11.5 - 12.5V	11.5 - 12.5V	8.5 - 9.5V
JEDEC-compatible software command set	yes	yes	yes
Autoselect Device ID read cycles	1 cycle	3 cycles	1 or 3 cycles
Common Flash Interface (CFI)	yes	yes	yes
Unlock Bypass Program command	yes	yes	yes
Erase Suspend/Resume commands	yes	yes	yes
Program Suspend/Resume commands	no	yes	no
Industrial Temperature (-40 to +85°C)	yes	yes	yes
Extended Temperature (-40 to +125°C)	yes	no	no
Program/Erase Cycle Endurance (typical)	1,000,000	100,000	1,000,000
Data Retention at 125°C (typical)	20 years	20 years	20 years
TSOP Package Option: 40-pin TS040	yes (4)	no	no
TSOP Package Option: 48-pin TS048	yes	yes (5)	yes
TSOP Package Option: 56-pin TS056	no	yes (6)	no
BGA Package Option: 48-ball VBK048	no	yes (5)	yes
BGA Package Option: 48-ball VBN048	yes	no	no
BGA Package Option: 64-ball LAA064	no	yes	no
BGA Package Option: 64-ball LAE064	no	yes	no

Notes:

1. *S29AL032D model 00 is x8 only.*
2. *If operating in x8 mode, units = 8-bit Byte; if operating in x16 mode, units = 16-bit Word.*
3. *S29GL032N models V1 and V2 support $V_{IO} < V_{CC}$.*
4. *TS040 pin out signal assignment is unique to S29AL032D model 00.*
5. *Applicable to S29GL032N models 03, 04.*
6. *Applicable to S29GL032N models 01, 02, V1, V2.*
7. *n/a = Not Applicable.*

1.1 Data Bus and Architectural Options

As illustrated in Table 2, the S29AL032D is available with a single bank architecture consisting of either a fixed x8 data bus with uniform 64 kB sectors (model 00) or a user configurable x8 or x16 data bus with a hybrid sector architecture consisting of 8 kB boot sectors and 64 kB uniform sectors with the boot sectors occupying either the top or bottom 64 kB of the flash array (models 03 and 04, respectively).

The S29GL032N is available with a single bank architecture that features a user configurable x8 or x16 data bus with either 64 kB uniform sectors (models 01, 02, V1, V2) or a hybrid sector architecture consisting of 8 kB boot sectors and 64 kB uniform sectors with the boot sectors occupying either the top or bottom 64 kB of the flash array (models 03 and 04, respectively).

The S29JL032H and S29JL032J are available with dual or quad bank boot sector architecture which enables zero latency simultaneous read-while-write operation. All models feature a user configurable x8 or x16 data bus. Dual bank devices (21, 22, 31, 32, 41, 42) are available with several bank size options, 4/28 Mbit, 8/24 Mbit or 16/16 Mbit, along with a hybrid sector array architecture consisting of 8 - 8 kB boot sectors and 64 kB uniform sectors. Consistent with the S29AL032D, the boot sectors occupying either the top or bottom 64 kB of the flash array. Quad bank devices (models 01, 02) feature two 12 Mbit blocks with 64 kB uniform sectors and two 4 Mbit blocks, one with 64 kB uniform sectors and the other with a hybrid sector architecture consisting of 8 kB boot sectors and 64 kB uniform sectors. Refer to Table 2 for model specific bank and sector architecture descriptions.

Table 2. Comparative Bus, Bank and Sector Architectures

Base Device	Model	Data Bus Width	Boot or Uniform Sectors	Bank Quantity	Bank Size and Orientation (Mbit)	Bank / Sector Architecture (SA0 - SAmax)
S29AL032D	00	x8	Uniform	1	32	64-64 kB
S29AL032D	03	x8 or x16	Boot	1	32	63-64 kB, 8-8 kB
S29AL032D	04	x8 or x16	Boot	1	32	8-8 kB, 63-64 kB
S29GL032N	01, V1 (1)	x8 or x16	Uniform	1	32	64-64 kB
S29GL032N	02, V2 (1)	x8 or x16	Uniform	1	32	64-64 kB
S29GL032N	03	x8 or x16	Boot	1	32	63-64 kB, 8-8 kB
S29GL032N	04	x8 or x16	Boot	1	32	8-8 kB, 63-64 kB
S29JL032J	01	x8 or x16	Boot	4	4 / 12 / 12 / 4	8-64 kB / 24-64 kB / 24-64 kB / 7-64 kB, 8-8 kB
S29JL032J	02	x8 or x16	Boot	4	4 / 12 / 12 / 4	8-8 kB, 7-64 kB / 24-64 kB / 24-64 kB / 8-64 kB
S29JL032J	21	x8 or x16	Boot	2	28 / 4	56-64 kB / 7-64 kB, 8-8 kB
S29JL032J	22	x8 or x16	Boot	2	4 / 28	8-8 kB, 7-64 kB / 56-64 kB
S29JL032J	31	x8 or x16	Boot	2	24 / 8	48-64 kB / 15-64 kB, 8-8 kB
S29JL032J	32	x8 or x16	Boot	2	8 / 24	8-8 kB, 15-64 kB / 48-64 kB
S29JL032J	41	x8 or x16	Boot	2	16 / 16	32-64 kB / 31-64 kB, 8-8 kB
S29JL032J	42	x8 or x16	Boot	2	16 / 16	8-8 kB, 31-64 kB / 32-64 kB

Note:

1. *S29GL032N models V1 and V2 support $V_{IO} < V_{CC}$.*

When migrating from S29AL032D to either S29GL032N or S29JL032J, software changes will be minimized when using models with the same sector architecture, e.g. S29AL032D model 03 top boot devices would readily migrate to either the S29GL032N model 03 top boot devices or any of the dual bank S29JL032J models 21, 31 or 41.

1.2 Simultaneous Read-while-Write

The multi-bank feature of the S29JL032J enables simultaneous read-while-write (simul-op) which allows a system to read with zero command latency from any location in the flash that is not within a bank that has an active embedded program or erase operation. Without this flash hardware feature, a system would have to either wait for the embedded operation to complete or suspend the embedded operation prior to performing a read to another location in the flash array. Use of this feature is optional and no software changes are required to accommodate the multi-bank feature of the S29JL032J in systems designed to support the single bank operation supported by the S29AL032D.

1.3 Secured Silicon Sector Region

The S29AL032D, S29GL032N and S29JL032J all have 256 bytes of one time programmable (OTP), unlimited times readable memory that is located outside of the NOR flash array. This region is accessed via a special access mode and is over laid in the Sector SA0 address space. By default, the Secured Silicon Sector region is erased and unlocked when shipped and is available for the user to program and subsequently lock.

Factory programming of the Secured Silicon Sector region with ESN and/or user supplied data is a custom ordering option for all Secured Silicon Sector enabled devices. Following factory Secured Silicon Sector programming of the S29AL032D or S29GL032N, the entire 256 byte Secured Silicon Sector region will be locked prior to shipment and a lock status bit only programmable by Cypress is set to prevent cloning. For factory

Secured Silicon Sector programming of the S29JL032J, only the lower 128 bytes of the Secured Silicon Sector region will be programmed and locked. The upper 128 bytes of the S29JL032J Secured Silicon Sector region will remain available to the user to program and lock.

When an Autoselect Secured Silicon Sector Lock Status read is performed, DQ7 set will indicate the factory lockable Secured Silicon Sector region was factory locked for the S29AL032D, S29GL032N and S29JL032J. DQ6 set will indicate that the user lockable Secured Silicon Sector region was locked by the user for the S29JL032J. There is no Autoselect Secured Silicon Sector Lock Status read value to indicate if the S29AL032D or S29GL032N was user locked.

1.4 Sector Protection Schemes

The S29AL032D, S29GL032N and S29JL032J boot sector models all support a static WP# enabled hardware outlying sector protection feature. On models with boot sectors at either the top or bottom of the array, the two outlying 8 kB sectors are protected when WP# is at or below V_{IL}. On the uniform sector S29GL032N models either the highest or lowest 64 kB sector is protected when WP# is at or below V_{IL}. The uniform sector S29AL032D model 00 does not support the WP# feature so the WP# input pin on replacement S29GL032N and S29JL032J devices must be controlled greater than V_{IL} to assure outlying sector(s) are not hardware protected.

The S29AL032D and S29JL032J support a sector group protection scheme which requires high voltage application to alter sector protection states. The functional difference between the S29AL032D and S29JL032J sector group protection implementation relates to high voltage input levels. The S29AL032D requires application of a V_{ID} super voltage in the range of 11.5 to 12.5V to RESET# to alter sector group protection and temporary unprotect all sectors. The S29JL032J supports a wider V_{ID} range of 8.5 to 12.5V. No changes are required to accommodate this wider allowable V_{ID} range when migrating from S29AL032D to S29JL032J.

The S29GL032N does not support the high voltage sector group protection scheme. It alternatively supports Cypress's more elaborate Advanced Sector Protection scheme which enables password, persistent and dynamic protection of individual sectors without having to switch high voltage into the flash. Details of this superset feature are discussed in the S29GL032N Data Sheet and the Cypress Advanced Sector Protection Application Note. If sector group protection is utilized on existing systems, migration to the S29GL032N will require software changes and potentially hardware changes to accommodate sector protection utilizing the Advanced Sector Protection scheme.

1.5 Buffer Programming

The S29GL032N supports two methods of programming, the legacy single datum programming method which utilizes the standard single byte/word programming command supported by the S29AL032D, as well as a parallel programming method utilizing new write buffer programming commands which allow up to 32B to be programmed in parallel. To maximize the programming throughput of the S29GL032N it is strongly recommended that support for write buffer programming be incorporated into system software. A full description of the new write buffer feature and commands can be found in the S29GL032N Data Sheet.

1.6 Accelerated Programming

The S29AL032D, S29GL032N and S29JL032J all support an accelerated programming via the application of a V_{HH} super voltage to the ACC input. The S29AL032D and S29GL032N require V_{HH} between 11.5 - 12.5V while the S29JL032J requires V_{HH} between 8.5 and 9.5V. The accelerated programming feature is primarily used on stand alone programming equipment so the V_{HH} incompatibility between the S29AL032D and S29JL032J devices will likely not pose a migration issue. If accelerated programming is implemented in-system, the switching V_{HH} circuit will require modification to prevent application of greater than 9.5V to the WP#/ACC input on the S29JL032J.

1.7 Autoselect Device ID

All S29AL032D models and dual bank S29JL032J models utilize a compatible single word Autoselect Device ID read operation. The S29JL032H and S29JL032J devices have common Device IDs for each model. In the subset of systems that query flash Device ID, system software will require minor modification to enable migration from the S29AL032D to S29JL032H or S29JL032J dual bank models because the S29AL032D Device IDs are unique to those family models. Refer to Table 3 for specific model Device IDs.

All S29GL032N models and quad bank S29JL032H models utilize a three word Autoselect Device ID read operation. The change from single to three byte Device ID was implemented on all new Cypress flash families

starting circa 2003 to accommodate identification of greater than 255 unique Cypress flash devices. Software can be enabled to either single or three byte Device ID determination by modifying the Device ID determination operation to the following flow:

1. Enter Autoselect mode (2 unlock write cycles followed by Autoselect Mode entry write cycle of 90h to flash base address)
2. Read x16 at address offset 1h (if returned value is 22FEh, go to step 3, else the returned value is the single-byte Device ID)
3. Read x16 address offsets 0Eh and 0Fh (the returned values appended to the previously read 22FEh make up the unique three-byte Device ID).
4. Write 0Fh to flash base address to exit Autoselect Mode and return to Read from Array mode.

Additional information regarding multi-byte Device ID implementation can be found in the S29GL032N and S29JL032J data sheets and the Migrating from Single-byte to Three-byte Device IDs Application Note.

Autoselect registers can be accessed via software commands or via a high voltage method which requires input of V_{ID} onto RESET#. The S29AL032D and S29GL032N require V_{ID} in the range of 11.5 to 12.5V. The S29JL032J allows V_{ID} in the wider range of 8.5 to 12.5V. No changes are required to accommodate this wider allowable V_{ID} range when migrating from S29AL032D to S29JL032J.

Querying of the flash Device ID is not a system software requirement so this feature difference may not impact migration from S29AL032D to S29GL032N or S29JL032J. An often employed alternate software configuration customizing method is to query the Common Flash Interface (CFI) register space to identify key flash characteristics for on-the-fly software driver customizing. The S29AL032D, S29GL032N and S29JL032J all support CFI. Refer to Table 3 for a listing of the differences between the CFI register values for these three devices.

The x8 only AL032D model 00 has CFI implemented to be compatible with older x8 only devices such as the AM29LV033C, which did not implement CFI register addressing in the same manner as the x8/x16 S29AL032D, S29GL032N, and S29JL032J devices, e.g. the specific CFI register data that would be at byte-wise x8 offset 0x68 (word-wise x16 offset 0x34) in the x8/x16 devices is at byte-wise x8 offset 0x34 on the x8-only S29AL032D model 00.

Table 3. Autoselect and CFI Related Differences (Sheet 1 of 3)

Feature	S29AL032D	S29GL032N	S29JL032J
Autoselect Device ID Code (DQ[7:0])	Model 00: A3h Model 03: F6h Model 04: F9h	Model 01,02,V1,V2: 7E/1D/00h Model 03: 7E/1A/01h Model 04: 7E/1A/00h	Model 01: 7E/0A/01h Model 02: 7E/0A/00h Model 21: 55h Model 22: 56h Model 31: 50h Model 32: 53h Model 41: 5Ch Model 42: 5Fh
Secured Silicon Sector OTP Area addressable space	256 bytes	256 bytes	256 bytes
Secured Silicon Sector OTP Area Factory Lockable	256 bytes	256 bytes	128 bytes
Secured Silicon Sector OTP Area User Lockable	256 bytes	256 bytes	128 bytes
Autoselect Secured Silicon Sector Secured Silicon Sector OTP Region - Factory Locked Code (DQ[7:0])	Model 00: 85h Model 03: 8Dh Model 04: 9Dh	Model 01,03,V1: 9Ah Model 02,04,V2: 8Ah	82h
Autoselect Secured Silicon Sector OTP Region - Default Not Factory Locked Code (DQ[7:0])	Model 00: 05h Model 03: 0Dh Model 04: 1Dh	Model 01,03,V1: 1Ah Model 02,04,V2: 0Ah	02h
CFI @ 3Eh (byte address) [@ 1Fh (byte address) for AL032D Model 00]: Typical timeout for single byte/word write	0004h	0007h	0003h
CFI @ 40h (byte address) [@ 20h (byte address) for AL032D Model 00]: Typical timeout for buffer write	0000h	0007h	0000h
CFI @ 42h (byte address) [@ 21h (byte address) for AL032D Model 00]: Typical timeout for block erase	000Ah	000Ah	0009h

Table 3. Autoselect and CFI Related Differences (Sheet 2 of 3)

Feature	S29AL032D	S29GL032N	S29JL032J
CFI @ 44h (byte address) [@ 22h (byte address) for AL032D Model 00]: Typical timeout for chip erase	0000h	0000h	000Fh
CFI @ 46h (byte address) [@ 23h (byte address) for AL032D Model 00]: Maximum timeout for single byte/word write	0005h	0003h	0004h
CFI @ 48h (byte address) [@ 24h (byte address) for AL032D Model 00]: Maximum timeout for buffer write	0000h	0005h	0000h
CFI @ 50h (byte address) [@ 28h (byte address) for AL032D Model 00]: Device Interface Description (refer to CFI publication 100)	Model 00: 0000h Model 03,04: 0002h	0002h	0002h
CFI @ 54h (byte address) [@ 2Ah (byte address) for AL032D Model 00]: Maximum bytes in buffer write	0000h	0005h	0000h
CFI @ 58h (byte address) [@ 2Ch (byte address) for AL032D Model 00]: Number of erase block regions	Model 00: 0001h Model 03,04: 0002h	Model 01,02: 0001h Model V1,V2: 0001h Model 03,04: 0002h	0002h
CFI @ 5Ah (byte address) [@ 20h (byte address) for AL032D Model 00]: Erase Block Region 1 Info	Model 00: 003Fh Model 03,04: 0007h	Model 01,02: 003Fh Model V1,V2: 003Fh Model 03,04: 0007h	0007h
CFI @ 5Eh (byte address) [@ 2Fh (byte address) for AL032D Model 00]: Erase Block Region 1 Info	Model 00: 0000h Model 03,04: 0020h	Model 01,02: 0000h Model V1,V2: 0000h Model 03,04: 0020h	0020h
CFI @ 60h (byte address) [@ 30h (byte address) for AL032D Model 00]: Erase Block Region 1 Info	Model 00: 0001h Model 03,04: 0000h	Model 01,02: 0001h Model V1,V2: 0001h Model 03,04: 0000h	0000h
CFI @ 62h (byte address) [@ 31h (byte address) for AL032D Model 00]: Erase Block Region 2 Info	Model 00: 0000h Model 03,04: 003Eh	Model 01,02: 0000h Model V1,V2: 0000h Model 03/04: 003Eh	003Eh
CFI @ 68h (byte address) [@ 34h (byte address) for AL032D Model 00]: Erase Block Region 2 Info	Model 00: 0000h Model 03,04: 0001h	Model 01,02: 0000h Model V1,V2: 0000h Model 03,04: 0001h	0001h
CFI @ 88h (byte address) [@ 44h (byte address) for AL032D Model 00]: Minor Version Number	0031h	0033h	0033h
CFI @ 8Ah (byte address) [@ 45h (byte address) for AL032D Model 00]: Process and Address Sensitive Unlock	Model 00: 0001h Model 03,04: 0000h	0010h	000Ch
CFI @ 90h (byte address) [@ 48h (byte address) for AL032D Model 00]: Temporary Sector Unprotect	0001h	0000h	0001h
CFI @ 92h (byte address) [@ 49h (byte address) for AL032D Model 00]: Sector Protection Scheme	0004h	0008h	0004h
CFI @ 94h (byte address) [@ 4Ah (byte address) for AL032D Model 00]: Number of simul-op sectors per bank	0000h	0000h	Model 01,02: 0038h Model 21,22: 0038h Model 31,32: 0030h Model 41,42: 0020h
CFI @ 98h (byte address) [@ 4Ch (byte address) for AL032D Model 00]: Read Page Mode Type	0000h	0002h	0000h
CFI @ 9Ah (byte address) [@ 4Dh (byte address) for AL032D Model 00]: ACC Voltage Minimum	00B5h	00B5h	0085h
CFI @ 9Ch (byte address) [@ 4Eh (byte address) for AL032D Model 00]: ACC Voltage Maximum	00C5h	00C5h	0095h
CFI @ 9Eh (byte address) [@ 4Fh (byte address) for AL032D Model 00]: Top or Bottom Boot Sectors	Model 00: 0000h Model 03: 0003h Model 04: 0002h	Model 01,V1: 0005h Model 02,V2: 0004h Model 03: 0003h Model 04: 0002h	Model 01,21: 0003h Model 02,22: 0002h Model 31,41: 0003h Model 32,42: 0002h

Table 3. Autoselect and CFI Related Differences (Sheet 3 of 3)

Feature	S29AL032D	S29GL032N	S29JL032J
CFI @ A0h (byte address): Program Suspend Support	n/a	0001h	0000h
CFI @ AEh (byte address): Bank Organization	n/a	n/a	Model 01,02: 0004h Model 21,22: 0002h Model 31,32: 0002h Model 41,42: 0002h
CFI @ B0h (byte address): Bank 1 Sector Qty	n/a	n/a	Model 01,02: 000Fh Model 21,22: 000Fh Model 31,32: 0017h Model 41,42: 0027h
CFI @ B2h (byte address): Bank 2 Sector Qty	n/a	n/a	Model 01,02: 0018h Model 21,22: 0038h Model 31,32: 0030h Model 41,42: 0020h
CFI @ B4h (byte address): Bank 3 Sector Qty	n/a	n/a	Model 01,02: 0018h Model 21,22: 0000h Model 31,32: 0000h Model 41,42: 0000h
CFI @ B6h (byte address): Bank 4 Sector Qty	n/a	n/a	Model 01,02: 0008h Model 21,22: 0000h Model 31,32: 0000h Model 41,42: 0000h

Note:

1. *n/a = Not Applicable.*

1.8 Operating Temperature Range

The S29AL032D is available in both the Industrial temperature range of -40 to +85°C and the Extended temperature range of -40 to +125°C. The S29GL032N and S29JL032J are only available in the Industrial temperature range of -40 to +85°C.

1.9 DC and AC Specification Differences

The S29AL032D, S29GL032N and S29JL032J have principally compatible DC and AC parameter specifications that allow migration often without change to memory controller or voltage regulation circuitry. As indicated in Table 1, the S29AL032D was available in two t_{ACC} speed grades: 70 ns and 90 ns. The S29GL032N is available in two t_{ACC} speed grades: 90 ns and 110 ns. The S29JL032J will be available in two t_{ACC} speed grades: 60 ns and 70 ns. Applications utilizing the 90 ns rated S29AL032D can readily migrate to either the 90 ns rated S29GL032N or the 70 ns rated S29JL032J.

Table 4 summarizes all difference in the DC specifications between the S29AL032D, S29GL032N and S29JL032J. The only DC parameter difference that may require hardware modification to accommodate is the lower V_{HH} (max) voltage applied to the WP#/ACC pin during accelerated programming (see Section 1.5, *Buffer Programming*). All other DC parameter differences are minor and should not prevent migration from S29AL032D to either S29GL032N or S29JL032J.

Table 4. DC Specification Differences (Sheet 1 of 2)

Parameter	Description		S29AL032D	S29GL032N	S29JL032J
I_{CC}	V_{CC} Active Initial Read Current @ 5 MHz	max	16 mA	30 mA	16 mA
I_{CC}	V_{CC} Active Intra-Page Read Current @ 33 MHz	max	n/a	20 mA (1)	n/a
I_{CC}	V_{CC} Active Program/Erase Current	max	35 mA	60 mA	30 mA
I_{CC}	V_{CC} Accelerated Program Current	max	30 mA	60 mA	n/s
I_{HH}	V_{HH} Accelerated Program Current	max	10 mA	20 mA	n/s
I_{LI}	Input Load Current All I/O But WP#/ACC	max	± 1 µA	± 1 µA	± 1 µA
I_{LI}	Input Load Current WP#/ACC	max	± 1 µA	± 2 µA	± 1 µA
V_{ID}	High Voltage Range for Autoselect		11.5 - 12.5V	11.5 - 12.5V	8.5 - 12.5V
V_{HH}	High Voltage Range for Accelerated Program		11.5 - 12.5V	11.5 - 12.5V	8.5 - 9.5V
V_{IO}	V_{IO} Supply Range		n/a	1.65 - 3.6V (2)	n/a

Table 4. DC Specification Differences (Sheet 2 of 2)

Parameter	Description		S29AL032D	S29GL032N	S29JL032J
V_{IL}	Input Logic Low @ 2 mA	max	0.8V	0.3 x V_{IO}	0.8 V
V_{IH}	Input Logic High @ -2 mA	min	0.7 x V_{CC}	0.7 x V_{IO}	0.7 x V_{CC}
V_{OL}	Output Logic Low @ 2 mA	max	0.45V	0.15 x V_{IO}	0.45V
V_{OH}	Output Logic High @ -2 mA	min	2.4	0.85 x V_{IO}	2.4

Notes:

1. *Only S29GL032N supports Page Read mode.*
2. *Only S29GL032N models V1 and V2 support $V_{IO} < V_{CC}$.*
3. *n/a = Not Applicable.*
4. *n/s = Not Specified.*

Table 5 details the difference in the AC specifications for t_{ACC} = 70 ns and 90 ns rated speed grades of the S29AL032D, S29GL032N and S29JL032J. Significant increases in programming throughput will occur when migrating from S29AL032D to S29JL032J while programming throughput will drop when migrating from the S29AL032D to S29GL032N. A substantial portion of this programming throughput decrease can be mitigated if system software is modified to support the parallel buffer programming feature of the S29GL032N. Implementing support for buffer programming of the S29GL032N is optional but likely desired.

Several timing parameter differences that may impact migration are detailed below.

Data polling on the S29GL032N and S29JL032J requires address to be set up at least 15 and 12 ns, respectively, prior to OE# assertion (t_{ASO}) and requires CE# and OE# to be negated at least 20 ns between data polling reads (t_{CEPH}, t_{OEPH}) to allow update of the embedded operation status data. The S29AL032D did not have these data polling specification requirements; however, common read operation implementations support these requirements and in most cases memory controller set up or firmware changes will not be required to accommodate these new timing requirements. System that utilize polling of the RY/BY# output instead of software data polling for embedded operation status determination will not be impacted by these new timing requirements.

The S29JL032J requires data to be set up (t_{DS}) at least 40 ns prior to data latching on write cycles as triggered by the rising edge of WE# or CE#, which ever occurs first. This is 5 ns more than the required data set up of 35 ns for the S29AL032D. Systems must be evaluated to determine if the memory controller configuration supports this longer data set up requirement. If the system can not support 40 ns data set up, then use of the faster 60 ns speed grade of S29JL032J is recommended as it support t_{DS} of 35 ns minimum.

The S29GL032N will release the data bus within 20 ns of CE# or OE# negation at the conclusion of a read cycle (t_{DF}), which is up to 4 ns slower than the S29AL032D. This generally is not an operational issue unless the data bus is shared by multiple components and the bus is actively driven by another component within this transition to High-Z period. Even if this is the case, the resulting bus contention will persist for no more than 4 ns which should not inhibit data latching on other peripherals sharing the data bus.

The S29GL032N requires OE# set up (t_{OE}) at least 35 ns prior to data being sampled during a read, which is 5 ns earlier than that required for the S29AL032D. Generally it is not an issue meeting this set up requirement set up requirement since most memory controllers assert OE# concurrent with or soon after CE# is asserted which results in significant setup margin prior to data being latched at the conclusion of a read cycle.

Additional information on AC timing definition and measurement can be obtained in the Understanding AC Characteristics Application Note.

Table 5. AC Specification Differences

Parameter	Description		S29AL032D		S29GL032N	S29JL032J
t_{RC}	Read Cycle Time	min	70 ns	90 ns	90 ns	70 ns
t_{ACC}, t_{CE}	Read Address/CE# To Output	max	70 ns	90 ns	90 ns	70 ns
t_{PACC}	Read Page Access Time	max	n/a	n/a	25 ns (1)	n/a
t_{OE}	Read OE# Setup To Data Valid	min	30 ns	35 ns	25 ns (2)	30 ns
t_{DF}	CE#/OE# to High-Z	max	16 ns	16 ns	20 ns	16 ns
t_{SRW}	Latency Between Write and Read Cycles	min	20 ns	20 ns	n/s	0 ns
t_{ASO}	Address Setup to OE# During Polling	min	n/s	n/s	15 ns	12 ns
t_{CEPH}, t_{OEPH}	CE# and OE# High While Polling	min	n/s	n/s	20 ns	20 ns
t_{AH}	Address Hold Time	min	45 ns	45 ns	45 ns	35 ns
t_{DS}	Data Setup Time	min	35 ns	45 ns	35 ns	40 ns
t_{WP}	Write Pulse Width - WP# Controlled	min	35 ns	35 ns	35 ns	30 ns
t_{WHWH1}	Single Word Program Time	typ	11 µs	11 µs	60 µs	6 µs
t_{WHWH1}	Single Word Program Time	max	360 µs	360 µs	n/s	80 µs
t_{WHWH1}	Accelerated Word Programming Time	typ	7 µs	7 µs	54 µs	4 µs
t_{WHWH1}	Accelerated Single Word Program Time	max	210 µs	210 µs	n/s	70 µs
t_{WHWH1}	Effective Per Word Write Buffer Program Time	typ	n/a	n/a	15 µs	n/a
t_{WHWH1}	Effective Per Word Accelerated Write Buffer Program Time	typ	n/a	n/a	12.5 µs	n/a
t_{WHWH2}	64 kB Sector Erase Time	typ	0.7 s	0.7 s	0.5 s	0.5 s
t_{WHWH2}	64 kB Sector Erase Time	max	10 s	10 s	3.5 s	5 s

Notes:

1. *Specified for $V_{IO} = V_{CC}$. For $V_{IO} < V_{CC}$, $t_{PACC} = 30$ ns.*
2. *Specified for $V_{IO} = V_{CC}$. For $V_{IO} < V_{CC}$, $t_{OE} = 30$ ns.*
3. *n/a = Not Applicable.*
4. *n/s = Not Specified.*

1.10 Packaging Differences

S29AL032D models 03 and 04 in the TSOP 48-pin TS048 package can migrate without to sector architecture compatible S29GL032N and S29JL032J models with no board layout or assembly changes due to the use of identical package and pin outs.

S29AL032D models 03 and 04 in the VBN048 10.0 x 6.0 mm 48-ball fine pitch BGA package can migrate to the S29GL032N or S29JL032J in the VBK048 8.15 x 6.15 mm 48-ball fine pitch BGA package without layout changes. These BGA packages share common ball and signal placement to facilitate migration with only a change in pick and place machine programming to accommodate the different package outside dimensions. Refer to Figures 1 and Figure 2 and Table 6 for a comparison of the specifications for these JEDEC standard packages.

S29AL032D model 00 in the TSOP 40-pin TS040 package cannot migrate to a S29GL032N or S29JL032J without board layout and assembly changes since neither device is available in TS040 package. Cypress recommends TS040 applications be modified to support use of the standard x8/x16 pinout TS048 package.

S29AL032D model 00 in the VBN048 10.0 x 6.0 mm 48-ball fine pitch BGA package cannot migrate to a S29GL032N or S29JL032J without board layout and assembly changes since this model has a unique pinout not supported by either the S29GL032N or S29JL032J. Cypress recommends S29AL032D model 00 applications using the VBN048 be modified to support use of the standard x8/x16 VBK048 or LAE064 BGA packages.

Figure 1. VBN048 Drawing (S29AL032D)

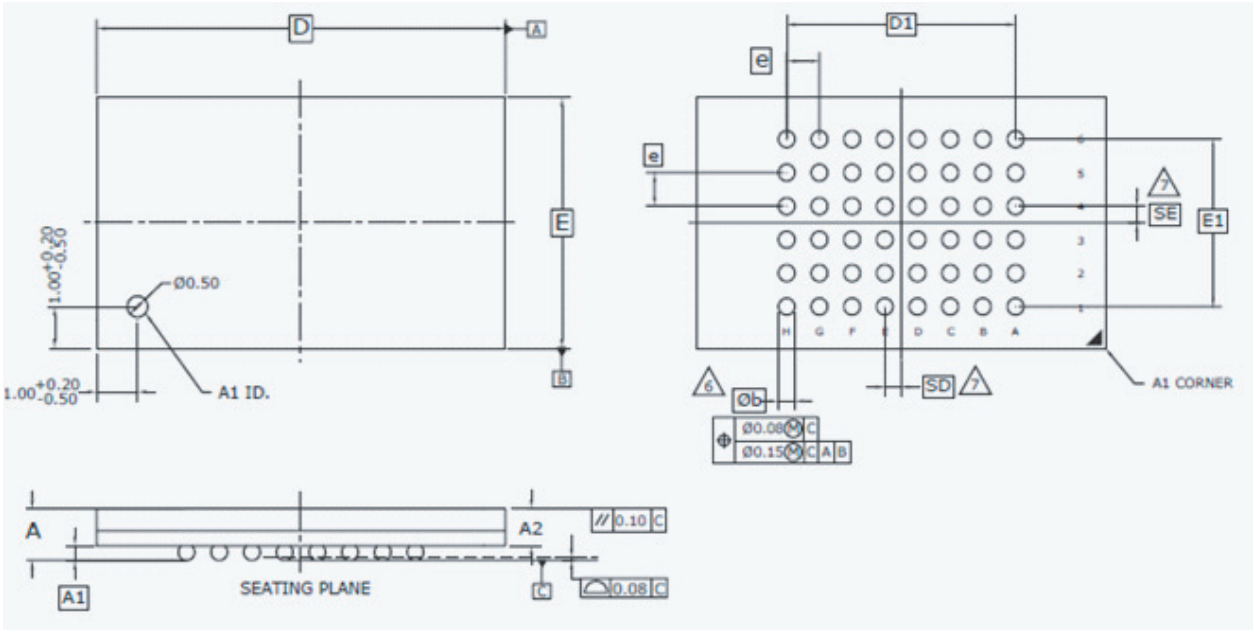

Figure 2. VBK048 Drawing (S29GL032N and S29JL032J)

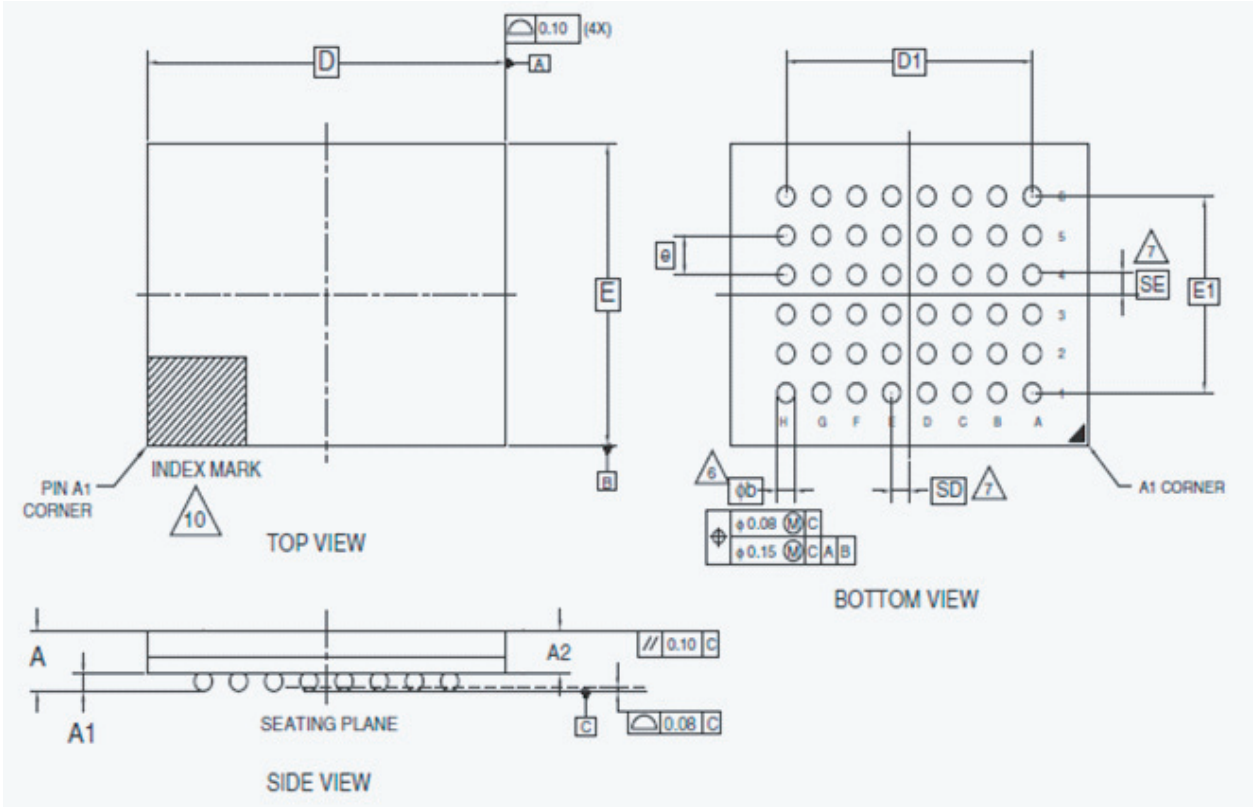

Table 6. VBN048 and VBK048 Package Dimensions

Parameter	JEDEC Symbol	VBN048 (S29AL032D)	VBK048 (S29GL032N, S29JL032J)
Overall Thickness (max)	A	1.00 mm	1.00 mm
Ball Height (min)	A1	0.17 mm	0.18 mm
Body Thickness (min)	A2	0.62 mm	0.62 mm
Body Thickness (max)	A2	0.73 mm	0.76 mm
Body Length (BCS.)	D	10.00 mm	8.15 mm
Body Width (BCS.)	E	6.00 mm	6.15 mm
Ball Footprint length (BCS.)	D1	5.60 mm	5.60 mm
Ball Footprint Width (BCS.)	E1	4.00 mm	4.00 mm
Row Matrix In D Dimension	MD	8	8
Column Matrix In E Dimension	ME	6	6
Total Ball Count	N	48	48
Ball Diameter (min)	fb	0.35 mm	0.35 mm
Ball Diameter (max)	fb	0.45 mm	0.43 mm
Ball Pitch (BCS.)	e	0.80 mm	0.80 mm
Solder Ball Placement (BCS.)	SD / SE	0.40 mm	0.40 mm
Depopulated Solder Balls		none	none

2 Conclusion

S29AL032D boot sector models can be replaced with architecturally compatible S29GL032N or S29JL032J in most applications with minimal software modifications. S29AL032D uniform sector model 00 cannot be readily migrated to either S29GL032N or S29JL032J due to pinout differences. It is important that careful examination of the impact of all feature implementation and DC and AC specification differences be reviewed for each application when selecting an appropriate device for migration. Table 7 provides a recommended migration path summary from S29AL032D models to specific S29GL032N and S29JL032J models based on application requirements. Table 8 provides recommended S29GL032N and S29JL032J ordering part numbers for specific S29AL032D ordering part numbers.

Table 7. Recommended Migration Device Models

S29AL032D Model	Boot Sector Orientation	Sector Architecture (SA0 to SAmax)	Application Requires T_{ACC} < 90 ns	Target S29GL032N Model	Target S29JL032J Model	Migration Comment
00	Uniform	64-64 kB	yes	-	31 or 32	Different sector architecture; Incompatible pin out
00	Uniform	64-64 kB	no	01 or 02	-	SW changes required; Incompatible pin out
03	Top	63-64 kB, 8-8 kB	yes	-	31	Identical sector architecture; Compatible pin out
03	Top	63-64 kB, 8-8 kB	no	03	31	Identical sector architecture; Compatible pin out
04	Bottom	8-8 kB, 63-64 kB	yes	-	32	Identical sector architecture; Compatible pin out
04	Bottom	8-8 kB, 63-64 kB	no	04	32	Identical sector architecture; Compatible pin out

Table 8. Recommended Migration Ordering Part Numbers (Sheet 1 of 2)

S29AL032D Ordering Part Number	Recommended Migration Order Part Number	Comments
S29AL032D70TAI00	S29JL032J70TFI31 S29JL032J70TFI32	Requires HW, SW and solder changes
S29AL032D70TFI00	S29JL032J70TFI31 S29JL032J70TFI32	Requires HW and SW changes
S29AL032D90TAI00	S29GL032N90TFI01 S29GL032N90TFI02	Requires HW, SW and solder changes
S29AL032D90TFI00	S29GL032N90TFI01 S29GL032N90TFI02	Requires HW and SW changes
S29AL032D70BAI00	S29JL032J70BHI31 S29JL032J70BHI32	Requires HW, SW and solder changes
S29AL032D70BFI00	S29JL032J70BHI31 S29JL032J70BHI32	Requires HW and SW changes
S29AL032D90BAI00	S29GL032N90DFI01 S29GL032N90DFI02	Requires HW, SW and solder changes
S29AL032D90BFI00	S29GL032N90DFI01 S29GL032N90DFI02	Requires HW and SW changes
S29AL032D70TAI03	S29GL032N90TFI03 S29JL032J70TFI31	Requires solder change, May require SW changes
S29AL032D70TFI03	S29GL032N90TFI03 S29JL032J70TFI31	May require SW changes
S29AL032D90TAI03	S29GL032N90TFI03 S29JL032J70TFI31	Requires solder change, May require SW changes
S29AL032D90TFI03	S29GL032N90TFI03 S29JL032J70TFI31	May require SW changes
S29AL032D70TAI04	S29GL032N90TFI04 S29JL032J70TFI32	Requires solder change, May require SW changes
S29AL032D70TFI04	S29GL032N90TFI04 S29JL032J70TFI32	May require SW changes
S29AL032D90TAI04	S29GL032N90TFI04 S29JL032J70TFI32	Requires solder change, May require SW changes
S29AL032D90TFI04	S29GL032N90TFI04 S29JL032J70TFI32	May require SW changes
S29AL032D70BAI03	S29JL032J70BHI31	Requires solder change, May require SW changes
S29AL032D70BFI03	S29JL032J70BHI31	May require SW changes
S29AL032D90BAI03	S29GL032N90BFI03 S29JL032J70BHI31	Requires solder change, May require SW changes
S29AL032D90BFI03	S29GL032N90BFI03 S29JL032J70BHI31	May require SW changes
S29AL032D70BAI04	S29JL032J70BHI32	Requires solder change, May require SW changes
S29AL032D70BFI04	S29JL032J70BHI32	May require SW changes
S29AL032D90BAI04	S29GL032N90BFI04 S29JL032J70BHI32	Requires solder change, May require SW changes
S29AL032D90BFI04	S29GL032N90BFI04 S29JL032J70BHI32	May require SW changes
S29AL032D90TAN00	No Recommendation	
S29AL032D90TFN00	No Recommendation	
S29AL032D90BAN00	No Recommendation	
S29AL032D90BFN00	No Recommendation	
S29AL032D90TAN03	No Recommendation	
S29AL032D90TFN03	No Recommendation	
S29AL032D90BAN03	No Recommendation	

Table 8. Recommended Migration Ordering Part Numbers (Sheet 2 of 2)

S29AL032D Ordering Part Number	Recommended Migration Order Part Number	Comments
S29AL032D90BFN03	No Recommendation	
S29AL032D90TAN04	No Recommendation	
S29AL032D90TFN04	No Recommendation	
S29AL032D90BAN04	No Recommendation	
S29AL032D90BFN04	No Recommendation	

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/07/2010	Initial version
*A	–	–	09/15/2010	DC Specification Differences table: updated rows V_{IH} and V_{OL}
*B	–	–	01/06/2012	Updated text Autoselect and CFI Related Differences table: Corrected CFI offsets for S29AL032D Model 00
*C	–	–	08/08/2012	In the Conclusion section, recommended Migration Ordering Part Numbers table: corrected JL032J BGA material set OPN character from F to H
*D	4981204	MSWI	10/22/2015	Updated in Cypress template
*E	5797473	AESATMP8	07/06/2017	Updated logo and Copyright.

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