AN98500

S29GL-S Page Read Mode - Reducing System Startup Time

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Associated Part Family: S29GL-S

AN98500 highlights the S29GL-S Flash Read Page Mode architecture, operation, and an example Page Read Mode performance.

1 Introduction

Today's high speed embedded systems are enabling higher performance and a richer user experience; these new system designs are seeing dramatic increases in system architecture complexity along with higher memory densities to support today's OS, Application, and digital data contents. Designers are using innovation to address competing system requirements to provide highest performance capabilities without impacting other systems constraints like cost or reliability.

The typical high performance embedded system uses code shadowing memory architecture. The system initial start-up time is significantly defined by the shadowing and initialization times where the shadowing time is characterized by the System On Chip (SOC) / flash access bandwidths and data densities being transferred from flash to DRAM. In general, new systems designs need to improve or at least maintain system start-up time without impacting costs. Slow system start-ups are not a desirable feature and not acceptable in many applications.

The Cypress portfolio provides several classes of flash-memory devices that offer multiple read access modes. The Cypress S29GL-S MirrorBit® Eclipse™ Family offers both Asynchronous and Page Read Mode access capabilities. The Page Read Mode architecture significantly improves read bandwidth (BW) performance compared to standard asynchronous accesses. Today there are a number of processors that have control logic integrated to seamlessly support the flash read page mode capabilities. This application note highlights the S29GL-S Flash Read Page Mode architecture, operation, and an example Page Read Mode performance.

2 Read Page Mode Operation and System Start-Up Time

The Read Page Mode provides a means to improve flash read bandwidth (BW), which can reduce system start-up time and improve overall system performance. There are chipset and flash memory suppliers who provide a range of devices that support both asynchronous and page read modes. Freescale's MPC, iMX, TI's OMAP™, and others have integrated control logic that enables seamless interface of the external buses to Cypress's flash, like the S29GL-S MirrorBit Eclipse family, and achieve read page mode capabilities. The S29GL-S offers high performance and cost effective support for both asynchronous and page read mode options. The following sections provide a high level overview of the page read mode operation along with comparisons of asynchronous and page mode read performance capabilities.

The Read Page Mode flash architecture enables significant Read BW improvements compared to asynchronous accesses performance. Asynchronous Read mode is the most basic read access and its read performance is derived from the flash devices initial read access time t_{ACC}. The initial access time defines the time for the flash to complete the process steps of address decoding along with converting and transferring the NVM data to the flash output buffer. Note a simple asynchronous device only processes a single word for each flash access. The Read Page Mode Architecture is more complex than simple Asynchronous flash. The Page Mode architecture transfers a group of words within a defined Page boundary from the flash array to a flash Buffer in parallel. A Page is a defined address boundary typically consisting of 4, 8, 16 or more words. The time to read a complete Page is defined by the initial access time t_{ACC} and sum of the subsequent reads within the Page Boundary defined by t_{PACC}. The information below highlights the flash Asynchronous initial access time and Page Read Accesses times:

Flash Asynchronous initial access time = t_{ACC}

Page Read Time = t_{ACC}, + Kx(t_{PACC})

Where:

- K is the total number of subsequent reads in the Page Boundary

- $t_{ACC} > t_{PACC}$

Note: Subsequent intra-Page reads (t_{PACC}) are from the flash's internal buffer, which does not require all the process steps associated with an initial asynchronous access (t_{ACC}).

The S29GL-S flash supports the Page mode access features; during an initial read from a new page boundary the S29GL-S stores a group of 16 adjacent words, referred to as the "Page." Subsequent data reads within this same Page address boundary are read from the internal flash buffers (t_{PACC}) per word. The S29GL-S lower address lines A[3:0] provide access to the intra-page addresses for the 16 individual words within a page. The upper address lines (A [MAX: 4]) select a new page address boundary. A new page is selected every time the page boundary address (A [MAX: 4]) changes or CE# toggles HIGH then LOW.

In summary, read page mode offers higher read BW performance than simple asynchronous read capability. The timing of an asynchronous Read BW is substantially defined by the flash t_{ACC}, and read page mode read BW is derived from the combination of the t_{ACC} and t_{PACC} where $t_{PACC} < t_{ACC}$.

3 Read Access Times: Asynchronous Read verses Page Read Mode

The previous section highlights that Page Read access mode offers improved read BW performance compared to asynchronous read accesses.

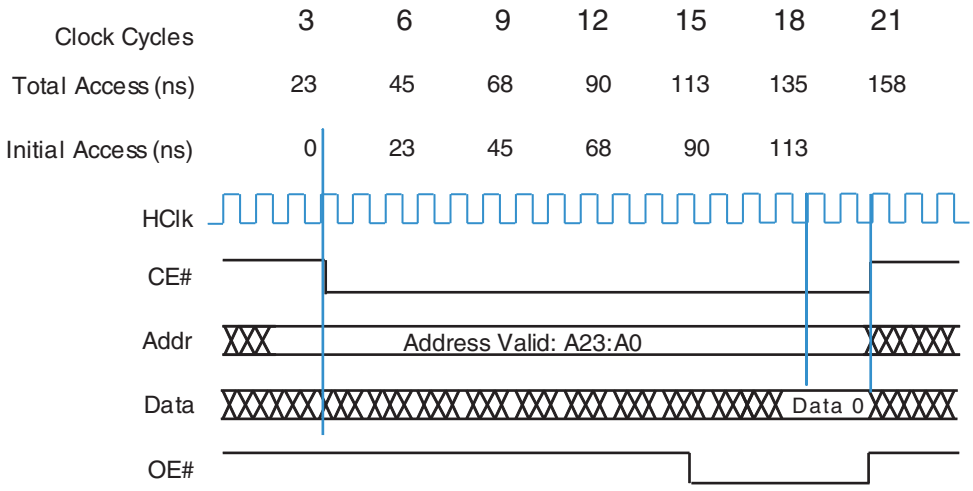
The S29GL-S data sheet specification shows this flash supports the following read access options:

- Initial Read Access: t_{ACC} options from 90 ns to 120 ns
  Ideal Asynchronous Read BW could reach ~22 MB/s, excluding processor setup and hold times.
- Page Read Access: t_{PACC} options from 15 ns to 30 ns
  Ideal Page Read BW could reach ~98.5 MB/s, excluding processor setup and hold times.

The following provides example Asynchronous and Page read performance data for a system configuration interfacing a Freescale iMX5x to a Cypress S29GL-S flash. Both the iMX5x and S29GL-S support Asynchronous and Page Read access modes. The read access shown in Figure 1 and Figure 2 below assumes the iMX5x BCLK is operating at 133 MHz using the shown setup and hold times.

Figure 1 highlights the overall read access cycle time to complete a single word Asynchronous access.

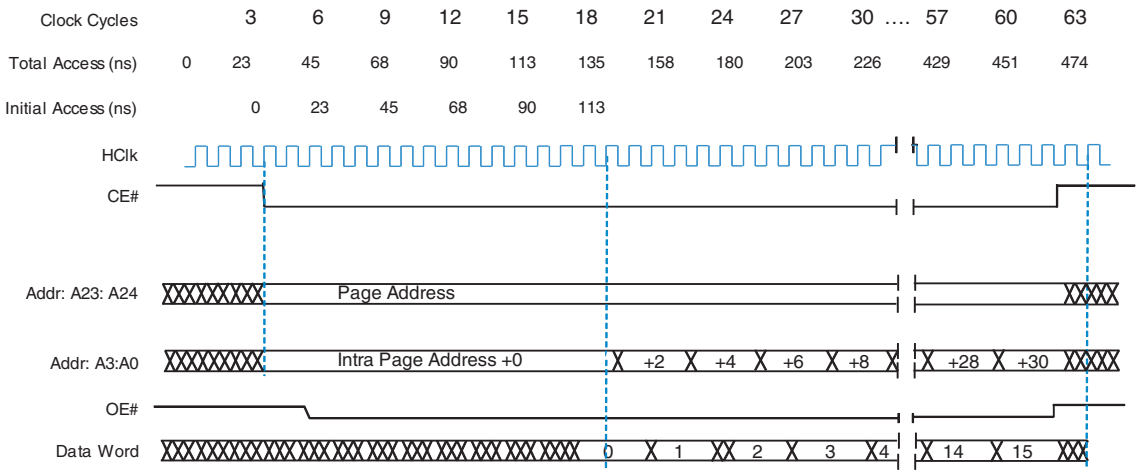
Figure 1. iMX5x / S29GL256S Asynchronous Read Timing (1 Word)



The setup conditions used to complete a single asynchronous word read requires 158 ns, which is approximately 13 MB/s.

Figure 2 shows the cycle time to complete a 16-word Page access.

Figure 2. iMX5x / S29GL256S Page Read Timing (16 Words / 32 Bytes)



The setup conditions used to complete this 16 word Page read requires 474 ns, which is approximately 68 MB/s.

The above Page Read configuration setup realizes a 68 MB/s read BW which is >5x greater than the Asynchronous Read BW of 13 MB/s.

4 Application Considerations

Every processor has its unique set of operating features and constraints, which may enable or not enable the realization of a given read BW. A given processor may multiplex or share pin functions between interfaces such as DDR and Local Bus, which may result in time multiplexing of the buses to transfer data from flash to DDR. In such cases, the overall sustained read bandwidth may be reduced from what is observed during a single word or Page access.

5 Conclusion

Many high-speed embedded systems, like automotive in-dash applications and consumer devices, continue to increase in complexity and code densities. Typically, these systems employ code shadowing architectures and require fast system start-up times. The previous section highlights that systems controllers, like the Freescale™ iMX5XC, can obtain improved read BW accessing Cypress flash devices like S29GL-S by using the Read Page mode feature. The exact read BW improvement depends on the processor design, configuration, and setup. Read Page Mode provides a straight forward, cost effective solution to significantly improve read BWs compared to standard asynchronous read accesses. The improved read page mode read BWs provide a simple and effective solution to provide faster system start-up times and improved performance.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/03/2011	Initial version.
*A	4959025	MSWI	10/12/2015	Updated to Cypress template.
*B	5843040	AESATMP8	08/03/2017	Updated logo and Copyright.
*C	6161525	PRIT	04/30/2018	Updated to new template. Completing Sunset Review.

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