

S29GL-S Page Read Mode - Reducing System Startup Time

Author: Ken Perdue

Associated Part Family: S29GL-S

AN98500 highlights the S29GL-S Flash Read Page Mode architecture, operation, and an example Page Read Mode performance.

1 Introduction

Today's high speed embedded systems are enabling higher performance and a richer user experience; these new system designs are seeing dramatic increases in system architecture complexity along with higher memory densities to support today's OS, Application, and digital data contents. Designers are using innovation to address competing system requirements to provide highest performance capabilities without impacting other systems constraints like cost or reliability.

The typical high performance embedded system uses code shadowing memory architecture. The system initial start-up time is significantly defined by the shadowing and initialization times where the shadowing time is characterized by the System On Chip (SOC) / flash access bandwidths and data densities being transferred from flash to DRAM. In general, new systems designs need to improve or at least maintain system start-up time without impacting costs. Slow system start-ups are not a desirable feature and not acceptable in many applications.

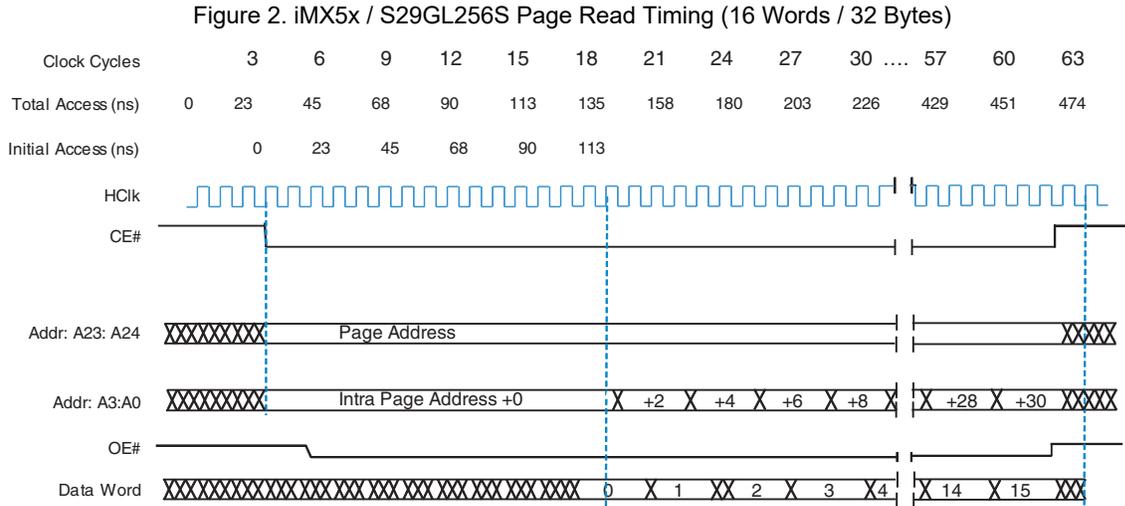
The Cypress portfolio provides several classes of flash-memory devices that offer multiple read access modes. The Cypress S29GL-S MirrorBit® Eclipse™ Family offers both Asynchronous and Page Read Mode access capabilities. The Page Read Mode architecture significantly improves read bandwidth (BW) performance compared to standard asynchronous accesses. Today there are a number of processors that have control logic integrated to seamlessly support the flash read page mode capabilities. This application note highlights the S29GL-S Flash Read Page Mode architecture, operation, and an example Page Read Mode performance.

2 Read Page Mode Operation and System Start-Up Time

The Read Page Mode provides a means to improve flash read bandwidth (BW), which can reduce system start-up time and improve overall system performance. There are chipset and flash memory suppliers who provide a range of devices that support both asynchronous and page read modes. Freescale's MPC, iMX, TI's OMAP™, and others have integrated control logic that enables seamless interface of the external buses to Cypress's flash, like the S29GL-S MirrorBit Eclipse family, and achieve read page mode capabilities. The S29GL-S offers high performance and cost effective support for both asynchronous and page read mode options. The following sections provide a high level overview of the page read mode operation along with comparisons of asynchronous and page mode read performance capabilities.

The Read Page Mode flash architecture enables significant Read BW improvements compared to asynchronous accesses performance. Asynchronous Read mode is the most basic read access and its read performance is derived from the flash devices initial read access time t_{ACC} . The initial access time defines the time for the flash to complete the process steps of address decoding along with converting and transferring the NVM data to the flash output buffer. Note a simple asynchronous device only processes a single word for each flash access. The Read Page Mode Architecture is more complex than simple Asynchronous flash. The Page Mode architecture transfers a group of words within a defined Page boundary from the flash array to a flash Buffer in parallel. A Page is a defined address boundary typically consisting of 4, 8, 16 or more words. The time to read a complete Page is defined by the initial access time t_{ACC} and sum of the subsequent reads within the Page Boundary defined by t_{PACC} . The information below highlights the flash Asynchronous initial access time and Page Read Accesses times:

Figure 2 shows the cycle time to complete a 16-word Page access.



The setup conditions used to complete this 16 word Page read requires 474 ns, which is approximately 68 MB/s.

The above Page Read configuration setup realizes a 68 MB/s read BW which is >5x greater than the Asynchronous Read BW of 13 MB/s.

4 Application Considerations

Every processor has its unique set of operating features and constraints, which may enable or not enable the realization of a given read BW. A given processor may multiplex or share pin functions between interfaces such as DDR and Local Bus, which may result in time multiplexing of the buses to transfer data from flash to DDR. In such cases, the overall sustained read bandwidth may be reduced from what is observed during a single word or Page access.

5 Conclusion

Many high-speed embedded systems, like automotive in-dash applications and consumer devices, continue to increase in complexity and code densities. Typically, these systems employ code shadowing architectures and require fast system start-up times. The previous section highlights that systems controllers, like the Freescale™ iMX5XC, can obtain improved read BW accessing Cypress flash devices like S29GL-S by using the Read Page mode feature. The exact read BW improvement depends on the processor design, configuration, and setup. Read Page Mode provides a straight forward, cost effective solution to significantly improve read BWs compared to standard asynchronous read accesses. The improved read page mode read BWs provide a simple and effective solution to provide faster system start-up times and improved performance.

Document History Page

Document Title: AN98500 - S29GL-S Page Read Mode - Reducing System Startup Time				
Document Number: 001-98500				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	–	–	06/03/2011	Initial version.
*A	4959025	MSWI	10/12/2015	Updated to Cypress template.
*B	5843040	AESATMP8	08/03/2017	Updated logo and Copyright.
*C	6161525	PRIT	04/30/2018	Updated to new template. Completing Sunset Review.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2011-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSOC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.