AN98559

Integrating 3-V Flash in 5-V Systems

AN98559 addresses two areas that are critical to enable the integration of 3.3-V flash into a system using a System Controller with 5-V I/O: the I/O signal requirements and the flash VCC power regulation requirements.

1 Abstract

Today there are a number of legacy 5-V designs in production; the number of options to directly support the 5-V controllers with native 5-V flash has substantially diminished in recent years. This application note will highlight design changes in a 5-V embedded system that enables the integration of 3.3-V flash devices. This application note will address two areas that are critical to enable the integration of 3.3-V flash into a system using a System Controller with 5-V I/O: the I/O signal requirements and the flash V_{CC} power regulation requirements.

2 3.3-V Flash Support in 5-V Legacy Designs

Flash Technology is being designed and manufactured on 65-nm, 45-nm, and even 32-nm lithography nodes; these flash devices predominately operate at Core voltages of 3.3-V or lower and support similar level I/O voltages. There are a number of legacy designs utilizing 5-V microcontrollers, but the number of options to directly support the 5-V controllers using native 5-V flash has substantially diminished. Today's lower voltage flash devices can be incorporated into a 5-V design. The following section will address both the I/O signal requirements and power regulation to allow integration of the 3.3-V flash into a 5-V based system.

2.1 Signal Translation

A 5-V System Controller's signals used to access the flash device include data, address, and control signals. These signals must meet the input requirements for a lower voltage flash device without impacting the system functionality. For example, a Cypress S29GL256P flash utilizes a native 3.3-V V_{CC} and its input signals are not 5-V tolerant. The flash device requires an interface to translate incoming control, data, and address signals from 5-V levels down to acceptable 3.3-V levels. Standard voltage translators can be employed to address this issue. Buffer Drivers and Bus Transceivers can be used to translate the incoming control, data, and address signals between the 5-V I/O and 3.3-V I/O levels. The SN74LVCH16244A and SN74LVCH16245A are low cost Buffer Drivers and Bus Transceivers ideal for this purpose. The SN74LVCH16244A device is a unidirectional buffer/line driver with 5-V tolerant I/O pins, suitable for address and control signal translation. The SN74LVCH16245A is a bi-directional bus transceiver used for input/output data signals. Integrating these ICs enables the voltage translations of all control signals, address, and data lines.

The next step is to determine the total number of unidirectional and bidirectional signals used by the System Controller to access a S29GL256P flash.

2.1.1 Unidirectional Signals: Address and Control Lines

The S29GL256P unidirectional signals consists of the address lines and six signal control pins (WE#, OE#, CE#, WP#, RY/BY#, and RESET#). The number of address lines will vary depending on the flash density.

This 256 Mbit flash requires 24 address lines. Figure 1 illustrates the connection of the first 16 address lines from the 5-V address bus to the 3-V flash address pins. Figure 2 outlines the connections for eight additional address lines and the six required control signals. Since the flash address and control pins are input only the Output Enable lines of the buffer can be tied to ground to simplify the control circuitry. The total address and control signal system requires 30 translation lines for this case.

Figure 1. Address Bus Interface

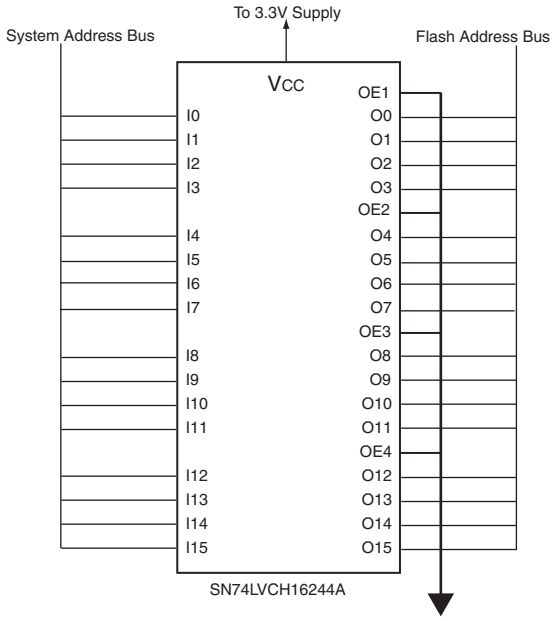
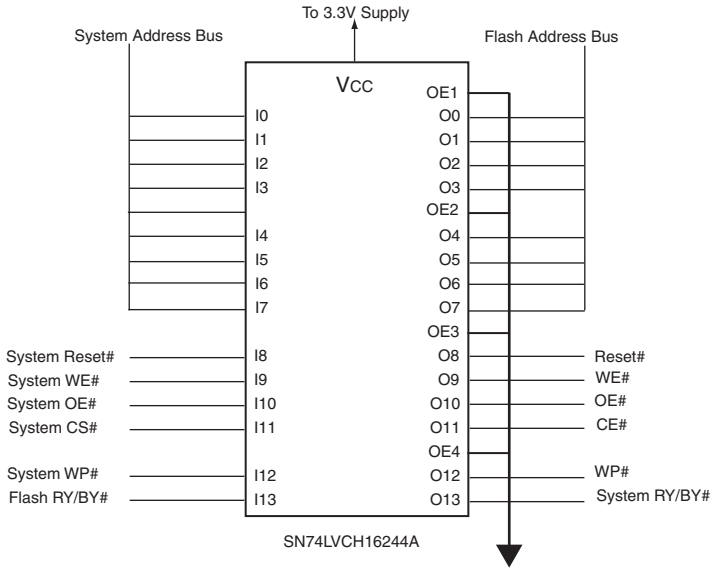


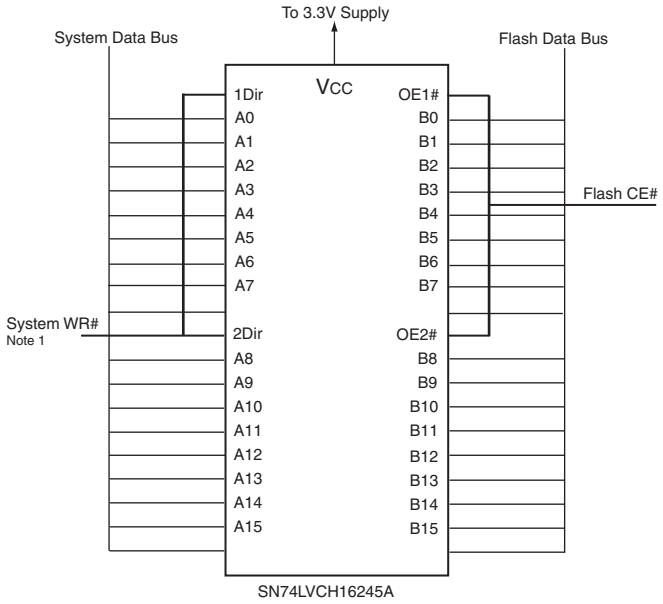
Figure 2. Address and Control Signals



2.1.2 Bi-Directional Signal: Data Bus

The S29GL256P 16-bit data bus requires a low voltage transceiver/buffer, to allow for bidirectional data transactions. The SN74LVCH16245A a 5-V tolerant transceiver/buffer can be used for this purpose. This device is similar to the previously used address buffers, but the 245 device contains additional logic input to differentiate between reads and writes. Figure 3 shows the 16 data bus connections.

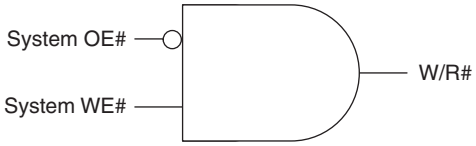
Figure 3. Data Bus Interface



Note:

1. *Some Controllers do not support the W/R# signal; this signal distinguishes between a bus read and a bus write cycle and can be synthesized from the System OE# and System WE# signals outlined in* Figure 4*. Note this circuit implementation assumes System OE# and System WR# are active low.*

Figure 4. Synthesize W/R#



2.2 Flash V_{CC} Power Regulation

The final point to address is the V_{CC} requirement for the S29GL256P device. To supply the correct operating voltage to this flash device, the 5-V supply must be regulated to 3.3-V to meet the flash V_{CC} range. The voltage regulation can be realized by way of a low cost LDO fixed linear regulator. Fixed linear regulators are readily available on the market from many companies such as Linear Technologies and other manufacturers. Reference the Linear Technology web site (http://www.linear.com) for data sheet and application notes for regulators such as LT1117, LT1121, or other 3.3-V regulars.

2.3 Summary

The proceeding information highlights a means to enable the use of 3.3-V flash in a 5-V systems design. This information addresses two critical systems-level areas: the I/O signal requirements and the flash V_{CC} power regulation requirements. There were detailed examples of interface and V_{CC} regulation devices to facilitate the use of 3-V Flash in a 5-V system design.

Please consult your device data sheet to ensure your flash software will adhere to the specified requirements. If you have further questions about using Cypress flash devices, contact Cypress support.

Document History Page

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**	–	–	10/13/2010	Initial version
*A	4958961	MSWI	10/12/2015	Updated in Cypress template
*B	5870037	AESATMP8	09/01/2017	Updated logo and Copyright.

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