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AN202751

Surface Mount Assembly Recommendations for Cypress FBGA Packages

AN202751 provides guidelines on surface mount assembly for Cypress's Fine Pitch Ball Grid Array (FBGA) packages, printed circuit board (PCB) design, surface mount process flow, and final joint inspection methods.

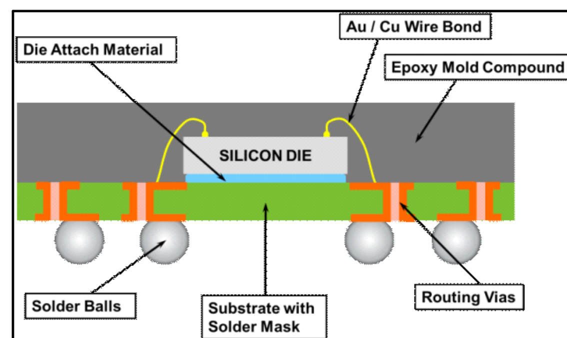
1 Abstract

This application note serves as a general guideline on surface mount assembly for Cypress's Fine Pitch Ball Grid Array (FBGA) packages. This application note includes printed circuit board (PCB) design considerations, surface mount process flow and final joint inspection methods. The recommendations have been included to reflect current industry practices and standards. Due to several components being assembled on the same board, process optimization and adjustment may also be required. Customers should also follow the recommendations of the PCB manufacturer and solder paste supplier. Please contact our sales representatives for further questions regarding surface mount assembly for Cypress products.

2 Cypress FBGA Packages

For every generation of technology, electronic systems shrink and the demand increases for smaller footprint packages with higher functional densities. FBGA packages, as shown in Figure 1, offer a better solution compared to traditional packages for such demands. FBGA offers a higher ratio of Input/Output (I/O) count to package size.

Figure 1. Schematic of Single Chip FBGA Construction



BGA packages offer additional advantages over traditional lead frame packages as described below.

- Robust mechanical structure: BGA solder balls are less susceptible to damage leading to failure compared to leads used in traditional packages
- Higher I/O density: As mentioned earlier, BGA packages allow to pack more I/Os in given area in a grid array increasing the I/O density of the package.
- Better electrical performance: BGA packages can be designed for superior electrical performance at higher frequencies by adding ground planes, power and ground rings to the package.
- Low cost assembly: Solder ball connections are more forgiving to placement tolerance due to its native property to self-align. This allows for lower cost assembly equipment and higher throughput.
- Better thermal management: These packages offer better thermal management by use of heat dissipating thermal vias and solder balls.

Cypress offers devices in a wide range of FBGA packages with ball pitch ranging from 0.50 mm up to 1.00 mm. The package design and attribute data for all these packages are detailed in Chapter 1 of the packaging handbook: Chapter 1 Package Design.

When an FBGA package is mounted on a PCB, most of the solder joints at the inside rows are hidden between the package body and the board, which makes it difficult to employ visual inspection to guarantee the quality of the surface mount process. Process control, material quality, and package/PCB design are the key areas that contribute to higher assembly yields.

3 PCB Design Consideration

3.1 PCB Land Pad Size

Cypress offers solder mask defined (SMD) pad on the package side, where the solder mask overlaps the pad surface. The size of the solder mask opening defines the solder wetted area. However, the solder ball land pads on the PCB can be either solder mask defined (SMD) or non-solder mask defined (NSMD), as shown in Figure 2. With SMD configuration, the solder mask covers the outer edge of the solder land pad. This configuration promotes a controlled collapse of the ball profile. The overlap of the solder mask onto the copper also increases the copper pad adhesion to the PCB laminate surface, which could be an important consideration when the assembled board is under extreme drop or bending, or when the resin system, which has low adhesion, is used. If SMD configuration on PCB is utilized, it is recommended to design the land pad size and solder mask opening to be the same size as the FBGA pad to provide a balanced stress on solder joints.

In the non solder mask defined (NSMD) configuration, the solder mask opening is larger than the solder land pad. Therefore, the entire top and side land pad surfaces are exposed for FBGA solder ball to adhere, providing a stronger joint. In this case, the solder joint has fewer stress points. The PCB pad diameter for solder ball attachment is recommended to be 80% - 100% of the package pad opening diameter.

Cypress recommends NSMD configuration for PCB land pad design for most applications. Table 1 provides the example of the optimum PCB land pad size and solder mask opening size for Cypress FBGA packages.

Figure 2. Solder Mask Defined and Non-Solder Mask Defined Configuration

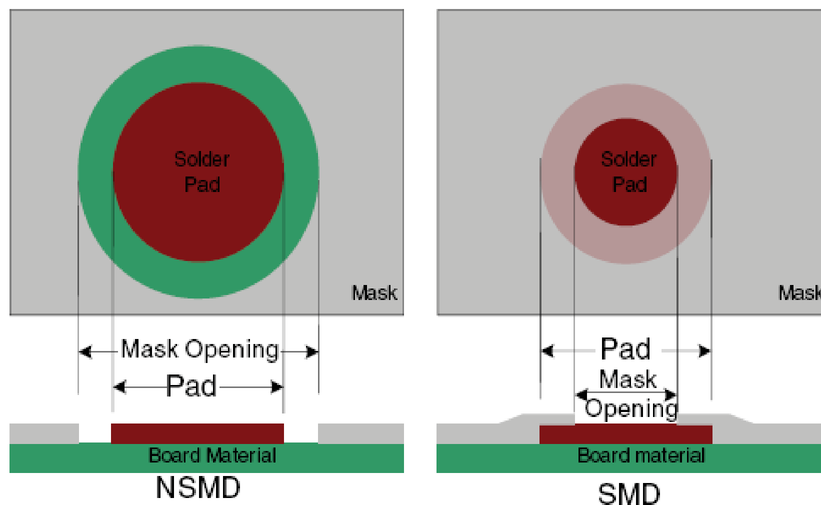


Table 1. Recommended PCB Pad Diameter for FBGA

		Recommended for SMD		Recommended for NSMD	
BGA Pad Pitch (mm) e	Ball Diameter (mm) ϕb	Pad Size (mm)	Mask Opening (mm)	Pad Size (mm)	Mask Opening (mm)
1.00	0.50-0.70	0.60	0.50	0.45	0.60
1.00	0.35-0.50	0.45	0.35	0.35	0.50
0.80	0.30-0.50	0.50	0.40	0.35	0.50
0.65	0.25-0.53	0.40	0.30	0.27	0.37
0.50	0.25-0.35	0.35	0.25	0.25	0.35

3.2 PCB Trace Width and Space

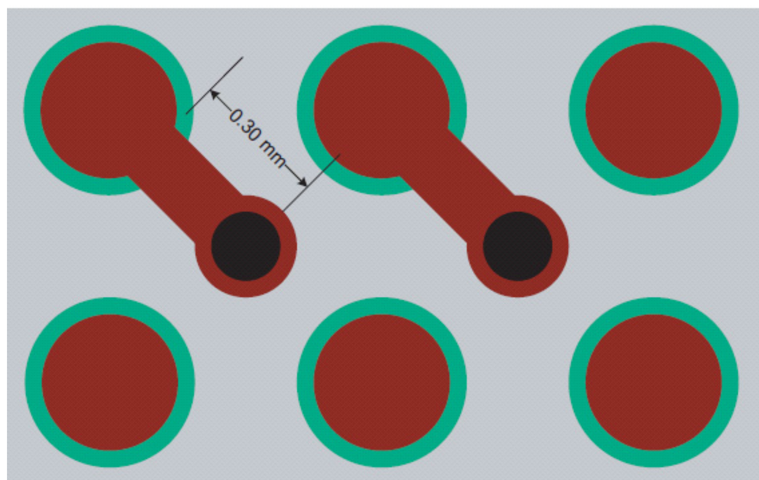
PCB trace width and space design depends on the pitch of the FBGA, the conventional PCB technology, and the routing scheme on the PCB. For conventional PCB technology, the trace width and space can be allowed to be as small as 4 mil (0.102 mm) or 5 mil (0.127 mm). The minimum trace width and space, if needed, is 3 mil (0.076 mm). Please keep in mind that PCB cost increases when the tighter design is required.

3.3 Via and Via Capture Pad

With small pitch FBGA, it is difficult to design escape routing for inside rows with only one signal trace between solder balls. With multi-layer PCB, utilizing one or more via, as shown in Figure 3, to drop the signal to another layer of the PCB can solve this problem. Via capture pads are usually placed diagonally with the surface land pads. Various drill sizes can be used depending on the solder ball pitch. Typical via mechanical drill diameter is 10mil (0.254 mm) with 20 mil (0.508 mm) diameter via capture pad. For 0.5 mm pitch FBGA, micro-via or High Density Interconnect (HDI) can be used. Typical micro-via diameter is 5 mil (0.127 mm) on a 10 mil (0.254 mm) or smaller diameter pad. Micro-via technologies was developed utilizing laser drilling, photo-defining, and plasma etching.

Vias are not recommended to be placed under the solder lands due to the risk of solder wicking inside the via during reflow. This could cause electrical open or potential reliability risk. Cypress recommends placing via at a minimum distance of 0.3mm from the solder land pad as shown in Figure 3.

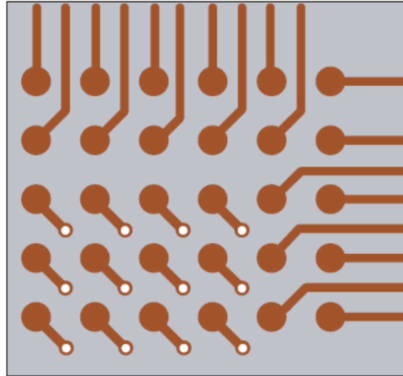
Figure 3. Recommended Placement of Via



3.4 Escape Routing

Escape routes should be designed while maintaining good signal integrity. It is recommended to limit one signal trace between two solder lands as shown in Figure 4.

Figure 4. Example of Escape Routing



Also abrupt changes in trace width at escape points should be avoided (see Figure 5) to reduce noise due to reflections. It is recommended to change the trace width gradually as shown in Figure 6.

Figure 5. Incorrect Trace Width Adjustment at Escape Point

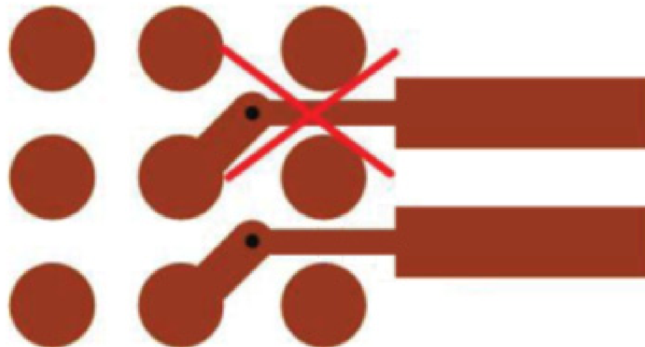
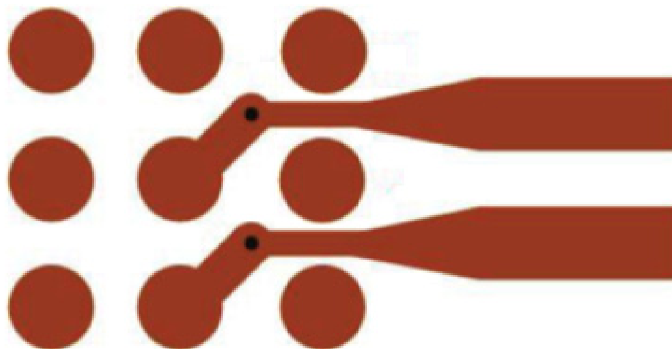


Figure 6. Correct Trace Width Adjustment at Escape Point



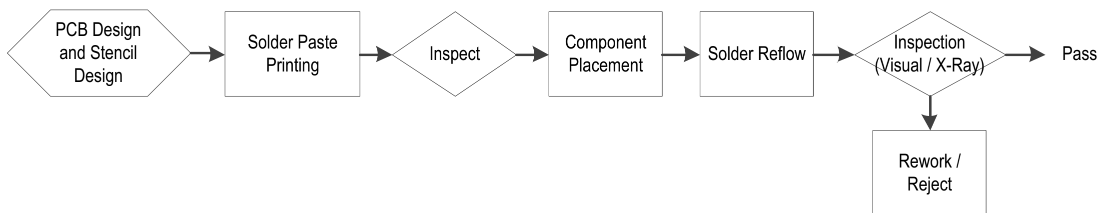
4 PCB Surface Finish

Another design consideration is the selection of the surface finish for the board. While hot air solder leveled (HASL) boards have been successfully used for FBGA; however, the uneven surface of the pad makes it more difficult to achieve consistent assembly yields. On the other hand, excellent yields have been achieved with both Ni/Au plated pads and also with bare copper pads coated with organic solderability preservatives (OSP). In the case of Ni/Au plated pads, it is important to control the plating quality to prevent embrittlement of the solder joint. This can occur if the gold is too thick; gold thickness of 5 mils maximum is recommended. There has been some concern in the industry that certain kinds of nickel plating can cause embrittlement. Your PCB supplier should be able to give advice on this subject.

5 Surface Mount Process

A general process flow for assembly of SMT products is shown in Figure 7. It is recommended to use a similar process flow for Cypress products including post-reflow inspection. This section will describe guidelines for high yield assembly process including stencil design, solder reflow optimization and final inspection techniques.

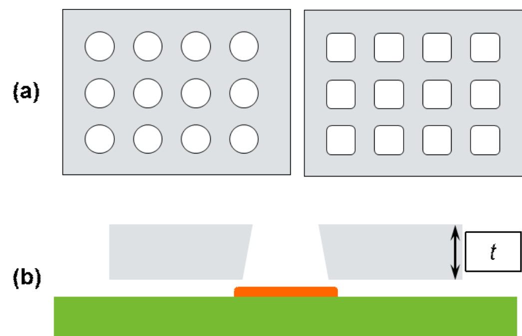
Figure 7. Typical Process Flow for SMT Assembly of Cypress FBGA Products



5.1 Solder Stencil Design Guidelines

Stencil should be made of stainless steel for durability and processed by electroform or laser cut with electro-polished walls for uniform paste release. The aperture should have circular shape or square shape with rounded corners as illustrated in Figure 8a. For circular shape aperture, the diameter of the aperture should be equal to the diameter of the land pad. For square shape aperture, the width of the square should be equal to the diameter of the land pad.

Figure 8. Top View of a Solder Paste Stencil with Circular and Square Openings



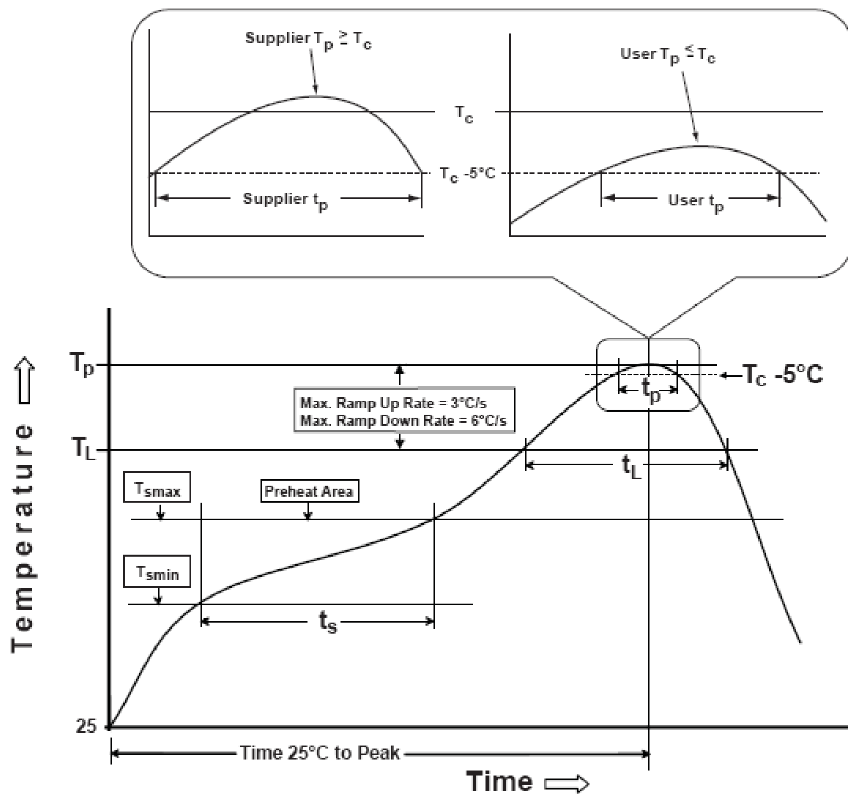
The square aperture with rounded corners should be kept within the confines of the solder mask. The stencil thickness (t), shown in Figure 8b for FBGA is generally in the 4 mils to 6 mils range. For acceptable paste release, the area ratio should be kept at more than 0.66. The area ratio is defined as the ratio of the area of aperture to the area of the aperture walls. More detail of the stencil design guidelines can be found in the IPC-7525A. An inspection of the PCB board after paste printing is recommended before picking and placing parts.

5.2 Solder Paste and Reflow Profile

A no-clean, type-3 solder paste is recommended for assembly. The advantage of using a low residue, no-clean solder paste is that additional processes of PCB cleaning and drying after reflow are not required. Sn63/Pb37 (63%Sn, 37%Pb) alloy is recommended for standard eutectic solder paste and SnAgCu alloy is recommended for lead-free application.

The actual reflow profile depends on the thermal mass of the entire populated board and the solder pasted used. Most paste manufacturers provide a suggested thermal profile for their products. Also, the assembly house should optimize the board mounting reflow profiles according to the board design and components on the board. Figure 9 shows the reflow profile according to J-STD-020E. This is not a recommendation for a reflow profile, but rather demonstrates the reflow profile to which surface mount devices have been qualified.

Figure 9. Qualification Reflow Profile per J-STD-020

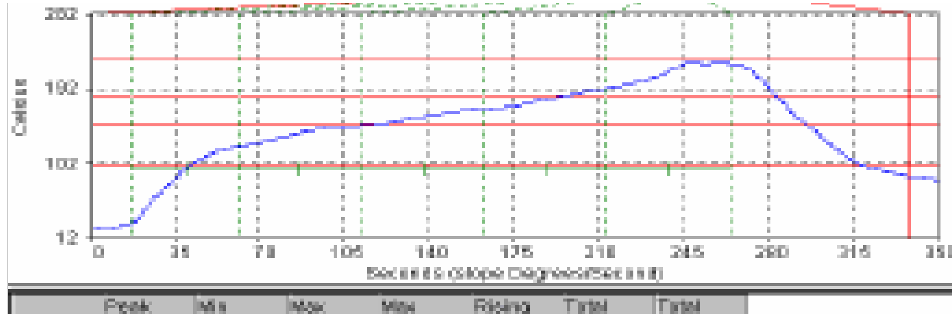


Parameter	Conditions
Preheat Temperature Range and Time	150°C 200°C for 60-120s
Ramp-up rate (T_L to T_P)	3 °C/s max.
Liquidus temperature and time	217°C for 60-150 seconds
Peak package temperature (T_P)	260 °C (Unless otherwise specified)
Time (T_P)* within 5 °C of Peak	30* seconds
Ramp-down rate (T_P to T_L)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.
** Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.*	

Some general guidelines for reflow soldering are mentioned below, although each board mounting situation is unique and should be tailored accordingly.

- SnPb Paste: The reflow peak temperature should be kept in the 220-230°C range, with total time above 183°C for 30-60 seconds, and ramp down rate at -5°C/second maximum. An actual reflow profile used to produce good board level reliability result is shown in Figure 10.
- SnAgCu Paste: the reflow peak temperature should be kept in the 235-245°C range, with total time above 217°C for 30-60 seconds, and ramp down rate at -5°C/second maximum. An actual reflow profile used to produce good board level reliability result is shown in Figure 11.

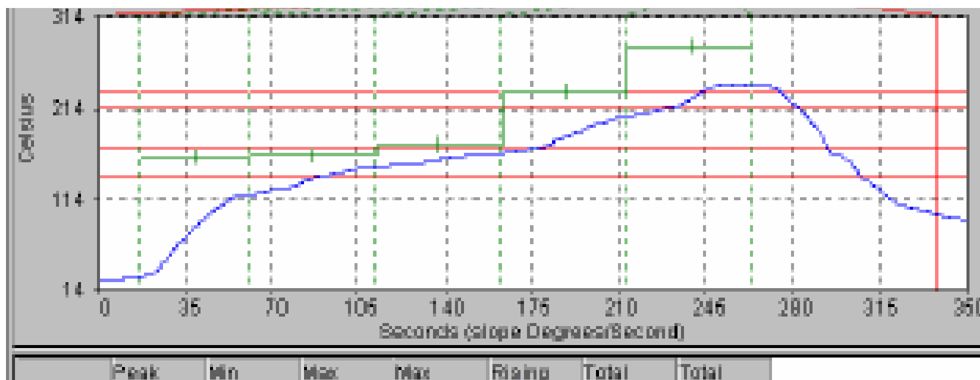
Figure 10. Generic SnPb Reflow Profile



Note:

1. *Time above 183°C: 50sec / Peak temperature: 222°C*

Figure 11. Generic SnAgCu (Pb-free) Reflow Profile



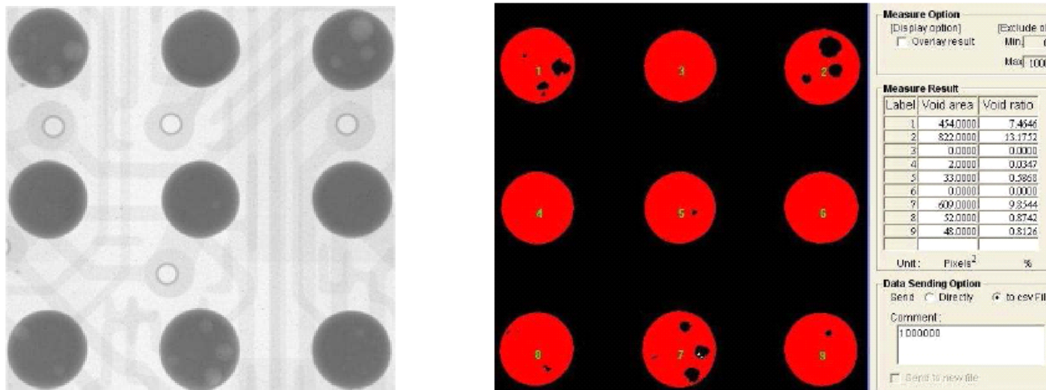
Note:

1. *Time above 217°C: 50 sec / Peak temperature: 240°C*

5.3 Solder Joint Inspection

Non-destructive inspection of FBGA on a PCB is typically done using transmission type X-ray equipment. X-ray can detect bridging, shorts, opens, and solder voids. With the help of imaging software, the % of void area can be determined, as shown in Figure 12.

Figure 12. Imagine Software to Calculate % Void Area



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- IPC - Association Connecting Electronic Industries, IPC-7095, Design and Assembly Process Implementation for BGA's, October 2004.
- IPC - Association Connecting Electronic Industries, IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard, February 2005.
- IPC - Association Connecting Electronic Industries, IPC-7525A, Stencil Design Guidelines, February 2007.
- IPC/JEDEC, J-STD-020E, Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices, December 2014.

Document History Page

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