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AN99121

NOR FLASH: A PRACTICAL GUIDE TO ENDURANCE AND DATA RETENTION

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AN99121 provides examples of endurance and data retention parameters and highlights the capabilities of Cypress MirrorBit and Floating gate flash.

1 Endurance

Endurance is the parameter that specifies the cumulative program/erase cycling capability of any individual sector within a device. Each sector-erase operation has the capability of introducing defects into the memory cell structure that may accumulate over time. At some point, these defects may prevent a cell from programming, erasing or reading. When such a failure occurs in a cell that contains critical data, the loss of data may cause system failure. The sector in which the failure occurs is effectively end-of-life.

All erase operations are physically performed at the sector level. A chip-erase is an internally managed sequence of sector erases. Thus, endurance is a sector-level specification. Any failure within a sector does not affect the health of any other sector in the array. The cumulative impact of repeated erasures must be assessed on a sector-by-sector basis.

Cypress's single-bit-per-cell floating-gate flash devices are designed to withstand 1,000,000 erase and reprogram cycles under typical conditions. These devices are the most robust non-volatile devices available in terms of endurance.

Cypress's two-bit-per-cell MirrorBit flash devices are designed to withstand 100,000 erase and reprogram cycles under typical conditions. These devices are the most cost effective non-volatile NOR devices available and provide more than adequate endurance for the vast majority of applications.

The endurance specification of a flash device should be evaluated in terms of the projected in-system rate of erasure for any given sector. In general, sectors that contain operational code may be updated a few times during manufacture, then infrequently once placed in the field. They accumulate very little wear associated with cumulative erase cycling.

On the other end of the use spectrum, sectors used for data logging may rapidly accumulate erase cycles depending on the frequency and size of the data being captured. Such use may ultimately lead to those sectors failing.

Table 1 attempts to put erase cycling quantities into the context of in-system usage. Average erasure frequency is tabulated for various cumulative erase cycles quantities for several typical product life spans.

Table 1. Endurance Erasure Rates per Sector

Erase Cycles per Sector	Product Life	Average Erasure Frequency	Approximate Number of Erasures
1,000	10 years	One every 3.7 days	2 times per week
1,000	5 years	One every 1.8 days	4 times per week
1,000	1 year	One every 8.8 hours	3 times per day
10,000	10 years	One every 8.8 hours	3 times per day
10,000	5 years	One every 4.4 hours	5 times per day
10,000	1 year	One every 53 minutes	27 times per day
100,000	10 years	One every 53 minutes	27 times per day
100,000	5 years	One every 26 minutes	55 times per day
100,000	1 year	One every 5 minutes	274 times per day

For those applications that require high data renewal rates such as periodic parameter capture or data logging, the designer needs to accurately assess the data capture requirements of the system and map them to the capabilities of target flash devices. It is recommended to employ software methods to minimize, distribute, or otherwise equalize sector erase cycling to meet system end-of-life requirements. This is sometimes referred to as wear leveling.

1.1 Example 1: Basic System Erase Cycling Assessment

A radar system has to capture 105 KB of parameter data whenever auto calibration is performed. When the system is operational, auto calibration is performed once per hour. The system will be operated twelve hours per day, every day, for ten years, at up to 85°C. The system has a 28 MB flash requirement for application code and the target flash device is the 32 MB S29GL256S. Can this device support the number of erase cycles required to support the stated system data logging requirements?

First, it is useful to estimate how the data is to be captured in the target flash device. The S29GL256S has 128 KB sectors. As such, the 105 KB of parameter data is to be mapped into one sector.

Next, the rate of sector erasure should be determined. Data must be captured 12 times per day for 10 years. That amounts to ~43,800 sector erase and program cycles over the life of the system if calibration is repeatedly logged in the same sector.

The S29GL256S provides typical 100,000 erase cycle endurance per sector, so it is able to meet the auto calibration data capture requirements of this system using one sector for data parameter storage.

This assumes that the old calibration data is overwritten with new data (with an intervening erase). In this case, the old calibration data would not be saved in the event of a power or system malfunction during the auto-calibration action. It would be wise to set aside two sectors for data capture and alternate the capture of auto-calibration parameter data between sectors. This ensures that the old data is available to the system if the new data is corrupted for any reason during the auto-calibration process. In this example, the flash device has adequate array space open to support two sectors for data logging. This method provides a 2X increase in endurance margin since the individual sector cumulative erase cycling is ~21,900 cycles over the 10 year system lifetime. Thus, using more sectors gives an increase in endurance margin.

1.2 Example 2: Data Capture Rate Determination

An industrial controller board will be used in multiple systems. It has a requirement to capture up to 7.5 KB of peripheral status data periodically. The frequency of status data capture will vary based on end system usage. The system has a 10-year operation requirement. The designer is targeting the 64 MB S29GL512S to support code and data storage, and has several sectors available for status data storage. The designer would like to assess the capability of the S29GL512S for this application and determine what status data capture frequencies can be supported using up to three sectors for data capture.

The S29GL512S has 128 KB sectors. As many as 16 data logging events of 7.5 KB can be captured in any one sector before the sector is full and requires erasure, assuming the data is logged at 8-KB boundaries for convenience.

The S29GL512S supports typical 100,000 erase cycles per sector. At 16 status data capture event per sector erase cycle, the S29GL512S can support 1,600,000 status capture events per sector over the life of the part.

For a system life of 10 years, 100,000 erase cycles equates to one erasure every 53 minutes. (Refer to Table 1) At 16 status data captures per sector erasure, that equates to the S29GL512S supporting a system status data capture frequency of once every ~3.3 minutes.

If two sectors are allocated for system status data, and status data capture is alternately stored in the two sectors, the S29GL512S supports a system status data capture frequency of once every ~1.7 minutes.

If three sectors are allocated for system status data, and status data capture is alternately stored in the three sectors, the S29GL512S supports a system status data capture frequency of once every ~1.1 minutes.

Based on this information, the designer can determine how many sectors should be set aside to support various system status data capture frequencies when using the S29GL512S.

2 Data Retention

A critical end-of-life parameter is the ability of a non-volatile device to properly maintain and provide on demand the programmed state of any data bit in the array for a minimum period of time. Data retention is the parameter that specifies the maximum period of time, after programming, that data can be expected to be retrieved from the array. The ability of the contents of any particular cell in an array to return correct data over a period time is affected by numerous issues, including temperature and voltage, electrostatic environment, exposure to radiation, cumulative erase cycles, etc.

Typical data retention is specified with no erase cycles on the data sheet. See Table 2 for typical data retention as related to erase cycles.

Both Cypress MirrorBit and floating-gate flash devices are designed to provide 20 years of data retention after initial programming when exposed to a 55°C environment.

There is a measurable relationship between data retention and endurance (erase cycling), in all non-volatile flash devices. Damage accumulation resulting from repeated erasures impacts the ability of the programmed contents of a cell to be properly discerned by a read operation after a period of storage.

Cypress MirrorBit flash is designed to retain data after a minimum of 10,000 cycles. Cypress floating gate is designed to retain data after a minimum of 100,000 cycles.

The interaction between data retention and endurance specifications in Cypress flash should be understood by a designer when selecting flash and allocating flash resources to code and data to ensure that system level data integrity requirements are met. The inter-relationship between data retention and endurance including other factors to determine data retention are illustrated in Table 2 for Cypress MirrorBit flash and in Table 3 for Cypress Floating gate flash. Specifically, it shows the expected data retention within a sector, after exposure to specific numbers of erase cycles and an average of temperatures. These post-cycling data retention periods are compliant with the JEDEC specification (JESD47G, JESD22-A117B).

Table 2. Cypress MirrorBit Data Retention and Endurance Relationship

Cumulative Erase Cycles per Sector	Average Temperature	Typical Data Retention Time Post-Cycling
1 program	55°C	20 years
1,000 cycles	55°C	10 years
10,000 cycles	55°C	1 year

Table 3. Cypress floating gate Retention and Endurance Relationship

Cumulative Erase Cycles per Sector	Average Temperature	Typical Data Retention Time Post-Cycling
1 program	55°C	20 years
1,000 cycles	55°C	10 years
10,000 cycles	55°C	1 year

Notes:

1. *The relationship between cumulative erase cycles and data retention assumes a uniform rate of cycling over the life of the device. More rapid cycling reduces the time interval between erase cycles which can lead to reduced data retention time.*
2. *An average temperature is used because systems generally do not continually operate at a single temperature nor at the extremes of the operating temperature range for long periods. The system designer needs to estimate the periods of time spent at each temperature in the operating range to determine the overall average temperature the device is exposed to over the life of the product.*

As illustrated in Table 2 and Table 3, data retention in Cypress flash is influenced by the number of erase cycles, temperature, and the interval time between cycles. System designers must ensure that the data retention capabilities of the flash meet the system requirements, based on data usage and operating environment. Of particular importance when evaluating device data retention specifications is the actual system requirement for data retention. In usage conditions, two examples of non-recommendation are introduced as follows.

An example is that a system is designed to do cycling at just a few sectors without using other remaining available sectors. It produces shorter interval between cycles in a same sector and cumulates a larger cycling number per sector, and ultimately it reduces the margin of data retention.

Another example is a manufacturing line or qualification test that rapidly applies erase cycles to flash sectors. Rapid erase cycling and a regular combination of lower temperature cycling and higher temperature storage are different situations from actual system use assumed in the JEDEC standard, and it reduces the margin of data retention at high temperature storage.

Executable code must necessarily have high data retention since the code must be correct for proper system operation. Since code is changed very infrequently, the sectors containing this code are not exposed to many erase cycles over the system life and the data within those sectors have the longest retention. Cypress MirrorBit flash is capable of providing 20 years of data retention under typical operating conditions for code, which normally is cycled very few times over the life of the product.

Data that is captured periodically, such as calibration parameter data or event log data, is subject to frequent replacement. Since flash array storage capabilities are limited, frequent replacement equates to frequent sector erasures. For this reason, it is important to assess the impact of sector erase cycling on the data retention capability of the flash device and the data retention requirements of the system. In most applications, data that is replaced frequently has a corresponding short system data retention requirement. Cypress MirrorBit flash provides data retention for typical 10 years post 1k cycles and typical 1 year post 10k cycles, which is more than adequate data retention for most data logging activities. That is roughly 10 yr/1 kcyc = 3.7 days and 10 yr/10 kcyc = 8.8 hours as shown in Table 1.

For those applications that may require longer term data retention following exposure to high quantities of erase cycles (close to 10,000 erase cycles), system software should be provisioned to periodically refresh the data log sector contents by erasing and reprogramming at least once a year. This maintenance activity provides indefinite cumulative data retention. Alternatively, system software can be used to spread erase cycles across multiple sectors through wear leveling. This is generally done by Flash File System (FFS) software.

2.1 Example 3: Assessment of Data Retention Limitation in Data Logging Applications

The designer of the system in Example 1 wants to determine if the S29GL512S provides adequate data retention for both code storage and auto calibration parameter data storage.

It is estimated that the portions of flash used for code storage may be updated up to 3 times during production line and then no more than once annually while in the field. While calibration parameter data will be captured 12 times per day for 10 years and stored in 10 sectors. The system must be capable of performing cycles in any temperature within the specified data sheet range for the full 10 years.

To assess the data retention for the executable code storage, it is necessary to calculate the life time quantity of erase cycles of the sectors used for code storage. This equates to a total of 10 erase cycles: 3 during production line and 7 during field usage for 10 years. Cypress MirrorBit flash sectors exposed 3 erase cycles in room temperature and 7 erase cycles in field support 10 years of data retention at an average temperature of 55°C. The S29GL512S therefore has no issues meeting the 10 year code-storage retention requirements of the system.

To assess the data retention for the calibration parameter data storage, it is necessary to determine the system calibration parameter retention requirement and the expected data retention of the sectors used for data logging based on usage.

The system requires that the calibration data be retained until the next auto calibration operation is complete. Based on a 12-hour-per-day operational duty cycle, calibration must be retained for no more than 13 hours. That is the system's data retention requirement for calibration parameter storage until the product reaches end of life after 10 years.

Each of the sectors used for data storage accumulates ~4,380 erase cycles per sector in the 10-year system life. Since these sectors are exposed to over 1,000 and less than 10,000 erase cycles, they provide over one year of data retention at an average 55°C temperature and with roughly equal cycle interval time. (Refer to Table 2.) Therefore the S29GL512S provides significant data retention margin for calibration parameter storage of the 12 hour system level requirement.

3 Summary

Endurance and data retention specifications are to be used as guidelines for designers to assess the ability of specific flash devices to meet end-of-life system requirements. Endurance and data retention are inter-dependent parameters.

Endurance, or the cumulative erase cycling capability, is a sector-level specification and as should be assessed based on the partitioned usage of the memory array. Cypress floating gate flash can typically withstand up to 1,000,000 erase cycles per sector. Cypress MirrorBit flash can typically withstand up to 100,000 erase cycles per sector. The impact of erase cycling on endurance can be mitigated by manipulation of how repetitively captured data is physically stored in the memory array.

Data retention is a cell-level specification that indicates how long data can be expected to be reliably retrieved following programming under specific conditions. Data retention in Cypress MirrorBit flash or other non-volatile flash devices is generally influenced by erase cycles, average temperature, and interval time between cycles.

The impact of high quantities of erase cycles on data retention in Cypress MirrorBit flash is insignificant in most applications, since the high frequency of data capture and replacement equates to a real system-level data-retention requirement that is orders of magnitude less than what MirrorBit can provide at end-of-life conditions.

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