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AN98649

How to Design a Power Management System with S6BP401A

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Associated Part Family: S6BP401A

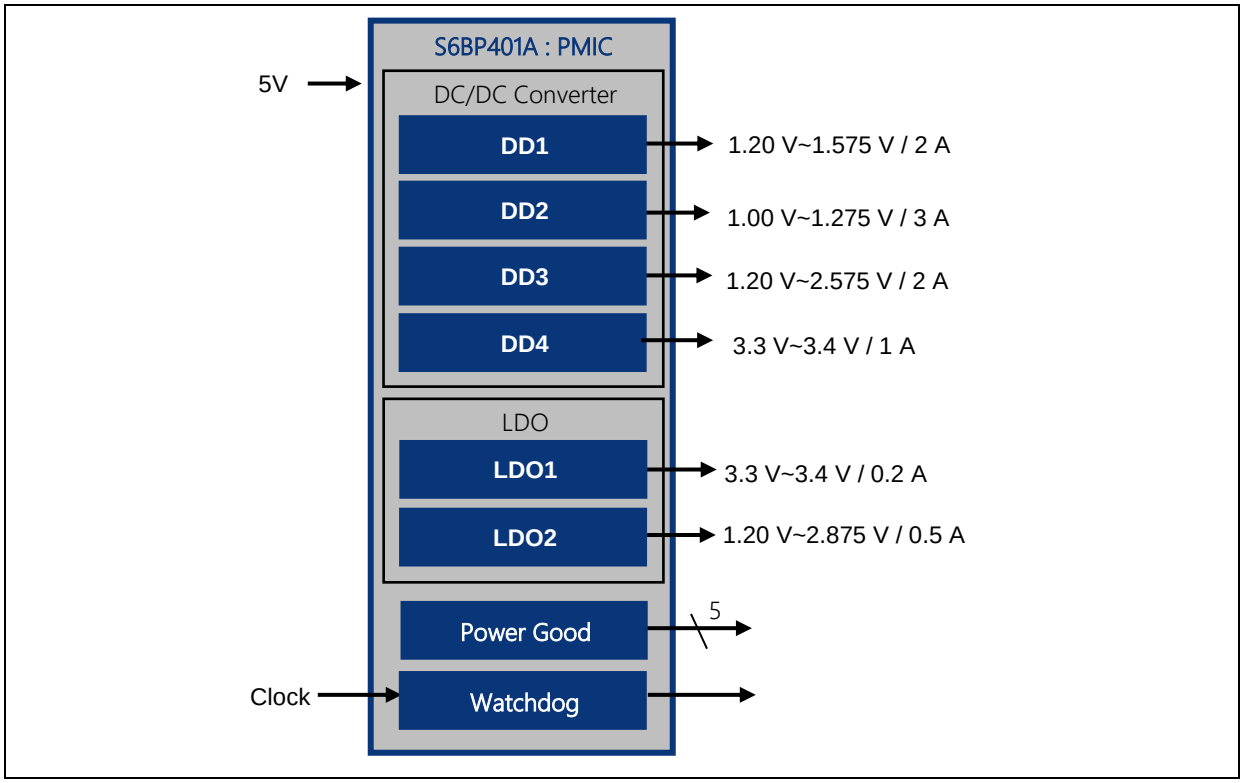
Related Documents: S6BP401A Datasheet

AN98649 explains how to select components and PCB layout guidelines for a power management system with S6BP401A, Cypress' 6-channel power management IC (PMIC).

1 Introduction

Cypress' S6BP401A is a PMIC for automotive advanced driver assistance systems (ADAS). It includes a 4-channel, step-down, 2.1-MHz DC/DC converter (DD1, DD2, DD3, and DD4), a 2-channel low-drop regulator (LDO; LDO1 and LDO2), and a watchdog timer as shown in Figure 1. S6BP401A enables you to design an ADAS system with minimal number of parts. The supply voltages of the power system that uses S6BP401A are high-precision, and S6BP401A has a power-good function and a watchdog timer function. Therefore, S6BP401A, which is compliant with AEC-Q100, provides a high-reliability power system in automotive systems.

Figure 1. Block Diagram of the Power Management System

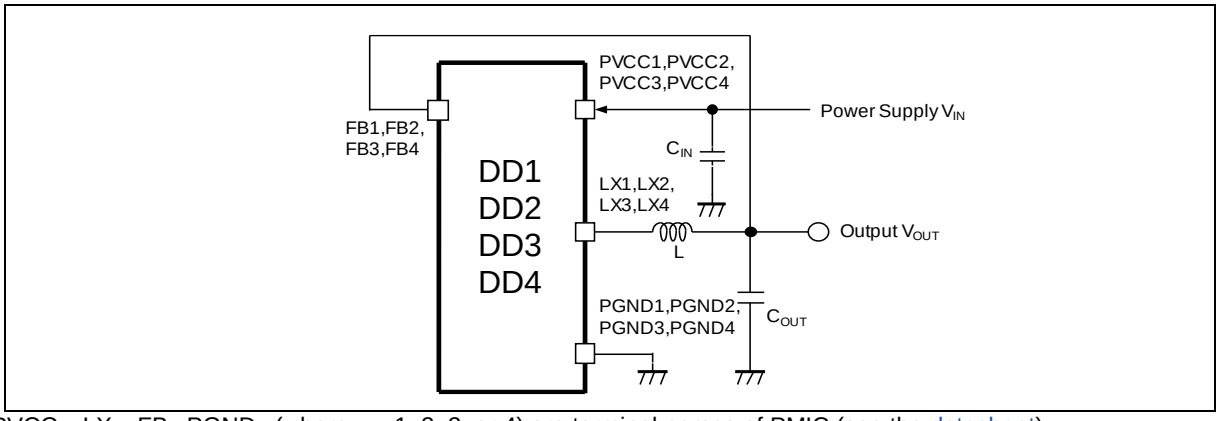


2 Components Selection

2.1 DC/DC Converter (DD1, DD2, DD3, and DD4) Parts Selection

DDx (where x=1, 2, 3, or 4) is a channel of DC/DC converter of PMIC. Select all components shown in Figure 2, which shows the DC/DC Converter section of an example circuit that uses S6BP401A.

Figure 2. Connection of the DC/DC Converter



PVCCx, LXx, FBx PGNDx (where x = 1, 2, 3, or 4) are terminal names of PMIC (see the datasheet).

2.1.1 Inductor (L)

Generally, the inductance of the coil is selected along with the value of the E6 series. Normally, you do not need to design an inductor for a power management system based on the S6BP401A device because it is designed to operate efficiently with a 1.5-µH external inductor. At the same time, you should calculate the maximum current value to confirm whether the electric current that flows to the inductor is within the rated parameters for the inductor by using Equation 1.

Equation 1

$$IL_{MAX} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}, \Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}}$$

Where:

IL_{MAX}: Rated current of inductor (A)

I_{OUT_MAX}: Maximum load current (A)

ΔI_L: Ripple current peak-to-peak value of inductor (A)

L: Inductance of inductor (H)

V_{IN}: Power supply voltage (V)

V_{OUT}: Output setting voltage (V)

f_{OSC}: Switching frequency (Hz)

2.1.2 Input Capacitor (C_{IN})

A ceramic capacitor that has a low equivalent series resistance (ESR), typically less than 10 mΩ, and excellent frequency characteristics (the capacitance is not reduced up to the switching frequency), should be used. Generally, the capacitance is selected along with the value of the E6 series. The recommended value is 10 µF. Ensure that $V_{CIN} > V_{IN}$, where V_{CIN} is the rated voltage of input capacitor (V) and V_{IN} is the power supply voltage (V).

2.1.3 Output Capacitor (COUT)

A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. Table 1 lists the recommended capacitance values for each DC/DC converter channel of the device:

Table 1. Output Capacitance List

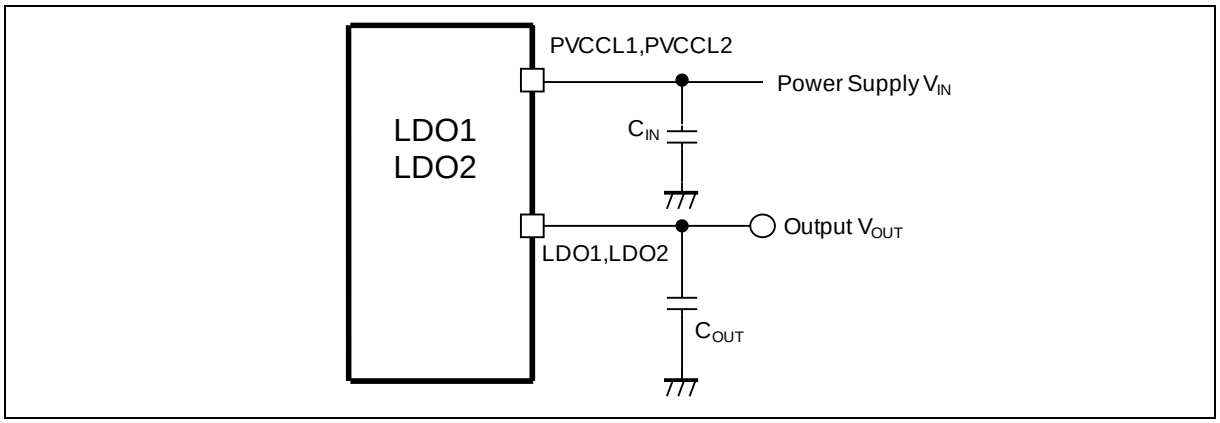
DD1	DD2	DD3	DD4
22 µF (2 nos.)	22 µF (3 nos.)	22 µF (2 nos.)	22 µF (2 nos.)

When you consider a ceramic capacitor, you should take into account the reduction of capacitance due to DC bias characteristics of the capacitor itself. Generally, a large-size capacitor has a stable DC bias characteristic. Ensure that $V_{COUT} > V_{OUT}$, where V_{COUT} is the rated voltage of output capacitor (V); V_{OUT} is the output setting voltage (V).

2.2 LDO (LDO1 and LDO2) Parts Selection

LDO1 and LDO2 are channels of the LDO of the PMIC. Figure 3 shows the LDO section of an example circuit that uses the S6BP401A power management solution. You have to select each component in this figure.

Figure 3. Connection of the LDO



PVCCLx, LDOx (where x = 1 or 2) is terminal name of PMIC (see the datasheet).

2.2.1 Input Capacitor (C_{IN}), Output Capacitor (C_{OUT})

A ceramic capacitor that has low ESR and excellent frequency characteristics should be used. Table 2 lists the recommended capacitance values.

Table 2. Output Capacitance List

	LDO1	LDO2
Input capacitor	1 µF	1 µF
Output capacitor	1 µF	10 µF

Calculate the necessary rated voltage of the capacitor by the following formula.

$$V_{CIN} > V_{IN} , V_{COUT} > V_{OUT}$$

Where:

V_{CIN}: Rated voltage of input capacitor (V)

V_{IN}: Power supply voltage (V)

V_{COUT}: Rated voltage of output capacitor (V)

V_{OUT}: Output setting voltage (V)

2.3 Common Parts Selection

2.3.1 VCC and VREG Bypass Capacitor

VCC and VREG that is terminal of PMIC (see the datasheet) need a bypass capacitor. A ceramic capacitor that has a low ESR and excellent frequency characteristics should be used. The recommended value for these capacitors is 1 µF. Calculate the necessary rated voltage of the capacitor by using the following formula.

Equation 2

$$V_{CVCC} > V_{IN}, V_{CVREG} > V_{VREG}$$

Where:

V_{CVCC}: Rated voltage of VCC bypass capacitor (V)

V_{IN}: Power supply voltage (V)

V_{CVREG}: Rated voltage of VREG bypass capacitor (V)

V_{VREG}: VREG voltage (V)

2.3.2 PG1, PG2, PG3, PG4, PGL2 and RST Pull-Up Resistor

PGx (where x = 1, 2, 3, or 4), PGL2, and RST terminals of the PMIC need a pull-up resister if the design uses the power good monitor or the watchdog function (see the datasheet for more information on each function). When you select the value for pull-up resistance, you should consider the leakage current (less than 1 µA) and the driving ability (3 mA) of each terminal. The resistance should be selected in the range of 2 kΩ to 100 kΩ.

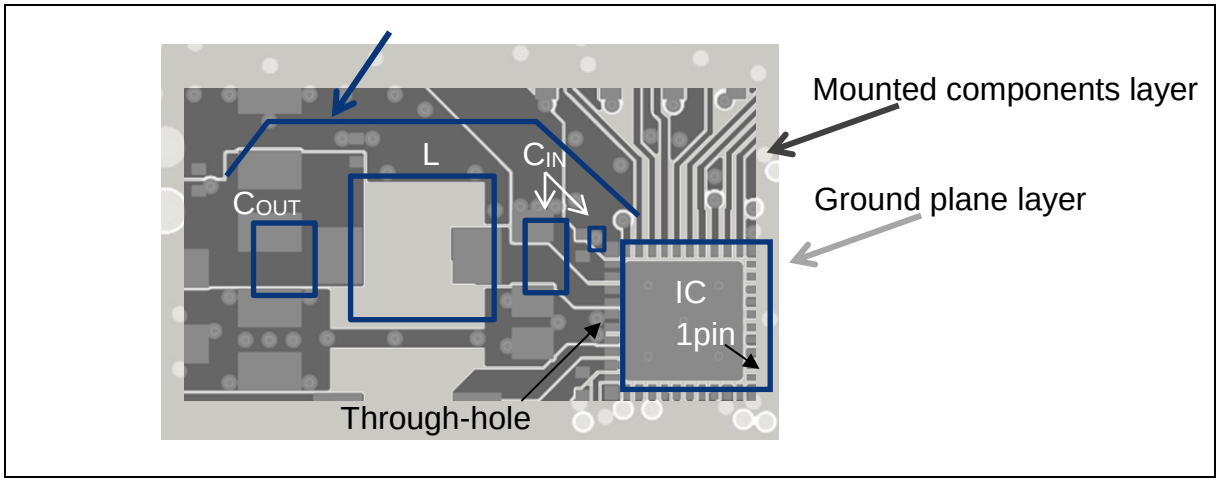
3 PCB Layout Guidelines

This section explains how to design PCB layout for a power management system with S6BP401A.

3.1 DC/DC Converter (DD1, DD2, DD3, and DD4)

Figure 4 shows an example layout of the DC/DC converter (DD2) section shown in Figure 2.

Figure 4. Layout Example of DD2



The switching components, consisting of an input capacitor (C_{IN}), IC, coil (L), and output capacitor (C_{OUT}), are placed close to each other. These components should be connected with a wide and short plane.

In particular, the current loop that includes the input capacitor (C_{IN}) and IC (PVCCx and PGNDx [where x = 1, 2, 3, or 4] terminal) should be carefully chosen to decrease the current loop. Another PCB layer, not a mounted components layer, should be used as a ground plane. The ground terminal of the switching component should be connected to this ground plane by through-holes that are put near the ground terminal of the switching component.

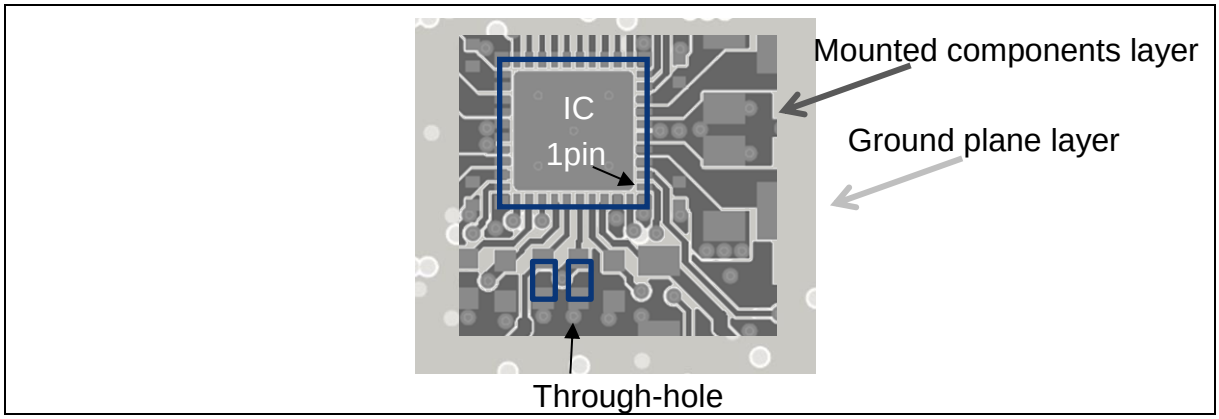
The feedback line from the FBx (where x = 1, 2, 3, or 4) terminal of the IC should be connected individually to the terminal of the output capacitors. This wiring is sensitive to noise. It should be away from the pattern of the LXx (where x = 1, 2, 3, or 4) terminal and the switching components.

There is leakage flux near a coil or the back of the PCB-mounted coil. Sensitive wiring and components should be located away from the coil or the back of the PCB-mounted coil.

3.2 LDO (LDO1 and LDO2)

Figure 5 shows an example layout of the LDO (LDO1) section shown in Figure 3.

Figure 5. Layout Example of LDO1

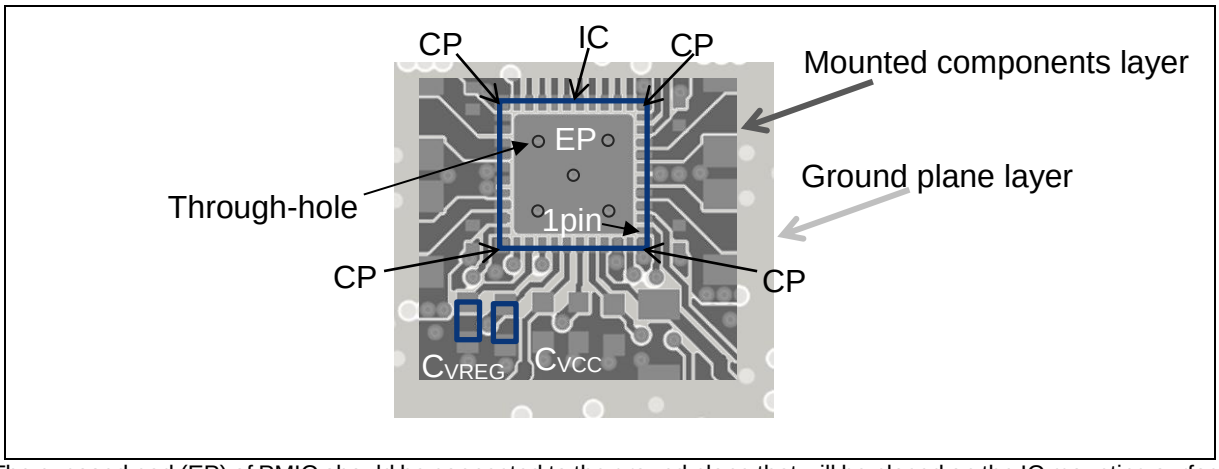


The input capacitor (C_{IN}) and output capacitor (C_{OUT}) should be placed close to the PVCCLx (where x = 1 or 2) terminal and the LDOx (where x = 1 or 2) terminal of the IC. These components should be connected with a wide and short plane. The ground terminal of each capacitor should be connected to the ground plane of another layer by through-holes that are placed near the ground terminal of each capacitor.

3.3 Common (Ground, VCC, and VREG Bypass Capacitors)

Figure 6 shows an example layout of the common section.

Figure 6. Layout Example of Common Section



The exposed pad (EP) of PMIC should be connected to the ground plane that will be placed on the IC mounting surface. The EP should be connected to the ground plane of another layer for heat dissipation and stable operation purposes.

The VCC and VREG bypass capacitors (C_{VCC}, C_{VREG}) should be placed close to the VCC and VREG terminals of the IC. These components should be connected with a short line. The ground terminal of each capacitor and the corner pad (CP) of the IC should be connected to the ground plane of another layer by through-holes that are placed near each ground terminal of the capacitor and each CP terminal IC.

Document History

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**	4880290	YMAE	08/11/2015	New application note
*A	5157275	YMAE	03/01/2016	Changed title. Added PCB layout guidelines.
*B	5815114	AESATMP8	07/13/2017	Updated logo and Copyright.
*C	6306566	YMAE	09/11/2018	Sunset review Updated template

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