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Spec Title: AN98581 - MIGRATION FROM MICROCHIP SST25VF-B, SST25VF-C, AND SST26VF TO CYPRESS S25FL1-K SPI FLASH FAMILY

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AN98581

# Migration from Microchip SST25VF-B, SST25VF-C, and SST26VF to Cypress S25FL1-K SPI Flash Family

AN98581 provides conversion guidelines for migrating from the Microchip SST25VF-B, SST25VF-C and SST26VF SPI series to the Cypress S25FL1-K SPI Flash Family. Cypress S25FL1-K flash is a feature rich and cost-optimized serial peripheral interface (SPI), non-volatile NOR flash family manufactured on a 90 nm 3-volt floating gate process.



## Contents



## 1 Introduction

Cypress S25FL1-K flash is a feature rich and cost-optimized serial peripheral interface (SPI), non-volatile NOR flash family manufactured on a 90 nm 3-volt floating gate process. The S25FL1-K family is composed of three members:

- S25FL116K 16 Mbit (2 MB)
- S25FL132K 32 Mbit (4 MB)
- S25FL164K 64 Mbit (8 MB)

This application note provides conversion guidelines for migrating from the Microchip SST25VF-B, SST25VF-C and SST26VF SPI series to the Cypress S25FL1-K SPI Flash Family.

This application note is based on information available to date from data sheets and other application notes publicly available from Cypress and Microchip. Please refer also to the latest relevant specifications. The document discusses the specification differences when migrating from SST25VF-B, SST25VF-C and SST26VF to S25FL1-K.

## 2 Feature Comparison

Microchip SST25VF-B, SST25VF-C, and SST26VF are well suited for migration to Cypress S25FL1-K products. Some of the reasons are compatible pinouts, packages, command set, and 4-kB sector structure.

Both Cypress S25FL1-K and Microchip devices support Single (Standard) I/O mode. Cypress S25FL1-K also supports Dual I/O and Quad I/O modes, while Microchip has Dual I/O mode on the SST25VF-C family and Quad mode on the SST26VF family.

The main differences between Cypress S25FL1-K and Microchip SST25VF-B family are:

- Data program scheme (See *Program Method* on page 4.)
- Status register structure (See *Status Registers* on page 4.)
- Block protection scheme (See *Block Protection Scheme* on page 6.)

The main differences between Cypress S25FL1-K and Microchip SST25VF-C family are:

- Data program scheme (See *Program Method* on page 4.)
- Status register structure (See *Status Registers* on page 4.)
- Block protection scheme (See *Block Protection Scheme* on page 6.)
- OTP handle methods (See *OTP (One-Time Program) Area* on page 8.)
- Hardware reset (See *Reset Operations* on page 8.)

The main differences between Cypress S25FL1-K and Microchip SST26VF family are:

- Block structure (See *Block Structure* on page 3.)
- Status register structure (See *Status Registers* on page 4.)
- Block protection scheme (See *Block Protection Scheme* on page 6.)
- OTP handle methods (See *OTP (One-Time Program) Area* on page 8.)
- Software reset (See *Reset Operations* on page 8.)

Table 1 summarizes the feature similarities and differences between S25FL-1K and SST25VF-B, SST25VF-C, SST26VF.

Table 1. High Level Feature Support Comparison

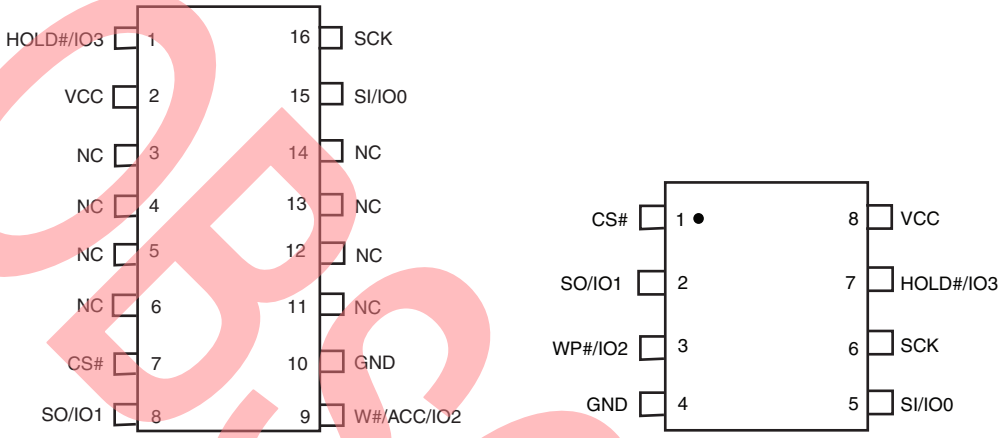
| Feature / Parameter | S25FL-1K | SST25VF-B | SST25VF-C | SST26VF |
|---|---|---|---|---|
| Single (Standard) IO Operations | √ | √ | √ | √ |
| Dual IO Operations | √ | x | √ | x |
| Quad IO Operations | √ | x | x | √ |
| Standard Normal Read SCK Frequency (max) | 50 MHz | 25 MHz | 33 MHz | 33 MHz |
| Standard Fast Read SCK Frequency (max) | 108 MHz | 80 MHz | 80 MHz | 80 MHz |
| Dual Fast Read SCK Frequency (max) | 108 MHz | x | 75 MHz (Dual-Output)<br>50 MHz (Dual I/O) | x |
| Quad Fast Read SCK Frequency (max) | 108 MHz | x | x | 80 MHz |
| Wrapped Read Modes | √ | x | x | √ |
| Index Jump Read | x | x | x | √ |
| Program Page Size | 256 bytes | 1 byte | 256 bytes | 256 bytes |
| AAI (Auto Address Increment)-Word-Program | x | ? | x | x |
| Program/Erase Suspend | x | x | x | √ |
| Dual-Input Page-Program | x | x | √ | x |
| 4 kB, 64 kB, and Chip Erase | √ | √ | √ | √ |
| 32-kB Block Erase | x | √ | √ | √ |
| Write Protection | √ | √ | √ | √ |
| Read Protection | x | x | x | √ |
| Volatile Configuration | √ | √ | √ | x |
| Hardware Reset | x | x | √ | x |
| Software Reset | x | x | x | √ |
| One Time Programmable Region(s) | 3 x 256 bytes | x | 32 bytes | 32 bytes |
| Temperature Range Option | -40°C to +85°C<br>-40°C to +105°C | 0°C to +70°C<br>-40°C to +85°C | 0°C to +70°C<br>-40°C to +8°5°C | -40°C to +85°C |

## 2.1 Hardware Package

The pinout of the SST25VF-B and SST26VF families is identical. For the SST25VF-C family, HOLD# can be used as RESET# when CS# is high.

The S25FL1-K can have its HOLD# pin connected to a system RESET function without causing it any problems. This allows direct replacement of the SST25VF064C without PCB redesign. Figure 1 shows those SOIC packages and pinouts. Please refer to the data sheets for detailed package information.

Figure 1. SOIC 150/208/300 mil Package and Pinout (16-pin and 8-pin Versions)




***Note:***

1. *On SST25VF-C, RST#/HOLD# replaces HOLD#.*

Table 2 and Table 3 summarize the available packages from Cypress and Microchip.

Table 2. Cypress S25FL1-K Available Packages

| | Cypress S25FL1-K | | |
|---|---|---|---|
| | **S25FL116K** | **S25FL132K** | **S25FL164K** |
| SOIC8 150 mil | √ | √ | x |
| SOIC8 208 mil | √ | √ | √ |
| SOIC16 300 mil | x | x | √ |
| USON 5x6 | √ | √ | √ |
| 24-Ball BGA 6 x 8<br>5 x5 ball and 6 x 4 ball | √ | √ | √ |

Table 3. Microchip Available Packages

| | SST25VF-B | | SST25VF-C | SST26VF | |
|---|---|---|---|---|---|
| | **25VF016B** | **25VF032B** | **25VF064C** | **25VF016** | **25VF032** |
| SOIC8 200 mil | √ | √ | √ | √ | √ |
| SOIC16 300 mil | x | x | √ | x | x |
| WSON 6 x 5 | √ | √ | x | √ | √ |
| WSON 6 x 8 | x | x | √ | x | x |

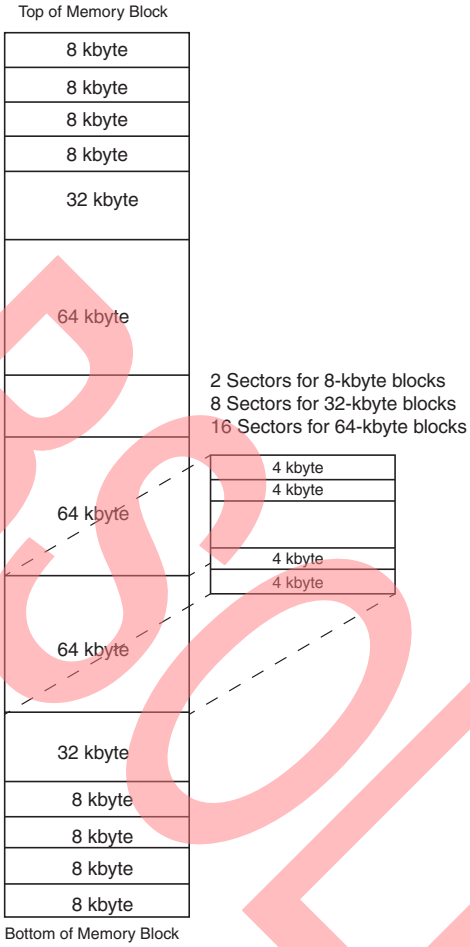
## 2.2 Block Structure

Both Microchip products (SST25VF-B, SST25VF-C, and SST26VF) and Cypress S25FL1-K support 4-kB sector erase.

The SST25VF-B and SST25VF-C support both 32-kB block erase and 64-kB block erase, while Cypress S25FL1-K supports 64-kB block erase only.

Figure 2 shows block structure of SST26VF. Block erase command needs to be sent according to the structure. Software change is needed when migrating from SST26VF to S25FL1-K if block erase command (D8H) is used.

Figure 2. Block Structure of SST26VF






## 2.3 Program Method

Both Microchip products (SST25VF-C and SST26VF) and Cypress S25FL1-K supports page program with program length from 1 to 256 bytes.

SST25VF-C supports Dual-Input Page-Program, while S25FL1-K does not.

The page program command (02H) in the SST25VF-B can only program 1 byte to flash. AAI (Auto Address Increment)-Word-Program is used to program multiple bytes to flash. When migrating to S25FL1-K, AAI-Word-Program function needs to be removed and the page program command used instead.

## 2.4 Multi-I/O Operation

The SST25VF-C supports Dual output read and Dual I/O read, which is also supported by S25FL1-K.

The SST26VF supports Quad I/O bus operation and when enabled, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or a “Reset Quad I/O instruction” is executed. S25FL1-K supports Quad output read and Quad I/O read operations but does not support Quad I/O bus operation. Changes to the software will be required when migrating to S25FL1-K if Quad I/O bus operation is used.

## 2.5 Status Registers

The SST25VF-B, SST25VF-C, and SST26VF have only one status register (SR1).

Cypress FL1-K devices have two additional status registers (SR2 and SR3), which can be used to provide status on additional device features and to configure the burst wrap feature. The Write Status Register instruction allows

the three status registers to be written in one command sequence. Only non-volatile status register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 through 2 of Status Register 1), CMP, LB3, LB2, LB1, LB0, QE, SRP1 (bits 6 through 0 of Status Register 2) and W6, W5, W4, and LC (bits 6 through 0 of Status Register 3) can be written. All other status register bit locations are read-only and will not be affected by the Write Status Register instruction.

Table 4 illustrates the status register bit assignments for Microchip products and S25FL1-K.

Table 4. Status Register Bit Assignments for Microchip Products and S25FL1-K

| Bits | Cypress | | Microchip | | | | | |
|---|---|---|---|---|---|---|---|---|
| | S25FL1-K | | SST25VF-B | | SST25VF-C | | SST26VF | |
| | Name | Function | Name | Function | Name | Function | Name | Function |
| SR1[7] | SRP0 | Status Register Protect0 | BPL | BP Lock Bit | BPL | BP Lock Bit | BUSY | Embedded Operation Status |
| SR1[6] | SEC | Sector/ Block Protect | AAI | Auto Address Increment Programming status | SEC | Security ID (OTP) status | RES | Reserved |
| SR1[5] | TB | Top/Bottom Protect | BP3 | Block Protect Bits | BP3 | Block Protect Bits | SEC | Security ID (OTP) status |
| SR1[4] | BP2 | Block Protect Bits | BP2 | | BP2 | | WPLD | Write Protection Lock-Down status |
| SR1[3] | BP1 | | BP1 | | BP1 | | WSP | Write Suspend-Program status |
| SR1[2] | BP0 | | BP0 | | BP0 | | WSE | Write Suspend-Erase status |
| SR1[1] | WEL | Write Enable Latch | WEL | Write Enable Latch | WEL | Write Enable Latch | WEL | Write Enable Latch |
| SR1[0] | BUSY | Embedded Operation Status | BUSY | Embedded Operation Status | BUSY | Embedded Operation Status | RES | Reserved |
| SR2[7] | RFU | Reserved | x | x | x | x | x | x |
| SR2[6] | CMP | Complement Protect | x | x | x | x | x | x |
| SR2[5] | LB3 | Security Register Lock Bits | x | x | x | x | x | x |
| SR2[4] | LB2 | | x | x | x | x | x | x |
| SR2[3] | LB1 | | x | x | x | x | x | x |
| SR2[2] | LB0 | | x | x | x | x | x | x |
| SR2[1] | QE | Quad Enable | x | x | x | x | x | x |
| SR2[0] | SRP1 | Status Register Protect1 | x | x | x | x | x | x |
| SR3[7] | RFU | Reserved | x | x | x | x | x | x |
| SR3[6] | W6 | Burst Wrap Length | x | x | x | x | x | x |
| SR3[5] | W5 | | x | x | x | x | x | x |
| SR3[4] | W4 | Burst Wrap Enable | x | x | x | x | x | x |
| SR3[3] | Latency Control (LC) | Variable Read Latency Control | x | x | x | x | x | x |
| SR3[2] | | | x | x | x | x | x | x |
| SR3[1] | | | x | x | x | x | x | x |
| SR3[0] | | | x | x | x | x | x | x |

## 2.6 Block Protection Scheme

The SST25VF-B and SST25VF-C protect sector data based on Block Protect Bits (BP3-0). The BP Bits are non-volatile read/write bits in the status register (SR[5-2]) that provide Write Protection control and status. Table 5 shows sector protection area of SST25VF-B and SST25VF-C. Please refer also to the status register handling.

Table 5. Sector Protection Area of SST25VF-B and SST25VF-C

| BP Status | | | | SST25VF-B | | | | SST25VF-C | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | VF016B | | VF032B | | VF064C | |
| BP 3 | BP 2 | BP 1 | BP 0 | Protected Portion | Protected Addresses | Protected Portion | Protected Addresses | Protected Portion | Protected Addresses |
| 0 | 0 | 0 | 0 | None | None | None | None | None | None |
| 0 | 0 | 0 | 1 | Upper 1/32 | 1F0000H-1FFFFFH | Upper 1/64 | 3F0000H-3FFFFFH | Upper 1/128 | 7F0000H-7FFFFFH |
| 0 | 0 | 1 | 0 | Upper 1/16 | 1E0000H-1FFFFFH | Upper 1/32 | 3E0000H-3FFFFFH | Upper 1/64 | 7E0000H-7FFFFFH |
| 0 | 0 | 1 | 1 | Upper 1/8 | 1C0000H-1FFFFFH | Upper 1/16 | 3C0000H-3FFFFFH | Upper 1/32 | 7C0000H-7FFFFFH |
| 0 | 1 | 0 | 0 | Upper 1/4 | 180000H-1FFFFFH | Upper 1/8 | 380000H-3FFFFFH | Upper 1/16 | 780000H-7FFFFFH |
| 0 | 1 | 0 | 1 | Upper 1/2 | 100000H-1FFFFFH | Upper 1/4 | 300000H-3FFFFFH | Upper 1/8 | 700000H-7FFFFFH |
| 0 | 1 | 1 | 0 | All Blocks | 000000H-1FFFFFH | Upper 1/2 | 200000H-3FFFFFH | Upper 1/4 | 600000H-7FFFFFH |
| 0 | 1 | 1 | 1 | All Blocks | 000000H-1FFFFFH | All Blocks | 000000H-3FFFFFH | Upper 1/2 | 400000H-7FFFFFH |
| 1 | 0 | 0 | 0 | None | None | None | None | All Blocks | 000000H-7FFFFFH |
| 1 | 0 | 0 | 1 | Upper 1/32 | 1F0000H-1FFFFFH | Upper 1/64 | 3F0000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 0 | 1 | 0 | Upper 1/16 | 1E0000H-1FFFFFH | Upper 1/32 | 3E0000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 0 | 1 | 1 | Upper 1/8 | 1C0000H-1FFFFFH | Upper 1/16 | 3C0000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 1 | 0 | 0 | Upper 1/4 | 180000H-1FFFFFH | Upper 1/8 | 380000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 1 | 0 | 1 | Upper 1/2 | 100000H-1FFFFFH | Upper 1/4 | 300000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 1 | 1 | 0 | All Blocks | 000000H-1FFFFFH | Upper 1/2 | 200000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |
| 1 | 1 | 1 | 1 | All Blocks | 000000H-1FFFFFH | All Blocks | 000000H-3FFFFFH | All Blocks | 000000H-7FFFFFH |

The SST26VF has a Block-Protection register that provides a software mechanism to write-lock the array and write-lock, and/or read-lock, the parameter blocks. The Block-Protection Register is 48-bits wide on the SST26VF016 and 80-bits wide on the SST26VF032: two bits each for the eight 8-kB parameter blocks (write-lock and read-lock), and one bit each for the remaining 32-kB and 64-kB overlay blocks (write-lock).

The Cypress S25FL1-K allows all, none, or a portion of the memory array be protected from Program and Erase instructions via the status register. It is similar to the sector protection scheme used by SST25VF-B and SST25VF-C but more flexible.

The Block Protect Bits (BP2-0) provide Write Protection control and status. The factory default setting for the block protection bits is 0 (none of the array is protected.). The non-volatile Top/Bottom bit (TB) controls whether the Block Protect Bits (BP2-0) protect from the Top (TB=0) or the Bottom (TB=1) of the array. The non-volatile Sector/Block Protect bit (SEC) selects whether the Block Protect Bits (BP2-0) protect 4-kB sectors (SEC=1) or 64-kB blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array.

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register. It is used in conjunction with SEC, TB, and BP2-0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed.

Refer to the Cypress data sheet for the valid combinations. Table 6 and Table 7 show S25FL1-K's sector protection using S25FL116K as an example.

Table 6. FL116K Block Protection (CMP = 0)

| Status Register | | | | | Protected Portion | Protected Addresses |
|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | | |
| x | x | 0 | 0 | 0 | None | None |
| 0 | 0 | 0 | 0 | 1 | Upper 1/32 | 1F0000h - 1FFFFFH |
| 0 | 0 | 0 | 1 | 0 | Upper 1/16 | 1E0000h - 1FFFFFH |
| 0 | 0 | 0 | 1 | 1 | Upper 1/8 | 1C0000h - 1FFFFFH |
| 0 | 0 | 1 | 0 | 0 | Upper 1/4 | 180000h - 1FFFFFH |
| 0 | 0 | 1 | 0 | 1 | Upper 1/2 | 100000h - 1FFFFFH |
| 0 | 1 | 0 | 0 | 1 | Lower 1/32 | 000000h - 00FFFFH |
| 0 | 1 | 0 | 1 | 0 | Lower 1/16 | 000000h - 01FFFFH |
| 0 | 1 | 0 | 1 | 1 | Lower 1/8 | 000000h - 03FFFFH |
| 0 | 1 | 1 | 0 | 0 | Lower 1/4 | 000000h - 07FFFFH |
| 0 | 1 | 1 | 0 | 1 | Lower 1/2 | 000000h - 0FFFFFH |
| x | x | 1 | 1 | x | All | 000000h - 1FFFFFH |
| 1 | 0 | 0 | 0 | 1 | Upper 1/512 | 1FF000h - 1FFFFFH |
| 1 | 0 | 0 | 1 | 0 | Upper 1/256 | 1FE000h - 1FFFFFH |
| 1 | 0 | 0 | 1 | 1 | Upper 1/128 | 1FC000h - 1FFFFFH |
| 1 | 0 | 1 | 0 | x | Upper 1/64 | 1F8000h - 1FFFFFH |
| 1 | 1 | 0 | 0 | 1 | Lower 1/512 | 000000h - 000FFFH |
| 1 | 1 | 0 | 1 | 0 | Lower 1/256 | 000000h - 001FFFH |
| 1 | 1 | 0 | 1 | 1 | Lower 1/128 | 000000h - 003FFFH |
| 1 | 1 | 1 | 0 | x | Lower 1/64 | 000000h - 007FFFH |

Table 7. FL116K Block Protection (CMP = 1)

| Status Register | | | | | Protected Portion | Protected Addresses |
|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | | |
| x | x | 0 | 0 | 0 | All | 000000h - 1FFFFFH |
| 0 | 0 | 0 | 0 | 1 | Lower 31/32 | 000000h - 1EFFFFH |
| 0 | 0 | 0 | 1 | 0 | Lower 15/16 | 000000h - 1DFFFFH |
| 0 | 0 | 0 | 1 | 1 | Lower 7/8 | 000000h - 1BFFFFH |
| 0 | 0 | 1 | 0 | 0 | Lower 3/4 | 000000h - 17FFFFH |
| 0 | 0 | 1 | 0 | 1 | Lower 1/2 | 000000h - 0FFFFFH |
| 0 | 1 | 0 | 0 | 1 | Upper 31/32 | 010000h - 1FFFFFH |
| 0 | 1 | 0 | 1 | 0 | Upper 15/16 | 020000h - 1FFFFFH |
| 0 | 1 | 0 | 1 | 1 | Upper 7/8 | 040000h - 1FFFFFH |
| 0 | 1 | 1 | 0 | 0 | Upper 3/4 | 080000h - 1FFFFFH |
| 0 | 1 | 1 | 0 | 1 | Lower 1/2 | 100000h - 1FFFFFH |
| x | x | 1 | 1 | x | None | None |
| 1 | 0 | 0 | 0 | 1 | Lower 511/512 | 000000h - 1FEFFFH |
| 1 | 0 | 0 | 1 | 0 | Lower 255/156 | 000000h - 1FDFFFH |
| 1 | 0 | 0 | 1 | 1 | Lower 127/128 | 000000h - 1FBFFFH |

Table 7. FL116K Block Protection (CMP = 1)

| Status Register | | | | | Protected Portion | Protected Addresses |
|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | | |
| 1 | 0 | 1 | 0 | x | Lower 63/64 | 000000h - 1F7FFFH |
| 1 | 1 | 0 | 0 | 1 | Upper 511/512 | 001000h - 1FFFFFH |
| 1 | 1 | 0 | 1 | 0 | Upper 255/256 | 002000h - 1FFFFFH |
| 1 | 1 | 0 | 1 | 1 | Upper 127/128 | 004000h - 1FFFFFH |
| 1 | 1 | 1 | 0 | x | Upper 63/64 | 008000h - 1FFFFFH |

## 2.7 Variable Latency

The Cypress S25FL1-K adds support for variable latency read timing. Customers can use the default latency code value when migrating from Microchip products to S25FL1-K without any change in read timing. Or, they can set latency code (SR3[3-0]) and change read timing to enable faster initial access time or higher clock rate read commands. See full feature details in S25FL1-K data sheet.

## 2.8 Burst Read Mode

The Microchip SST26VF supports 8/16/32/64-byte linear burst with wrap-around. Set Burst command cycle (C0H) is used to set burst length. Read Burst command cycle (0CH) is used to execute a Read Burst operation.

The Cypress S25FL1-K supports Fast Quad IO Read (EBH) in Burst with Wrap mode. Status Register 3 provides a bit (SR3[4]) to enable a read with wrap option for the Quad I/O Read command. To set burst length, Status Register 3 provides bits (SR3[6:5]) to select the alignment boundary. Burst wrap length can be aligned on 8-, 16-, 32-, or 64-byte boundaries. The S25FL1-K also supports Set Burst with Wrap command (77H) preceding the Fast Quad IO Read command. See full feature details in S25FL1-K data sheet.

## 2.9 OTP (One-Time Program) Area

The Microchip SST25VF-C and SST26VF supports 32 bytes' OTP area. Eight bytes are unique, factory pre-programmed identifier and 24 bytes are user-programmable. Read SID (88H) is used to read OTP area. Program SID (A5H) is used to program OTP area. Lockout SID (85H) is used to lockout OTP area programming.

The Cypress S25FL1-K provides three 256 bytes' Security Registers. Each security register can be read (opcode 48H), programmed (opcode 42H), erased (opcode 44H), and permanently locked by setting status register bits LB1, LB2 and LB3 to 1.

## 2.10 Reset Operations

The Microchip SST25VF-C has a RST# pin that provides a hardware method for resetting the device.

The Microchip SST26VF supports a software reset operation. It is used to put the device in normal operating ready mode. This operation consists of two commands: Reset-Enable (RSTEN 66H) and Reset (RST 99H).

The Cypress S25FL1-K does not have a hardware Reset pin. If the host system memory controller resets, without a complete power down and power up sequence, while S25FL1-K is set to Continuous Mode Read, S25FL1-K will not recognize any initial standard SPI commands from the controller. To address this possibility, it is recommended to issue a Continuous Read Mode Reset (FFFFh) command as the first command after a system Reset. Doing so will release the device from the Continuous Read Mode and allow Standard SPI commands to be recognized.

If Burst Wrap Mode is used, it is also recommended to issue a Set Burst with Wrap (77h) command that sets the W4 bit to one as the second command after a system Reset. Doing so will release the device from the Burst Wrap Mode and allow standard sequential read SPI command operation.

Issuing these commands immediately after a non-power-cycle (warm) system reset ensures the device operation is consistent with the power on default device operation.

# 3 Command Set Comparison

Microchip devices and S25FL1-K share similar instructions (op-codes) in their command set, which determine a compatible set of internal algorithms. Nevertheless, not all commands are supported when comparing one product family with the other.

Table 8 shows a comparison summary of the command set of a Cypress S25FL1-K device and Microchip SST25VF-B, SST25VF-C, and SST26VF.

Table 8. Command Set of S25FL1-K and Microchip Devices (Sheet 1 of 2)

| Command Description | S25FL1-K | SST25VF-B | SST25VF-C | SST26VF |
|---|---|---|---|---|
| **Configuration, Status, Erase, Program Commands** | | | | |
| Read Status Register 1 | 05H | 05H | 05H | 05H |
| Read Status Register 2 | 35H | x | x | x |
| Read Status Register 3 | 33H | x | x | x |
| Write Enable | 06H | 06H | 06H | 06H |
| Write Enable for Volatile Status Register | 50H | 50H | 50H | x |
| Write Disable | 04H | 04H | 04H | 04H |
| Write Status Registers | 01H | 01H | 01H | x |
| Set Burst with Wrap | 77H | x | x | x |
| Page Program | 02H | 02H (1) | 02H | 02H |
| Auto Address Increment Programming | x | ADH | x | x |
| Dual Input Program | x | x | A2H | x |
| Sector Erase (4 kB) | 20H | 20H | 20H | 20H |
| Block Erase (32 kB) | x | 52H | 52H | x |
| Block Erase (64 kB) | D8H | D8H | D8H | x |
| Block Erase | x | x | x | D8H (2) |
| Chip Erase | C7H/60H | C7H/60H | C7H/60H | C7H |
| Suspends Program/Erase | x | x | x | B0H |
| Resumes Program/Erase | x | x | x | 30H |
| **Read Commands** | | | | |
| Read Data | 03H | 03H | 03H | 03H |
| Fast Read | 0BH | 0BH | 0BH | 0BH |
| Fast Read Dual Output | 3BH | x | 3BH | x |
| Fast Read Quad Output | 6BH | x | x | x |
| Fast Read Dual I/O | BBH | x | BBH | x |
| Fast Read Quad I/O | EBH | x | x | x |
| Continuous Read Mode Reset | FFH | x | x | x |
| Set Burst Length | x | x | x | C0H |
| nB Burst with Wrap | x | x | x | 0CH |
| Jump to address within 256 Byte page indexed by n | x | x | x | 08H |
| Jump to address within block indexed by n | x | x | x | 09H |
| Jump to block indexed by n | x | x | x | 10H |
| **ID, Security, and Other Commands** | | | | |
| Deep Power-down | B9H | x | x | x |
| Release Power down / Device ID | ABH | x | x | x |
| Manufacturer/ Device ID | 90H | 90H/ABH | 90H/ABH | x |
| JEDEC ID Read | 9FH | 9FH | 9FH | 9FH |
| Quad I/O JEDEC ID Read | x | x | x | AFH |
| Read SFDP Register | 5AH | x | x | x |

Table 8. Command Set of S25FL1-K and Microchip Devices (Sheet 2 of 2)

| Command Description | S25FL1-K | SST25VF-B | SST25VF-C | SST26VF |
|---|---|---|---|---|
| Read Security Registers | 48H | x | x | x |
| Erase Security Registers | 44H | x | x | x |
| Program Security Registers | 42H | x | x | x |
| Enable SO to output RY/BY# status during AAI programming | x | 70H | x | x |
| Disable SO to output RY/BY# status during AAI programming | x | 80H | x | x |
| Enable HOLD# ping functionality of the RST#/HOLD# pin | x | x | AAH | x |
| Read Security ID | x | x | 88H | 88H |
| Program User Security ID area | x | x | A5H | A5H |
| Lockout Security ID Programming | x | x | 85H | 85H |
| No Operation | x | x | x | 00H |
| Reset Enable | x | x | x | 66H |
| Reset Memory | x | x | x | 99H |
| Enable Quad I/O | x | x | x | 38H |
| Reset Quad I/O | x | x | x | FFH |
| Read Block Protection Register | x | x | x | 72H |
| Write Block Protection Register | x | x | x | 42H |
| Lock Down Block Protection Register | x | x | x | 8DH |

***Notes:***

1. *02H command sequence of SST25VF-B can program 1 byte only every time.*
2. *Block size being erased of SST26VF is based on its block structure.*

# 4 Timing Considerations

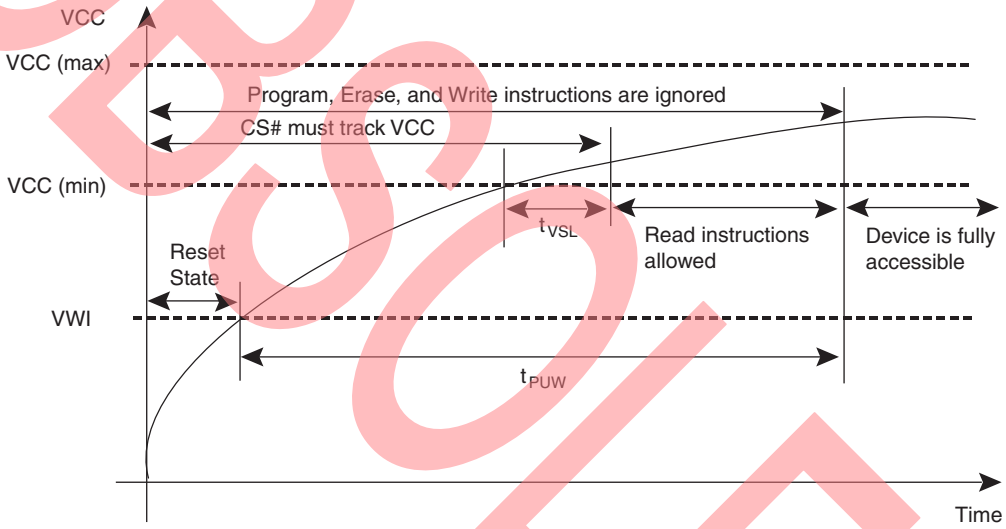
## 4.1 Power-Up Timing

One of the most sensitive electrical specifications is the power-up timing needed to correctly initialize the device. Table 9 and Figure 3 show the power-up characteristics of the S25FL1-K family.

Table 9. S25FL1-K Power-Up Timing Requirement

| Parameter | Symbol | Spec | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ (min) to CS# Low | $t_{VSL}$ | 10 | | µs |
| Time Delay Before Write Command | $t_{PUW}$ | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | $V_{WI}$ | 1.0 | 2.0 | V |

Figure 3. Power-Up Timing and Voltage Levels




On the Microchip side, $V_{CC}$ ramp rate is more restrictive. All functionalities and DC specifications are specified for a $V_{CC}$ ramp rate of greater than 1V per 100 ms (0v - 3.0V in less than 300 ms for SST25VF-B/SST25VF-C, and 0V to 2.7V in less than 270 ms for SST26VF). Table 10 shows the power-up characteristics of the Microchip products.

Table 10. SST25VF-B, SST25VF-C, and SST26VF Power-Up Timing Requirement

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| $V_{CC}$ Min to Read Operation | TPU-READ | 100 | µs |
| $V_{CC}$ Min to Write Operation | TPU-WRITE | 100 | µs |

## 4.2 Data In Setup/Hold Time

Two AC timing parameters that are critical in SPI designs are Data In Setup Time and Data In Hold Time. They specify how long data needs to be valid before and after the rising edge of the clock signal, respectively. The minor different requirement should not be an issue in the design but may just need to be verified. Table 11 shows the Data in Setup/Hold timing characteristics for both S25FL1-K and Microchip devices.

Table 11. Data in Setup/Hold Timing Characteristics Comparison

| **S25FL1-K** | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | | | **Unit** |
| Data In Setup Time | 2 | | | ns |
| Data In Hold Time | 5 | | | ns |
| **SST25VF016B** | | | | |
| | **SCK Frequency Limits** | | | |
| | 25 MHz | 50 MHz | 80 MHz | |
| **Parameter** | Min | | | **Unit** |
| Data In Setup Time | 5 | 2 | 2 | ns |
| Data In Hold Time | 5 | 5 | 4 | ns |
| **SST25VF032B** | | | | |
| | **SCK Frequency Limits** | | | |
| | 25 MHz | 66 MHz | 80 MHz | |
| **Parameter** | **Min** | | | **Unit** |
| Data In Setup Time | 5 | 2 | 2 | ns |
| Data In Hold Time | 5 | 4 | 4 | ns |
| **SST25VF-C** | | | | |
| | **SCK Frequency Limits** | | | |
| | 33 MHz | 50 MHz | 75/80 MHz | |
| **Parameter** | **Min** | | | **Unit** |
| Data In Setup Time | 3 | 3 | 2 | ns |
| Data In Hold Time | 5 | 5 | 4 | ns |
| **SST26VF** | | | | |
| | **SCK Frequency Limits** | | | |
| | 33 MHz | 80 MHz | | |
| **Parameter** | **Min** | | | **Unit** |
| Data In Setup Time | 3 | 3 | | ns |
| Data In Hold Time | 4 | 4 | | ns |

## 4.3 Further Timing Comparison

In general, the timing characteristics of both Microchip and Cypress flash families are almost identical, with just a little deviation.

One difference is that the S25FL1-K family has a faster CS# deselect time than SST25VF-B and SST25VF-C. There is no need to do any changes but it is important to note that read performance of the application can be increased easily here.

When SPI clock frequency is 80 MHz, CS# deselect time for read after writes of SST26VF is 12.5 ns minimum. The minor different requirement should not be an issue in the design but may just need to be verified when migrating from SST26VF to S25FL-1K.

Table 12 shows a comparison between S25FL1-K and Microchip devices with regards to the various CS# deselect times.

Table 12. CS# Deselect Timing Characteristics Comparison

| S25FL1-K | | | | |
|---|---|---|---|---|
| **Parameter** | **Min** | | | **Unit** |
| CS# deselect time between Reads | 7 | | | ns |
| CS# deselect time for Read after Writes | 40 | | | ns |
| **SST25VF016B** | | | | |
| **Parameter** | **SCK Frequency Limits** | | | **Unit** |
| | 25M Hz | 50 MHz | 80 MHz | |
| | **Min** | | | |
| CS# deselect time | 100 | 50 | 50 | ns |
| **SST25VF032B** | | | | |
| **Parameter** | **SCK Frequency Limits** | | | **Unit** |
| | 25MHz | 66MHz | 80MHz | |
| | **Min** | | | |
| CS# deselect time | 100 | 50 | 50 | ns |
| **SST25VF-C** | | | | |
| **Parameter** | **SCK Frequency Limits** | | | **Unit** |
| | 33 MHz | 50 MHz | 75/80 MHz | |
| | **Min** | | | |
| CS# deselect time | 50 | 50 | 50 | ns |
| **SST26VF** | | | | |
| **Parameter** | **SCK Frequency Limits** | | | **Unit** |
| | 33 MHz | 80 MHz | | |
| | **Min** | | | |
| CS# deselect time | 100 | 12.5 | ns | |

# 5 Conclusion

Migrating from Microchip SST25VF-B, SST25VF-C, and SST26VF families to the Cypress S25FL1-K is straightforward and requires minimal accommodation in regards to either system software or hardware.

Additionally, once accommodations are made, if required, S25FL1-K flash will enable access to a wider range of SPI flash features and superior read throughput up to 54 Mbytes/s using Quad bit data path.

# Document History Page

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