AN98577

Migration from FL-P to FL-S Family SPI Interface Flash Memories

AN98577 discusses the specification differences that must be considered when migrating from an FL-P flash device to an FL-S flash device.

Contents

1 Introduction

The FL-P family of Serial Peripheral Interface (SPI) NOR flash devices is made on the Cypress® 90 nm MirrorBit® technology process node. The FL-P SPI NOR flash device family is composed of 5 members:

- 4 MB S25FL032P MIO SDP
- 8 MB S25FL064P MIO SDP
- 16 MB S25FL128P SIO SDP
- 16 MB S25FL129P MIO SDP
- 32 MB S70FL256P MIO DDP

The S25FL128P supports Single Input/Output (SIO) synchronous transactions while the remaining devices support Multiple Input/Output (MIO) data width commands for SIO, Dual Input/Output (DIO) and Quad Input/Output (QIO) synchronous transactions. The S25 prefix devices are Single Die per Package (SDP) devices, which are controlled via a single chip select. The S70 prefix device is a Dual Die Package (DDP) device consisting of two S25FL129P die, each of which is independently controlled by separate chip select inputs with all other inputs and outputs shared.

The FL-S family of SPI NOR flash devices is made on Cypress's 65 nm MirrorBit technology process node and uses the new Eclipse™ architecture for improved data integrity, program, and erase performance. The FL-S SPI NOR flash family is composed of 4 members:

- 16 MB S25FL128S MIO SDP
- 32 MB S25FL256S MIO SDP
- 64 MB S25FL512S MIO SDP
- 128 MB S70FL01GS MIO DDP

The S25 devices are SDP. The S70 device is a DDP consisting of two S25FL512S die. All FL-S family members support SIO, DIO and QIO synchronous transactions. Additionally, they are available with support for Double Data Rate (DDR) synchronous transactions.

This application note discusses the specification differences that must be considered when migrating from an FL-P flash device to an FL-S flash device. Discussions will focus on same density migrations, specifically the cases when migrating from the S25FL128P or S25FL129P to S25FL128S and when migrating from the S70FL256P to the S25FL256S. Concerns regarding migration from/to other densities can be extrapolated from the provided discussions. Detailed discussion of new functions and features supported by the FL-S family are not included in this document unless some hardware or software accommodation is required for migration from an FL-P device. Please refer to the appropriate FL-S data sheet for full descriptions of all new features and functions.

2 Feature Comparison and Differences

The FL-S SPI NOR supports a superset of the FL-P SPI NOR features. Table 1 summarizes the feature similarities and differences between the FL-P and FL-S. The differences are discussed in more detail in later sections.

Table 1. High Level Feature Comparison

Feature / Parameter	FL-P	FL-S
Single Die Package Density Options	4 MB, 8 MB, 16 MB	16 MB, 32 MB, 64 MB
Dual Die Package Density Options	32 MB	128 MB
Program Page Buffer Size	256 B (1)	256 B or 512 B (1)
Main Erase Block Qty x Size	64 kB or 256 kB (1)	64 kB or 256 kB (1)
Parameter Block Qty x Size	0 or 32 x 4 kB (2)	0 or 32 x 4 kB (2)
SIO Transactions	Yes	Yes
DIO and QIO Transactions	Yes (3)	Yes
DDR Transactions (option)	No	Yes
SIO Normal Read SCK Frequency (max)	50 MHz	50 MHz
SIO Fast Read SCK Frequency (max)	104 MHz	133 MHz
DIO/QIO Fast Read SCK Frequency (max)	80 MHz	104 MHz
DDR Fast/DIO/QIO Read SCK Frequency (max)	n/a	66 MHz
3 Byte Addressing	Yes	Yes
3 Byte Addressing + Bank Address	No	Yes
4 Byte Addressing	No	Yes
AutoBoot Function	No	Yes
Hardware Reset	No	Yes (4)
Independent V_{IO}	No	Yes (4)
High Voltage Accelerated Programming	Yes	No
Erase Suspend/Resume Function	No	Yes
Program Suspend/Resume Function	No	Yes
Deep Power Down Mode	Yes	No
ID and Common Flash Interface (CFI) Registers	Yes (5)	Yes
Data Protection: Block Protection (BP)	Yes	Yes
Data Protection: Advanced Sector Protection (ASP)	No	Yes
User One Time Programmable (OTP) Regions Qty x Size	30 x 16B, 1 x 10B (6)	31 x 32B
Electric Serial Number	2 x 8 bytes (7)	16 bytes

Notes:

1. *4 and 8 MB FL-P densities have 64 kB primary erase blocks with a 256B write page. 16 and 32 MB densities can be ordered with either 64 kB or 256 kB primary erase blocks with 256B or 512B write page sizes respectively. 64 and 128 MB densities have 256 kB primary erase blocks with a 512B write page size.*
2. *4 kB parameter blocks not supported in S25FL128P and all FL device with 256 kB erase blocks.*
3. *S25FL128P does not support DIO or QIO transactions.*
4. *Reset and V_{IO} inputs are available as ordering options for FL-S devices.*
5. *CFI only supported on FL129P.*
6. *OTP Regions not supported on FL128P.*
7. *ESN on FL-P is optional via customer order.*

Table 2 summarizes the supported commands for each device. Pertinent differences will be discussed in subsequent sections.

Table 2. Commands (Sheet 1 of 2)

Command	Description	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S S70FL01GS
		Instruction Codes		
Read Identification (3-byte addressing)				
RDID	Read Identification JEDEC	9Fh	9Fh	9Fh
READ_ID	Read Manufacturer and Device Identification	90h	90h	90h
RES	Read Electronic Signature	ABh	ABh	ABh
Read Operations (3-byte addressing)				
READ	Read Data Bytes	03h	03h	03h
FAST_READ	Read Data Bytes at Higher Speed	0Bh	0Bh	0Bh
DOR	Dual Output Read	-	3Bh	3Bh
QOR	Quad Output Read	-	6Bh	6Bh
DIOR	Dual I/O High Performance Read	-	BBh	BBh
QIOR	Quad I/O High Performance Read	-	EBh	EBh
FDDR	Fast Read DDR	-	-	0Dh
RDDRD	Read DDR Dual I/O	-	-	BDh
RDDRQ	Read DDR Quad I/O	-	-	EDh
Read Operations (4-byte addressing)				
READ4	Read Data Bytes	-	-	13h
FAST_READ4	Read Data Bytes at Higher Speed	-	-	0Ch
DOR4	Dual Output Read	-	-	3Ch
QOR4	Quad Output Read	-	-	6Ch
DIOR4	Dual I/O High Performance Read	-	-	BCh
QIOR4	Quad I/O High Performance Read	-	-	ECh
FDDR4	Fast Read DDR	-	-	0Eh
RDDRD4	Read DDR Dual I/O	-	-	BEh
RDDRQ4	Read DDR Quad I/O	-	-	EEh
Write Control				
WREN	Write Enable	06h	06h	06h
WRDI	Write Disable	04h	04h	04h
Program Operations (3-byte addressing)				
PP	Page Program	02h	02h	02h
QPP	Quad Page Programming	-	32h	32h, 38h
Program Operations (4-byte addressing)				
PP4	Page Program	-	-	12h
QPP4	Quad Page Programming	-	-	34h
PGSP	Program Suspend	-	-	85h
PGRS	Program Resume	-	-	8Ah
Erase Operations (3-byte addressing)				
P4E	Parameter 4 kB Sector Erase	-	20h	20h
P8E	8 kB (two 4 kB) Parameter Sector Erase	-	40h	-
SE	64 kB or 256 kB Sector Erase	20h / D8h	D8h	D8h
BE	Bulk Erase	C7h / 60h	C7h / 60h	C7h / 60h
ERSP	Erase Suspend	-	-	75h

Table 2. Commands (Sheet 2 of 2)

Command	Description	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S S70FL01GS
		Instruction Codes		
ERRS	Erase Resume	-	-	7Ah
Erase Operations (4-byte addressing)				
P4E4	Parameter 4 kB Sector Erase	-	-	21h
SE4	64 kB or 256 kB Sector Erase	-	-	DCh
Power Saving Mode				
DP	Deep Power Down	B9h	B9h	-
RES	Release from Deep Power-Down and Read Electronic Signature			
ABh	ABh	-		
OTP Operations				
OTPP	Program OTP memory space	-	42h	42h
OTPR	Read data in the OTP memory space	-	4Bh	4Bh
Register Operations				
RDSR	Read Status Register	05h	05h	05h
RDSR2	Read Status Register-2	-	-	07h
RCR	Read Configuration Register	-	35h	35h
WRR	Write (Status and Configuration) Register	01h	01h	01h
CLSR	Clear Status Register - Erase/Program Fail reset	-	30h	30h
ABRD	AutoBoot Register Read	-	-	14h
ABWR	AutoBoot Register Write	-	-	15h
BRRD	Bank Register Read	-	-	16h
BRWR	Bank Register Write	-	-	17h
BRAC	Bank Register Access	-	-	B9h
ASPRD	ASP Read	-	-	2Bh
ASPP	ASP Program	-	-	2Fh
DLPRD	Read Data Learning Pattern	-	-	41h
PNVDLR	Program NV Data Learning Register	-	-	43h
WVDLR	Write Volatile Data Learning Register	-	-	4Ah
PLBWR	PPB Lock Bit Write	-	-	A6h
PLBRD	PPB Lock Bit Read	-	-	A7h
DYBRD	DYB Read	-	-	E0h
DYBWR	DYB Write	-	-	E1h
PPBRD	PPB Read	-	-	E2h
PPBWR	PPB Program	-	-	E3h
PPBE	PPB Erase	-	-	E4h
WDBRD	WDB Read	-	-	E5h
WDBP	WDB Program	-	-	E6h
PASSRD	Password Read	-	-	E7h
PASSP	Password Program	-	-	E8h
PASSU	Password Unlock	-	-	E9h
Reset Operations				
RESET	Software Reset	-	-	F0h
MBR	Mode Bit Reset	-	-	FFh

The primary areas of concern for migrations from FL-P to FL-S are device identification, extended addressing, feature reduction, DC and AC specification differences and package and pin out differences.

Migration to the S25FL128S from any monolithic S25FL-P device is straightforward as the superset features incorporated into the S25FL-S family do not conflict with the legacy feature set. The S25FL128S utilizes the same device identification methodology, commands, timing, and packaging employed by the S25FL-P family.

Migration to the S25FL256S from the S70FL256P is not as straightforward because the S25FL256S has a single chip select input and requires different addressing methodology to access its full 32 MB array, compared to the pair of lower density S25FL129P devices within the S70FL256P DDP.

2.1 Device Identification

The S25FL-S family supports standard READ-ID (90h), RDID (9Fh), and RES (ABh) device identification command methods, as shown in Table 3 through Table 5, respectively. The S25FL-S uses the same identification data convention as employed in S25FL-P, for example, the S25FL128S provides the same returned values as the S25FL129P. The system can be made aware of additional features in the S25FL-S devices by accessing the CFI address space.

2.1.1 READ-ID (90h)

The READ-ID Byte 1 return value for dual die packaged devices is the same value as each die in the package, for example, READ-ID Byte 1 for 32 MB S70FL256P is 17h, the same value as for the 16 MB S25FL129P. Applications can access CFI register address 27h to determine the total density of a device. The returned value at CFI address 27h will be N (hex) where Device Size = 2^N Bytes, for example, for the 32 MB S70FL256P and S25FL256S, a read to CFI address 27h will return the value 19h, which is 25 (base10) and device size (bytes) = 2^{25} = 33,554,432 = 32 MB.

Table 3. Product Identification – READ-ID

Device	Primary Erase Block Size	READ-ID Byte 0 Manufacturer Information	READ-ID Byte 1 Device Information
S25FL032P	64 kB	01h	15h
S25FL064P	64 kB	01h	16h
S25FL128P	64 kB	01h	17h
S25FL128P	256 kB	01h	17h
S25FL129P	64 kB	01h	17h
S25FL129P	256 kB	01h	17h
S70FL256P	64 kB	01h	17h
S70FL256P	256 kB	01h	17h
S25FL128S	64 kB	01h	17h
S25FL128S	256 kB	01h	17h
S25FL256S	64 kB	01h	18h
S25FL256S	256 kB	01h	18h
S25FL512S	256 kB	01h	19h
S70FL01GS	256 kB	01h	19h

2.1.2 RDID (9Fh)

Use of the RDID (9Fh) command method for device identification is the preferred method and it is consistently implemented in the FL-P and FL-S families as illustrated in Table 4. The flash will sequentially output Common Flash Interface register values starting on the 128th clock after the RDID command is provided. Specific CFI register values are documented in each device data sheet.

Table 4. Product Identification - RDID

Device	Primary Erase Block Size	RDID Byte 0 Mfg ID	RDID Byte 1 Device ID	RDID Byte 2 Device ID	RDID Byte 3 Extended Bytes	RDID Byte 4 Extended Bytes	RDID Byte 5 Reserved	RDID Byte 6 Reserved
S25FL032P	64 kB	01h	02h	15h	4Dh	XXh	XXh	XXh
S25FL064P	64 kB	01h	02h	16h	4Dh	XXh	XXh	XXh
S25FL128P	64 kB	01h	20h	18h	03h	01h	XXh	XXh
S25FL128P	256 kB	01h	20h	18h	03h	00h	XXh	XXh
S25FL129P	64 kB	01h	20h	18h	4Dh	01h	XXh	XXh
S25FL129P	256 kB	01h	20h	18h	4Dh	00h	XXh	XXh
S70FL256P	64 kB	01h	20h	18h	4Dh	01h	XXh	XXh
S70FL256P	256 kB	01h	20h	18h	4Dh	00h	XXh	XXh
S25FL128S	64 kB	01h	20h	18h	4Dh	01h	03h	00h
S25FL128S	256 kB	01h	20h	18h	4Dh	00h	03h	00h
S25FL256S	64 kB	01h	02h	19h	4Dh	01h	00h	00h
S25FL256S	256 kB	01h	02h	19h	4Dh	00h	00h	00h
S25FL512S	256 kB	01h	02h	20h	4Dh	00h	00h	00h
S70FL01GS	256 kB	01h	02h	21h	4Dh	00h	00h	00h

Note:
XXh = undefined

2.1.3 RES (ABh)

The Read Electronic Signature (RES) (ABh) command returned value for the monolithic S25FL256S is 18h and for the dual die packaged 32 MB S70FL256P is 17h, the same return value as from each of its two 16 MB S25FL129P die, reference Table 5. System software may require modification to accommodate this difference. As stated above, applications can access CFI register address 27h to determine the total density of a device. The CFI device density showing twice the density as that of the device ID indicates a DDP.

Table 5. Product Identification - RES

Device	RES Electronic Signature
S25FL032P	15h
S25FL064P	16h
S25FL128P	17h
S25FL129P	17h
S70FL256P	17h
S25FL128S	17h
S25FL256S	18h
S25FL512S	19h
S70FL01GS	20h

2.2 Extended Addressing

The S25FL-P and S70FL256P utilize a 3-byte (byte boundary 24 bits) address within commands to individually access all bytes in each die (up to 16 MB per die). To accommodate addressing above 16 MB, the FL-S family members support a new Bank Address Register and three addressing options listed below. Table 6 provides a description of the new Bank Address Register.

Table 6Bank Address Register

Bit	Field Name	Function	Type	Default Value	Description
7	EXTADD	Extended Address Enable	Volatile	0b	1 = 4-byte addressing required with legacy command 0 = 3-byte addressing with legacy command + Bank Address
6 to 2	RFU	Reserved	Volatile	0000b	Reserved for Future Use
1	BA25	Bank Address	Volatile	0b	A25 for 512 Mb device, RFU for lower density devices
0	BA24	Bank Address	Volatile	0b	A24 for 256 Mb device, RFU for lower density devices

2.2.1 Extended Addressing – Legacy Instructions with Bank Address Register

Use legacy instructions with 3-byte addresses along with the Bank Address Register (BAR). The volatile Bank Address register is used to provide the 4th byte of the address to allow switching between 16 MB banks of the flash array. Specifically, BAR[0] equates to address bit A24 and BAR[1] equates to address bit A25. The 3-byte address selects an address within the Bank selected by BAR[1:0] for read, erase, and program commands. BAR[7] cleared to zero selects the 3 byte + bank address extended addressing method. At power up and hardware reset, the default is BAR cleared to zero, selecting this addressing method and Bank 0, which limits initial access to the lowest 16 MB of the flash array. For Read operations, the device will continuously transfer out data until the end of the array starting from the address provided in the read command, regardless of which bank it is in. The BAR[1:0] value is only used for the starting address of the read operation and is not updated during a streaming read operation. Table 7 lists the Bank Address Registers settings applicable to the monolithic S25FL-S devices.

Table 7. Bank Address Registers Settings for S25FL-S

Address (minimum)	Address (maximum)	16 MB Bank	BAR[1]	BAR[0]
0x00000000	0x00FFFFFF	0	0	0
0x01000000	0x01FFFFFF	1	0	1
0x02000000	0x02FFFFFF	2	1	0
0x03000000	0x03FFFFFF	3	1	1

2.2.2 Extended Addressing – Legacy Instructions with 4-Byte Addressing

Use legacy instructions with 4-byte addresses. Table 8 lists the command instructions that will require 4-byte addresses when BAR[7] = 1 in the FL-S family.

Table 8. Commands Requiring 4-Byte Addressing When BAR[7] = 1

Command	Command Description	Instruction Code
PP	Program Page	02h
RD	Read Normal	03h
FSTRD	Read Fast	0Bh
QPP	Program Quad Page	32h
RDDO	Read Dual Out	3Bh
RDQO	Read Quad Out	6Bh
RDDIO	Read Dual I/O	BBh
SE	Erase 64/256 kB	D8h
RDQIO	Read Quad I/O	EBh
P4E	Parameter 4 kB Erase	20h

The legacy 3-byte standard instructions can be used in conjunction with the EXTADD Bit in the Bank Address Register (BAR[7]). By default BAR[7] is cleared to 0 following power up and hardware reset to enable standard 3-byte addressing to the lowest 16 MB of the flash array. When BAR[7] is set to 1, the legacy commands require 4-byte addresses.

2.2.3 Extended Addressing – New Instructions with 4-Byte Addressing

Use of new command instructions which require 4-byte (32-bit) addresses. Table 9 lists the 4-byte command instructions supported by the FL-S family.

Table 9. Commands Requiring 4-byte Addressing

Command	Command Description	Instruction Code
FSTRD4	Read Fast (4 Byte Address)	0Ch
PP4	Program Page (4 Byte Address)	12h
RD4	Read Normal (4 Byte Address)	13h
QPP4	Program Quad Page (4 Byte Address)	34h
RDDO4	Read Dual Out (4 Byte Address)	3Ch
RDQO4	Read Quad Out (4 Byte Address)	6Ch
RDDIO4	Read Dual I/O (4 Byte Address)	BCh
SE4	Erase 64/256 kB (4 Byte Address)	DCh
RDQIO4	Read Quad I/O (4 Byte Address)	ECh
P4E4	Parameter 4 kB Erase (4 Byte Address)	21h

2.2.4 New Commands to Support Bank Address Register

The FL-S family supports three new commands for accessing and modifying the Bank Address Register: Bank Register Read (BRRD), Bank Register Write (BRWR), and Bank Register Access (BRAC).

2.2.4.1 Bank Register Read (BRRD)

The BRRD command (opcode 16h) is used to read the current Bank Address Register contents. The BRRD command consists of CS# assertion, followed by input of the single opcode byte 16h, followed by the output of the single data byte BAR[7:0]. The BAR[7:0] will be output repetitively if CS# and SCK remain active. The command is terminated with CS# negation.

2.2.4.2 Bank Register Write (BRWR)

The BRWR command (opcode 17h) is used to write address bits above A23 into the Bank Address Register (BAR[1:0]). The command is also used to write the Extended address control (EXTADD) bit in the Bank Address Register (BAR[7]). This command does not require use of a preceding WREN command. The BRWR command consists of CS# assertion, followed by input of the single opcode byte 17h, followed by input of the single data byte BAR[7:0], followed by CS# negation.

2.2.4.3 Bank Register Access (BRAC)

The BRAC command (opcode B9h) provides an alternative method to modify the BAR to enable accesses to higher 16 MB array banks while using legacy 3-byte addressing. This method is necessary in systems that cannot support the new BRRD and BRWR commands due to SPI memory controllers with fixed instruction code libraries. The BRAC command uses the same opcode and format as the legacy Deep Power Down (DPD) command that is generally available in legacy SPI memory controllers. The FL-S family does not support Deep Power Down mode. The BRAC command consists of CS# assertion, followed by input of the single opcode byte B9h, followed by CS# negation. When a BRAC command is immediately followed by a Write Register (WRR) command (opcode 01h), the host provided data is used to update BAR[1:0]. The upper bits of the first data byte and the optional second data byte of the WRR command are ignored. The flash returns to the standby state following the BRAC + WRR command sequence. The combined BRAC followed by WRR command sequence has no effect on the value of EXTADD (BAR[7]). Any command other than WRR, or any other sequence where CS# goes low and returns high following a BRAC command will close access to BAR and return the interface to the standby state. A WREN command is not needed or allowed between the BRAC and WRR commands. This BRAC + WRR command sequence is only allowed during standby, program suspend or erase suspend states.

2.3 Feature Reduction

The FL-P family supported a few features that are not supported in the FL-S family flash. Specifically, the FL-S family does not support Deep Power Down mode, high voltage accelerated programming, or parallel programming (a feature unique to S25FL128P in SO-16 package). Deep Power Down is not required in many applications and the much faster program operations of the FL-S Eclipse architecture provides better performance than the FL-P accelerated or parallel programming methods. In general, there should be no in-system impact due to the lack of these features on FL-S.

2.3.1 Deep Power Down Mode

The FL-S flash will ignore the Deep Power Down (DPD) command (opcode B9h) unless it is immediately followed by a WRR command (opcode 01h) to allow programming of BAR[1:0]), as discussed in Section 2.2.4.3. Since this is not an expected command sequence for FL-P flash, there should be no impact on operation as the flash will remain in standby mode consuming minimal power.

Because FL-S does not transition into Deep Power Down mode, the Release from Deep Power Down command (RES: ABh) has a truncated function in the FL-S and is called the Read Electronic Signature (RES) command in FL-S documentation. On FL-S flash, issuing the RES command will leave the device in Standby mode and will output the Electronic Signature byte on the 5th byte cycle of the command sequence to allow backward compatibility with FL-P flash.

2.3.2 High Voltage Accelerated Programming

The FL-P flash supported application of V_{HH} (nominally 9V) on the W#/ACC input to accelerate programming, a feature often utilized on gang programmers but not in-system. The FL-S family does not support high voltage accelerated programming and does not support application of V_{HH} onto the W# input. The FL-S flash programming throughput is much higher than FL-P flash so there is no negative impact due to this feature omission unless V_{HH} application is implemented in-system to accelerate programming of FL-P flash.

2.3.3 Parallel Programming

The FL-S family does not support byte wide accelerated programming as uniquely implemented on the S25FL128P in SO-16 package, a feature often occasionally utilized on gang programmers but not in-system. The FL-S flash programming throughput is much higher than FL-P flash so there is no negative performance or cost impact due to this feature omission. See Section 2.5 on page 12 for a discussion on pin out difference accommodation.

2.4 DC and AC Parameter

Table 10 and Table 11 provide comparisons of DC and AC parameters for FL-P and like density FL-S devices. While most parameter differences should not cause performance issues when migrating from a FL-P flash to a FL-S flash, it is highly recommended that the user carefully review all parameter differences for potential impact.

Table 12 provides a comparison of program and erase performance parameters for FL-P and like density FL-S devices. FL-S flash deliver substantially higher programming performance as well as main block and bulk erase performance. It is recommended that programming operations on FL-S flash be performed on a minimum block size and alignment of 16 bytes to maximize data integrity. Up to sixteen 16 byte aligned blocks can be programmed per 256 byte page programming operation. Up to thirty two 16 byte aligned blocks can be programmed per 512 byte page programming operation.

Table 10. DC Parameter Comparison (Sheet 1 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P	S70FL256P	S25FL128S S25FL256S S25FL512S
V_{CC}: Core Source Voltage	Min/ Max	V	2.7 / 3.6	2.7 / 3.6	2.7 / 3.6	2.7 / 3.6
V_{CC}-cutoff: V_{CC} below which re-initialization required	Min	V	2.4	2.4	2.4	2.4
V_{CC}-low: V_{CC} below which re-initialization can occur	Min	V	2.3	2.3	2.3	2.3
Voltage with respect to V_{SS} on W#(/ACC)/IO2	Min/ Max	V	-0.5 / 9.5	-0.5 / 9.5	-0.5 / 9.5	-1.0 / V_{CC}+1.0
Voltage with respect to V_{SS} on RESET#, SCK, CS#, CS2#	Min/ Max	V	-0.5 / V_{CC} + 0.5	-0.5 / V_{CC} + 0.5	-0.5 / V_{CC} + 0.5	-1.0 / 9.5

Table 10. DC Parameter Comparison (Sheet 2 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P	S70FL256P	S25FL128S S25FL256S S25FL512S
Voltage with respect to V_{SS} on SI/IO0, SO/IO1, HOLD#/IO3	Min/ Max	V	-0.5 / V_{CC} + 0.5	-0.5 / V_{CC} + 0.5	-0.5 / V_{CC} + 0.5	-1.0 / V_{CC} + 1.0
V_{HH}: ACC Accelerated Programming Voltage	Min/ Max	V	8.5 / 9.5	8.5 / 9.5	8.5 / 9.5	n/a
V_{IL}: Input Low Voltage	Min/ Max	V	-0.3 / 0.3 x V_{CC}	-0.3 / 0.3 x V_{CC}	-0.3 / 0.3 x V_{CC}	-0.5 / 0.2 x V_{IO}
V_{IH}: Input High Voltage	Min/ Max	V	0.7 x V_{IO} / V_{CC} + 0.5	0.7 x V_{IO} / V_{CC} + 0.5	0.7 x V_{IO} / V_{CC} + 0.5	0.7 x V_{IO} / V_{IO} + 0.4
V_{OL}: Output Low Voltage (I_{oh} = 1.6mA, V_{CC} = 2.7V)	Max	V	0.4	0.4	0.4	0.15xV_{IO}
V_{OL}: Output High Voltage (I_{oh} = -0.1mA)	Min	V	V_{CC} -0.6	V_{CC} -0.6	V_{CC} -0.6	0.85 x V_{IO}
I_{LI}: Input Leakage Current (V_{CC} = 3.6V, V_{IN} = V_{IL}/V_{IH})	Max	µA	±2	±2	±4	±2
I_{LO}: Output Leakage Current (V_{CC} = 3.6V, V_{IN} = V_{IL}/V_{IH})	Max	µA	±2	±2	±4	±2
I_{CC}: Active Read Current (SDR-SIO, FSCK = 40/50 MHz)	Max	mA	10	12	12	14
I_{CC}: Active Read Current (SDR-SIO, FSCK = max)	Max	mA	22	25	25	25
I_{CC}: Active Read Current (SDR-QIO, FSCK = 80 MHz)	Max	mA	n/a	38	38	50
I_{CC}: Active Page Program (PP) Current (CS# = V_{IL})	Max	mA	26	26	26	100
I_{CC}: Active WR Program (WRR) Current (CS# = V_{IL})	Max	mA	26	15	15	100
I_{CC}: Active Block Erase (SE) Current (CS# = V_{IL})	Max	mA	26	26	26	100
I_{CC}: Active Bulk Erase (BE) Current (CS# = V_{IL})	Max	mA	26	26	26	100
I_{SB}: Standby Current (CS# = V_{IO}, SI/RESET/SCK = V_{IO}/ GND)	Typ/ Max	µA	80 / 200	80 / 200	160 / 400	70 / 100
I_{PD}: Deep Power Down Current (CS# = V_{CC}, SO + V_{IN} = V_{CC},GND)	Max	µA	20	10	20	n/a

Note:
n/a = Not Applicable

Table 11. AC Parameter Comparison (Sheet 1 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S
FSCK,R: SCK Frequency - READ	Max	MHz	40	40	50
FSCK,R: SCK Frequency - RDID	Max	MHz	40	50	133
FSCK,C: SCK Frequency - QPP (SIO)	Max	MHz	n/a	104	80
FSCK,C: SCK Frequency - QPP (DIO,QIO)	Max	MHz	n/a	80	80
FSCK,C: SCK Frequency - Other Commands (SIO)	Max	MHz	104	104	133
FSCK,C: SCK Frequency - Other Commands (DIO,QIO)	Max	MHz	n/a	80	104
t_{PU}: Required Delay from V_{CC}>V_{CC}-min to CS# low	Max	µs	300	300	300
t_{PD}: V_{CC}-low time to re-initialize (V_{CC}<V_{CC}-low)	Min	µs	1	1	1
t_{WH}, t_{CH}, t_{WL}, t_{CL}: Clock High/Low Time	Min	ns	4.5	4.5	3.6

Table 11. AC Parameter Comparison (Sheet 2 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S
t_{CRT}, t_{CLCH}: SCK Rise Slew Rate	Min	V/ns	0.1	0.1	0.1
t_{CFT}, t_{CHCL}: SCK Fall Slew Rate	Min	V/ns	0.1	0.1	0.1
t_{CS}: CS# High Time (Read Instructions)	Min	ns	50	10	10
t_{CS}: CS# High Time (Program/Erase Instructions)	Min	ns	50	50	50
t_{CSS}: CS# Setup to SCK	Min	ns	3	3	3
t_{CSH}: CS# Hold from SCK	Min	ns	3	3	3
t_{SU-DAT}: Data input Setup to SCK	Min	ns	3	3	3
t_{HD-DAT}: Data input Hold from SCK	Min	ns	2	2	2
t_{HD}, t_{CD}: HOLD# Setup to SCK	Min	ns	3	3	3
t_{HC}, t_{CH}: HOLD# Hold Time from SCK	Min	ns	3	3	3
t_V: SCK low to Output Valid (V_{CC} = V_{IO})	Min	ns	0	0	0
t_{HO}: Output Hold Time	Min	ns	0	0	0
t_{LZ}, t_{HZ}: HOLD# to Output Low/High-Z	Min	ns	8	8	8
t_{DIS}: Output Disable Time	Max	ns	8	8	8
t_{WPS}: WP# Setup Time	Min	ns	20	20	20
t_{WPH}: WP# Hold Time	Min	ns	100	100	100
t_W: WRR Write Time	Max	ms	100	50	100
t_{DP}: CS# High to Deep Power Down Mode	Max	µs	3	10	n/a
t_{RES}: Release from DP Mode	Max	µs	30	30	n/a
t_{PSL}, t_{ESL}: Program/Erase Suspend Latency	Max	µs	n/a	n/a	20
t_{PRS},t_{ERS}: Program/Erase Resume Latency	Min	µs	n/a	n/a	100
t_{RPH}: RESET# Low to CS# Low	Min	µs	n/a	n/a	35
t_{RP}: RESET pulse width	Min	ns	n/a	n/a	200
t_{RH}: RESET# High to CS# Low	Min	ns	n/a	n/a	200

Note:
n/a = Not Applicable

Table 12. Program and Erase AC Parameter Comparison (Sheet 1 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S
t_{PP}: 256B Page Programming Time	Typ/ Max	ms	1.2 / 3.0	1.2 / 3.0	0.25 / 0.55
t_{PP}: 512B Page Programming Time	Typ/ Max	ms	n/a	n/a	0.34 / 0.75
t_{PP-ACC}: Accelerated 256B Page Program Time	Typ/ Max	ms	1.0 / 2.4	1.2 / 2.4	n/a
t_{PE}: 4 kB Parameter Block erase Time	Typ/ Max	s	n/a	0.2 / 0.8	0.13 / 0.65
t_{SE}: 64 kB Main Block Erase Time	Typ/ Max	s	0.5 / 3	0.5 / 2.0	0.13 / 0.65
t_{SE}: 64 kB Low/High Parameter Block Erase Time	Typ/ Max	s	0.5 / 3	0.5 / 2.0	2.1 / 10.4
t_{SE}: 256 kB Main Block Erase Time	Typ/ Max	s	2.0 / 12	2.0 / 8.0	0.52 / 2.6

Table 12. Program and Erase AC Parameter Comparison (Sheet 2 of 2)

Feature / Parameter	Type	Units	S25FL128P	S25FL032P S25FL064P S25FL129P S70FL256P	S25FL128S S25FL256S S25FL512S
t_{BE}: 128 Mbit Density Bulk Erase	Typ/ Max	s	128 / 768	128 / 256	33 / 165
t_{BE}: 256 Mbit Density Bulk Erase Time	Typ/ Max	s	n/a	256 / 512	66 / 330

Note:
n/a = Not Applicable

2.5 Packaging and Pin Out

The S25FL128S and S25FL256S will be available in SO-16, WSON 8 and BGA-24 packaging with pin outs compatible with S25FL-P flash. The S25FL256S has only one chip select and is pin out compatible with the S70FL256P in so far as the unused CS2# input location is not connected internally so any electrical activity on this input will be ignored.

The S25FL128P SO-16 package option supported a byte wide parallel I/O option via pins 4, 5, 6, 8, 11, 12, 13, 14 to allow program acceleration on programming equipment. This function is not supported on other FL-P models or any FL-S model. This functionality is not utilized in-system so the non-multiplexed parallel I/O pins 4, 5, 6, 11, 12, 13, 14 should be electrically isolated, making the S25FL128P SO-16 in-system connections compatible with other S25FL-P and S25FL-S SO-16 implementations for single IO transactions.

The FL-S family has two superset hardware features that are enabled via external inputs, Hardware Reset, enabled by a dedicated RESET# input, and Versatile IO, enabled through a dedicated VIO power supply input. These features are only available on select versions of SO-16 and BGA packaged FL-S devices. Refer to specific device data sheets for appropriate ordering part numbers to select models with and without these functions enabled.

Devices with the RESET# input option have an internal pull-up on this input so it can be left unconnected if the function is not desired. Devices that do not have the RESET# input option have this pin electrically isolated and have the RESET# circuit input is internally pulled > V_{IH}.

Devices with the V_{IO} input option must have a power supply level between 1.65V and V_{CC} applied. During power up, V_{IO} must not exceed V_{CC} and should not lag V_{CC} by more than 200 mV until it reaches 1.65V. Devices that do not have a V_{IO} input option have this pin electrically isolated and have the I/O ring supply input tied to V_{CC} internally.

Certain package pins may be connected to the die for access to internal signals and should not be driven by the host or tied to either V_{CC} or V_{SS} externally. On all SO-16 packages, pins 11, 12, and 13 should be electrically isolated. On all FAB024 and FAC024 packages, balls B1, C1, and D1 should be electrically isolated. This is consistent across all FL-P and FL-S flash; however, the nomenclature used in FL-P data sheets differ in that these unused I/O are labeled either NC (No Connect) or DNC (Do Not Connect).

2.6 Block Protection

The S25FL-S flash supports the same block protection scheme implemented in the S25FL-P flash which utilizes TBPROT and BP[2:0] Status Register bits to define which integer fraction of the array is protected. In the S70FL256P flash, Block Protection must be set individually for each 16 MB array accessed independently via CS# and CS2#. In the S25FL256S, the BP[2:0] bits act on its entire 32 MB array. When migrating from the S70FL256P to the S25FL256P, this difference has to be accommodated if the Block Protection feature is utilized. Table 13 illustrates BP[2:0] settings to achieve equivalent Block Protection in S70FL256P and S25FL256S.

Table 13. 256 Mbit Block Protection (Sheet 1 of 2)

Fractional Protection Area of 32 MB Array	Memory Protection Size	S70FL256P CS#		S70FL256P CS2#		S25FL256S	
		TBPROT	BP[2:0]	TBPROT	BP[2:0]	TBPROT	BP[2:0]
None	0 kB	0 or 1	000b	0	000b	0	000b
Upper 64th	512 kB	0 or 1	000b	0	010b	0	001b
Upper 32nd	1024 kB	0 or 1	000b	0	011b	0	010b

Table 13. 256 Mbit Block Protection (Sheet 2 of 2)

Fractional Protection Area of 32 MB Array	Memory Protection Size	S70FL256P CS#		S70FL256P CS2#		S25FL256S	
		TBPROT	BP[2:0]	TBPROT	BP[2:0]	TBPROT	BP[2:0]
Upper 16th	2048 kB	0 or 1	000b	0	100b	0	011b
Upper 8th	4096 kB	0 or 1	000b	0	101b	0	100b
Upper 4th	8192 kB	0 or 1	000b	0	110b	0	101b
Upper Half	16384 kB	0 or 1	000b	0	111b	0	110b
All Blocks	32768 kB	0 or 1	1111b	0	111b	0	111b
None	0 kB	1	000b	0 or 1	000b	1	000b
Lower 64th	512 kB	1	010b	0 or 1	000b	1	001b
Lower 32nd	1024 kB	1	011b	0 or 1	000b	1	010b
Lower 16th	2048 kB	1	100b	0 or 1	000b	1	011b
Lower 8th	4096 kB	1	101b	0 or 1	000b	1	100b
Lower 4th	8192 kB	1	110b	0 or 1	000b	1	101b
Lower Half	16384 kB	1	111b	0 or 1	000b	1	110b
All Blocks	32768 kB	1	111b	0 or 1	1111b	1	111b

2.7 Additional Feature Differences

The FL-S flash supports several additional features whose use is optional and which legacy system software does not need to accommodate. These include:

Advanced Sector Protection — In addition to the legacy fractional block protection scheme, FL-S supports a robust read and write protection scheme that allows for both dynamic and persistent protection of individual sectors, with or without password protection. A host of new commands and several new registers were added to support this new security feature. Details can be found in the FL-S data sheets.

Autoboot — New feature that allows post power up reads to initiate at a specific address without any preamble read command. The AutoBoot Register and the AutoBoot Register Read (ABRD: 14h) and AutoBoot Register Write (ABWR: 15h) commands were added to enable this feature.

Erase and Program Operation Suspend and Resume — New Erase Suspend (ERSP: 75h), Erase Resume (ERRS: 7Ah), Program Suspend (PGSP: 85h), and Program Resume (PGRS: 8Ah) commands allow erase and program operations to be individually suspended and resumed to all access to data in blocks of the flash which are not actively being modified. Status Register 2 has been added to allow software to determine if a particular block is in suspension, as well as a new Read Status Register-2 command (RDSR2: 07h) to access this new register.

Software Reset — New Software Reset command (RESET: F0h) restores the device to its initial power up state, except for the volatile FREEZE bit in the Configuration Register and the volatile PPB Lock bit in the PPB Lock Register.

3 Conclusion

Migration from monolithic S25FL-P devices to S25FL128S is straightforward and requires minimal accommodation in regards to either system software or hardware. Migration from monolithic or dual die stacked FL-P devices to S25FL256S, S25FL512S, or S70FL01GS will require some modification of legacy system software and possibly system hardware to accommodate. Once accommodations are made, if required, FL-S flash will enable growth to higher density, faster read access, with superior program and erase performance, in existing systems.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	12/16/2010	Initial version
*A	-	-	02/10/2012	Corrected High Level Feature Comparison table Updated Product Identification - READ-ID table Corrected Bank Address Register table Corrected Bank Address Registers Settings for S25FL-S table
*B	4928211	MSWI	09/21/2015	Updated in Cypress template
*C	5822805	AESATMP8	07/18/2017	Updated logo and Copyright.

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