THIS SPEC IS OBSOLETE

Spec No: 001-98540

Spec Title: AN98540 - CONNECTING CYPRESS SPI FLASH TO CONFIGURE ALTERA FPGAS

Replaced by: 001-98558

AN98540

Connecting Cypress SPI Flash to Configure Altera FPGAs

Author: Cypress

AN98540 describes how to connect Cypress SPI Flash with Altera FPGAs as their configuration device. The Altera FPGAs that are in scope are: Altera Cyclone, Cyclone II, Cyclone III, Cyclone IV, Cyclone IV GX, Stratix II, Stratix II GX, Stratix III, Stratix IV and Arria GX.

Contents

1 Introduction

Altera® FPGAs are programmable logic devices used for basic logic functions, chip-to-chip connectivity, signal processing, and embedded processing. These devices are programmed and configured using an array of SRAM cells that need to be re-programmed on every power-up. Several different methods of configuring FPGAs are normally used. They include programming by a microprocessor, JTAG port, or directly by a serial PROM or flash. Cypress® SPI (Serial Peripheral Interface) flash can be easily connected to Altera FPGAs in order to configure the FPGA at power-up. The Active Serial SPI configuration mode is supported for Altera Cyclone® IV, Cyclone® III, Cyclone® II, Cyclone®, Stratix® IV Stratix® III, Stratix® II, Stratix® II GX, Arria® II GX, and Arria® GX families.

A workaround for Active Serial Mode Programming of Cypress SPI Flash with Altera Quartus® II V10.1 or higher is detailed in Section 2.2, *Active Serial Mode Programming of Cypress SPI Flash with Altera Quartus® II V10.1* on page 2.

2 Configuration Considerations and Methods

Configuration considerations related to connecting SPI flash to an Altera FPGA that are addressed in this section. The details of the Altera FPGA configuration cycle are presented, and various methods or design options for programming Cypress SPI flash are discussed.

2.1 Configuration Cycle

The three stages of the configuration cycle are power-on reset, configuration, and initialization. The FPGA's power-on reset (POR) circuit keeps the device FPGA in a reset state until all applied voltages reach stable levels on power-up. As soon as the FPGA enters POR, it drives the nSTATUS signal low to indicate it is busy, drives the CONF_DONE signal low to indicate that its configuration has not been completed, and tri-states all user I/O pins. After POR, the FPGA releases nSTATUS and enters configuration mode when this signal is pulled high by the external pull-up resistor connected to nSTATUS.

The serial clock (DCLK) generated by the FPGA device controls the configuration data transfer from SPI flash to the FPGA. After all configuration data is transferred to the FPGA, it releases the CONF_DONE pin, which is pulled high by an external pull-up resistor. FPGA initialization begins after CONF_DONE goes to a logic high-level. After internal initialization, the FPGA enters user mode.

2.2 Active Serial Mode Programming of Cypress SPI Flash with Altera Quartus® II V10.1

Here are the Altera Quartus II V10.1 (or higher) instructions for programming the Cypress SPI flash shown in Table 1 using Active Serial Mode:

1. Open a Quartus II project.
2. Go to File > Convert Programming Files.
3. Make the following selections:
   a. Programming File Type = .pof
   b. Select Mode = Active Serial
   c. Configuration device = EPCS64 (example for S25FL064P, also see Table 1)
   d. Click Advanced… and check the “Disable EPCS ID Check”
   e. Click on SOF Data and add the .sof file (Image file)
   f. Click “Generate” > a *.pof file is created.
4. Go to the Programmer and Select the Active Serial Programming Mode and add the .pof file
5. Check Program/Config and Start

Note: Quartus II V12 and V13 don't allow the user to program pof file to Cypress SPI flash. These versions should not be used with Cypress SPI Flash as the FPGA configuration device.

2.3 Direct Programming SPI Flash

During production, the Cypress SPI flash is loaded with configuration data via a third-party programmer. After installation in the final product, the off-board programmed SPI flash configures the Altera FPGA at every power-up. However, if a change in configuration data is planned, the SPI flash requires reprogramming on-board. Figure 5 through Figure 7 show headers for direct SPI flash In-System Programming (ISP). ISP programmer selection dictates header configuration. In order to allow an external source to directly program the SPI flash through this header, the nCONFIG input signal must be held Low to force the FPGA I/O pins into a High-Z state during programming, thereby eliminating any interference from the FPGA I/O pins to the SPI flash reprogramming.

2.4 Programming Cypress SPI Flash via the Parallel Flash Loader Megafunction

As listed in the Altera Parallel Flash Loader (PFL) Megafunction User Guide (ver 1.1, Feb 2011), Cypress S25FL032P, S25FL064P, and S25FL129P SPI Multi I/O flash are supported by the PFL megafunction in Quad mode. The PFL megafunction is instantiated in the Quartus II software and can program the SPI flash through the JTAG interface and control configuration from the SPI flash to the Altera FPGA. Quartus II software versions 10.0 and later support Quad mode Cypress S25FL-P SPI flash in the PFL megafunction.

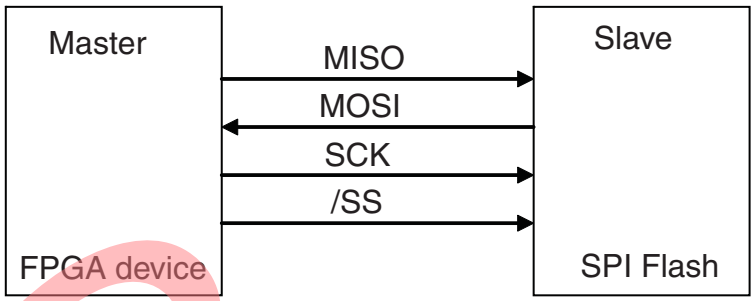
3 SPI Basics

Serial Peripheral Interface (SPI) is a simple 4-wire synchronous interface protocol which enables a master device and one or more slave devices to intercommunicate. The SPI bus consists of 4 signal wires:

- Master Out Slave In (MOSI) signal generated by the master (data to slave)
- Master In Slave Out (MISO) signal generated by the slave (data to master)
- Serial Clock (SCK) signal generated by the master to synchronize data transfers
- Slave Select (SS) signal generated by master to select individual slave devices — also known as Chip Select (CS) or Chip Enable (CE)

In this application note the FPGA is the master device and the SPI serial flash to configure the FPGA is the slave device; see Figure 1.

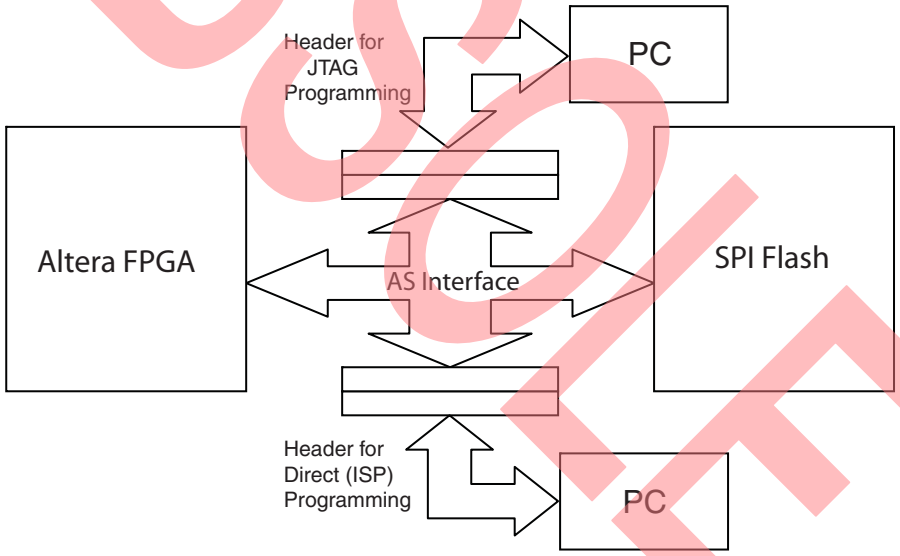
Figure 1. Direct Configuring FPGA Interface with SPI Flash



4 SPI Flash Connections to FPGAs

Figure 2 displays a simplified block diagram of the connection between SPI flash and Altera FPGA. It shows the SPI interface between Altera FPGA and SPI flash, as well as the headers for direct (in-system) and JTAG programming the SPI flash for configuration data updates from a PC or embedded host. Altera calls their SPI interface the Active Serial (AS) configuration interface.

Figure 2. Configuration Interface with Re-Programming Capability



The following is a detailed explanation of connections between Altera FPGA and Cypress SPI flash. The SPI flash connections to the Cyclone, Stratix, and Arria family FPGA devices with direct (ISP) programming only are shown in Figure 3 through Figure 6, while the connections for both direct and JTAG programming capability are shown in Figure 7 through Figure 10. Note that JTAG programming is not currently supported by Altera, but has been added as a future capability.

Signal connections to the 10-pin male headers for ISP and JTAG programming are provided in Table 12. Altera USB Blaster, MasterBlaster, ByteBlaster II, Ethernet Blaster, or MasterBlasterMV download cables are available to program the embedded Cypress SPI flash with configuration data updates, connected to either the ISP (AS mode) or JTAG headers.

Signal descriptions are listed in Table 13. The FPGA supplies the DCLK output from its internal oscillator to drive the clock input of SPI flash.

Logic levels and voltage connections for the Mode Select (MSEL) pins for each Altera FPGA family are listed in Table 14. The Mode Select pins have internal pull-down resistors that are always active.

Table 5 through Table 11 show the smallest SPI flash devices required for typical configuration bit requirements of different members of the Cyclone, Stratix, and Arria families.

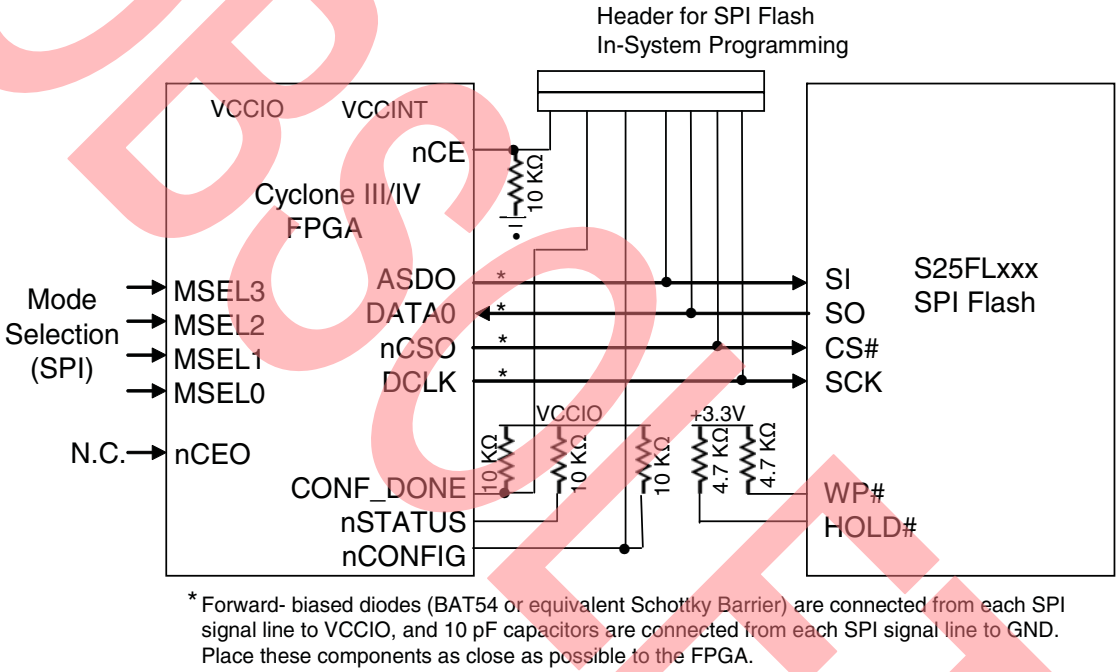
Table 1. Altera EPCS to Cypress SPI Compatible Device Mapping

Altera	Cypress Part Number
EPCS4	S25FL208K0RMFI04
EPCS16	S25FL116K0XMFI04
EPCS64	S25FL064P0XMFI00
EPCS128	S25FL128SAGMFI01

Notes:

1. *Devices are pin, package, feature, and command set compatible though Manufacturer and Device IDs are different.*
2. *Cypress offers additional package options for these Serial Flash devices.*

Figure 3. Cyclone III/IV FPGA Configuration from Cypress SPI Serial Flash Connection



* Forward- biased diodes (BAT54 or equivalent Schottky Barrier) are connected from each SPI signal line to VCCIO, and 10 pF capacitors are connected from each SPI signal line to GND. Place these components as close as possible to the FPGA.

Note: For Cyclone IV, connect a 25 Ohm the series resistor at the near end of the serial configuration device.

Table 2. SPI Flash Selection for Cyclone IV E Family FPGA Devices

FPGA	Number of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP4CE6	2,944,088	S25FL208K
EP4CE10	2,944,088	S25FL208K
EP4CE15	4,086,848	S25FL208K
EP4CE22	5,748,552	S25FL008K
EP4CE30	9,534,304	S25FL116K
EP4CE40	9,534,304	S25FL116K
EP4CE55	14,889,560	S25FL116K
EP4CE75	19,965,752	S25FL032P
EP4CE115	28,571,696	S25FL032P

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed data files.*

Table 3. SPI Flash Selection for Cyclone IV GX Family FPGA Devices

FPGA	Number of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP4CGX15	3,805,568	S25FL208K
EP4CGX22	7,600,040	S25FL208K
EP4CGX30	7,600,040	S25FL208K
	24,500,000	S25FL032P
EP4CGX50	24,500,000	S25FL032P
EP4CGX75	24,500,000	S25FL032P
EP4CGX110	39,425,016	S25FL064P
EP4CGX150	39,425,016	S25FL064P

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed data files.*

Figure 4. Stratix III/IV FPGA Configuration from Cypress SPI Serial Flash Connection

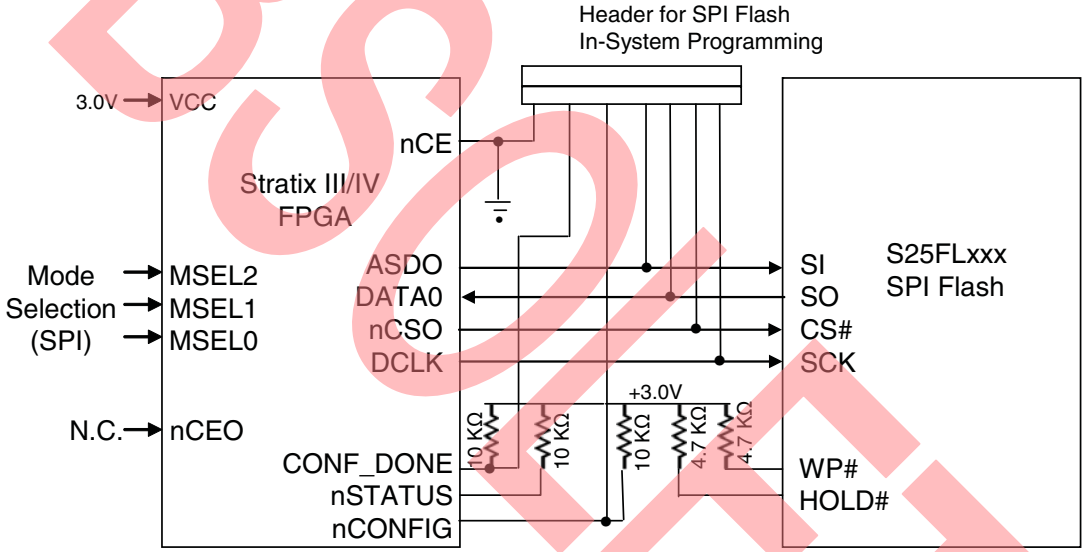


Table 4. SPI Flash Selection for Stratix IV Family FPGA Devices (Sheet 1 of 2)

FPGA	Number of Configuration Bits	Minimum SPI Flash Device (Cypress Part Number)
EP4SE230	94,557,465	S25FL128S
EP4SE360	128,395,577	S25FL128S
EP4SE530	171,722,057	S25FL128S (3)
EP4SE820	241,684,465	S25FL128S (3)
EP4SGX70	47,833,345	S25FL064P
EP4SGX110	47,833,345	FL064P
EP4SGX180	94,557,465	S25FL128S
EP4SGX230	94,557,465	S25FL128S
EP4SGX290	128,395,577	S25FL128S
	171,722,057	S25FL128S (3)
EP4SGX360	128,395,577	S25FL128S
	171,722,057	S25FL128S (3)

Table 4. SPI Flash Selection for Stratix IV Family FPGA Devices (Sheet 2 of 2)

FPGA	Number of Configuration Bits	Minimum SPI Flash Device (Cypress Part Number)
EP4SGX530	171,722,057	S25FL128S (3)
EP4S40G2	94,557,465	S25FL128S
EP4S40G5	171,722,057	S25FL128S (3)
EP4S100G2	94,557,465	S25FL128S
EP4S100G3	171,722,057	S25FL128S (3)
EP4S100G4	171,722,057	S25FL128S (3)
EP4S100G5	171,722,057	S25FL128S (3)

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed data files.*
3. *Compression required for bit stream configurations larger than 128 Mbits.*

Table 5. SPI Flash Selection for Stratix III Family FPGA Devices

FPGA	Number of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP3SL50	22,000,000	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP3SL70	22,000,000	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP3SL110	47,000,000	64 Mb (S25FL064P) / 32 Mb (S25FL032P)
EP3SL150	47,000,000	64 Mb (S25FL064P) / 32 Mb (S25FL032P)
EP3SL200	93,000,000	128 Mb (S25FL129P) / 64 Mb (S25FL064P)
EP3SE260	93,000,000	128 Mb (S25FL129P) / 64 Mb (S25FL064P)
EP3SL340	120,000,000	128 Mb (S25FL129P) / 128 Mb (S25FL129P)
EP3SE50	26,000,000	32 Mb (S25FL032P) / 32 Mb (S25FL032P)
EP3SE80	48,000,000	64 Mb (S25FL064P) / 32 Mb (S25FL032P)
EP3SE110	48,000,000	64 Mb (S25FL064P) / 32 Mb (S25FL032P)

Notes:

1. *Preliminary data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Table 6. SPI Flash Selection for Cyclone III Family FPGA Devices

FPGA	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP3C5	3,000,000	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP3C10	3,000,000	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP3C16	4,100,000	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP3C25	5,800,000	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP3C40	9,600,000	16 Mb (S25FL116K) / 8 Mb (S25FL208K)
EP3C55	14,900,000	16 Mb (S25FL116K) / 16 Mb (S25FL116K)
EP3C80	20,000,000	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP3C120	28,600,000	32 Mb (S25FL032P) / 32 Mb (S25FL032P)

Notes:

1. *Preliminary data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Figure 5. Cyclone/Cyclone II FPGA Configuration from Cypress SPI Serial Flash Connection

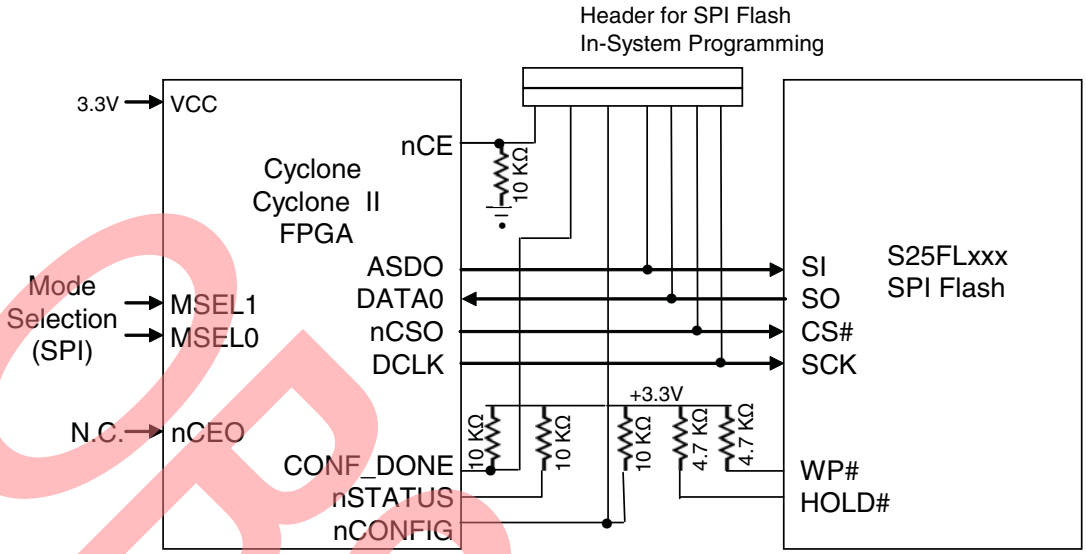


Table 7. SPI Flash Selection for Cyclone II Family FPGA Devices

FPGA	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP2C5	1,265,792	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2C8	1,983,536	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2C15	3,892,496	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2C20	3,892,496	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2C35	6,848,608	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2C50	9,951,104	16 Mb (S25FL116K) / 8 Mb (S25FL208K)
EP2C70	14,319,216	16 Mb (S25FL116K) / 16 Mb (S25FL116K)

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Table 8. SPI Flash Selection for Cyclone Family FPGA Devices

FPGA	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP1C3	627,376	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP1C4	924,512	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP1C6	1,167,216	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP1C12	2,323,240	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP1C20	3,559,608	8 Mb (S25FL208K) / 8 Mb (S25FL208K)

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Figure 6. Stratix II/Stratix II GX/Arria GX FPGA Configuration from Cypress SPI Serial Flash Connection

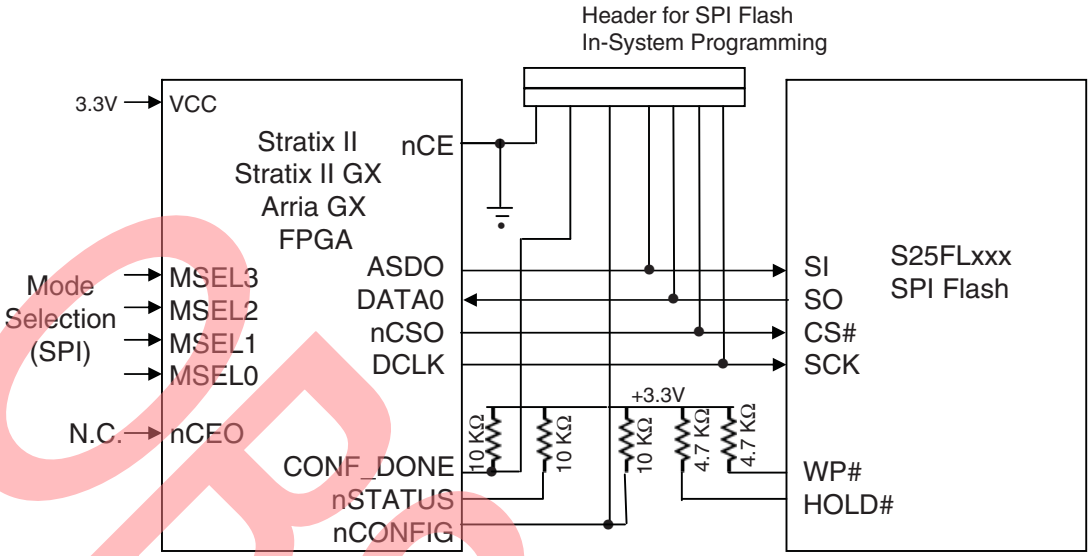


Table 9. SPI Flash Selection for Stratix II Family FPGA Devices

FPGA	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP2S15	4,721,544	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP2S30	9,640,672	16 Mb (S25FL116K) / 8 Mb (S25FL208K)
EP2S60	16,951,824	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP2S90	25,699,104	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP2S130	37,325,760	64 Mb (S25FL064P) / 32 Mb (S25FL032P)
EP2S180	49,814,760	64 Mb (S25FL064P) / 32 Mb (S25FL032P)

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Table 10. SPI Flash Selection for Stratix II GX Family FPGA Devices

FPGA	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP2GX30C/D	9,640,672	16 Mb (S25FL116K) / 8 Mb (S25FL208K)
EP2GX60C/D/E	16,951,824	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP2GX90E/F	25,699,104	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP2GX130G	37,325,760	64 Mb (S25FL064P) / 32 Mb (S25FL032P)

Notes:

1. *Final data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Table 11. SPI Flash Selection for Arria GX Family FPGA Devices (Sheet 1 of 2)

Device	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP1AGX20C/D	7,203,621	8 Mb (S25FL208K) / 8 Mb (S25FL208K)
EP1AGX35C/D	10,859,197	16 Mb (S25FL116K) / 8 Mb (S25FL208K)
EP1AGX50C/D	14,514,773	16 Mb (S25FL116K) / 16 Mb (S25FL116K)

Table 11. SPI Flash Selection for Arria GX Family FPGA Devices (Sheet 2 of 2)

Device	# of Configuration Bits (1)	Minimum SPI Flash Device (Cypress Part Number) (2)
EP1AGX60C/ D/E	16,951,824	32 Mb (S25FL032P) / 16 Mb (S25FL116K)
EP1AGX90E	25,699,104	32Mb (S25FL032P) / 16 Mb (S25FL116K)

Notes:

1. *Preliminary data values from Altera.*
2. *Device sizes are for uncompressed/compressed data files, which assumes a minimum 35% reduction in data size due to compression.*

Figure 7. Stratix III/IV FPGA Configuration with Both ISP and JTAG Programming Capability

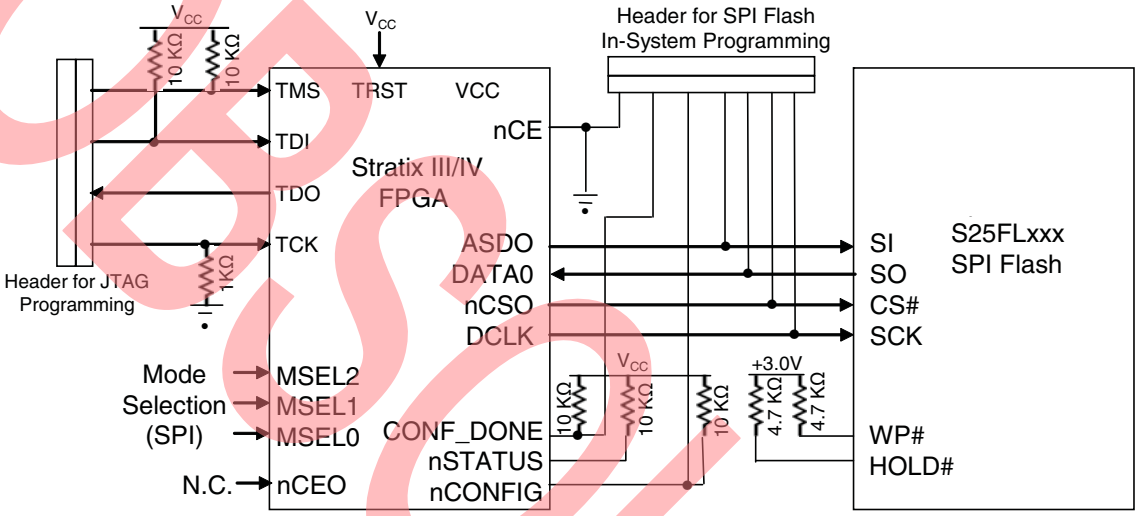
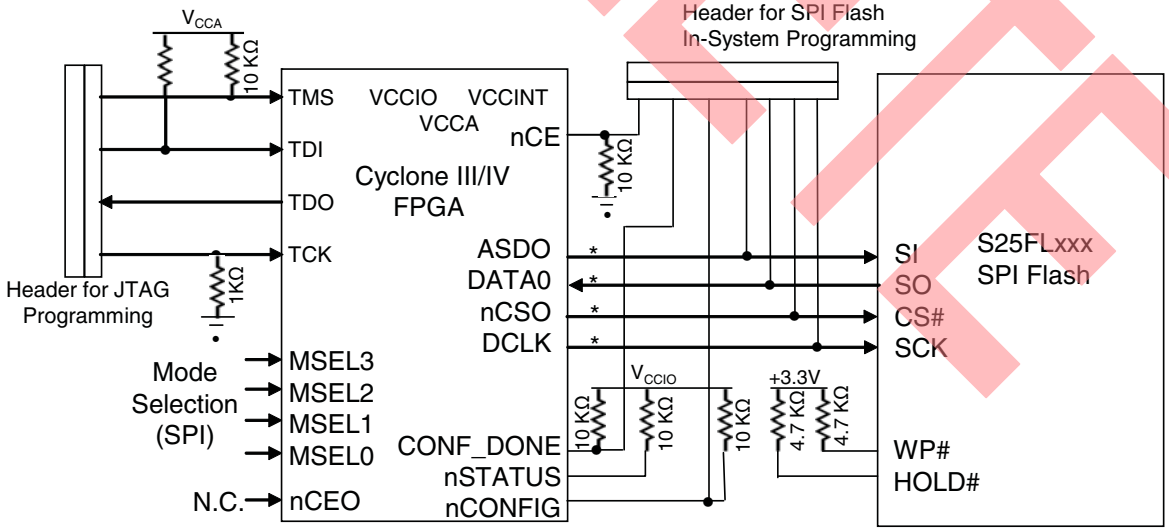
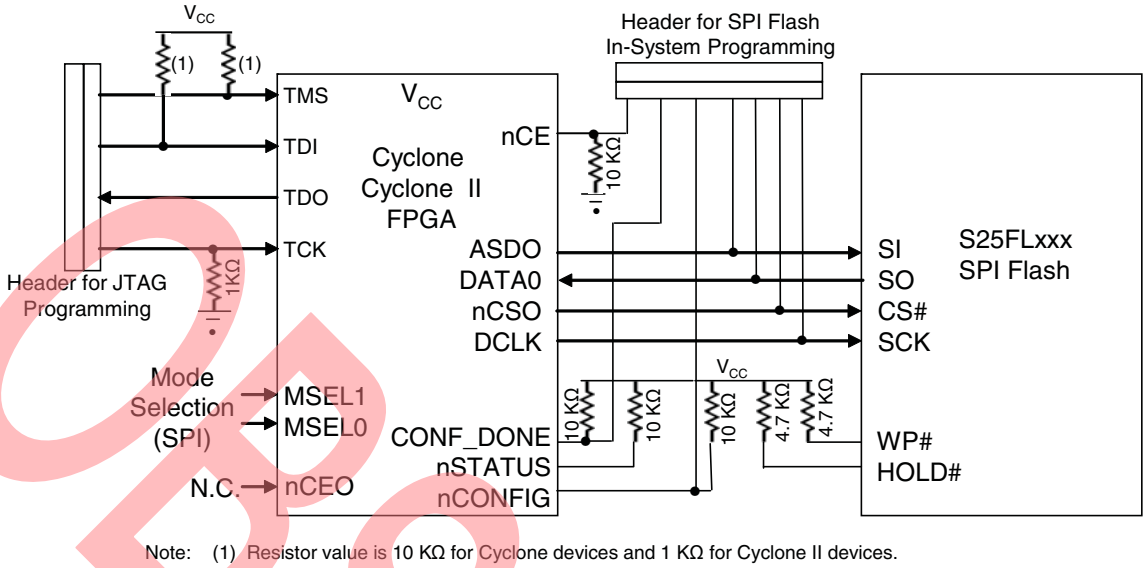


Figure 8. Cyclone III/IV FPGA Configuration with Both ISP and JTAG Programming Capability



* Forward-biased diodes (BAT54 or equivalent Schottky Barrier) are connected from each SPI signal line to VCCIO, and 10 pF capacitors are connected from each SPI signal line to GND. Place these components as close as possible to the FPGA.

Figure 9. Cyclone/Cyclone II FPGA Configuration with Both ISP and JTAG Programming Capability



Note: (1) Resistor value is 10 KΩ for Cyclone devices and 1 KΩ for Cyclone II devices.

Figure 10. Stratix II/Stratix II GX/Arria GX FPGA Configuration with Both ISP and JTAG Programming Capability

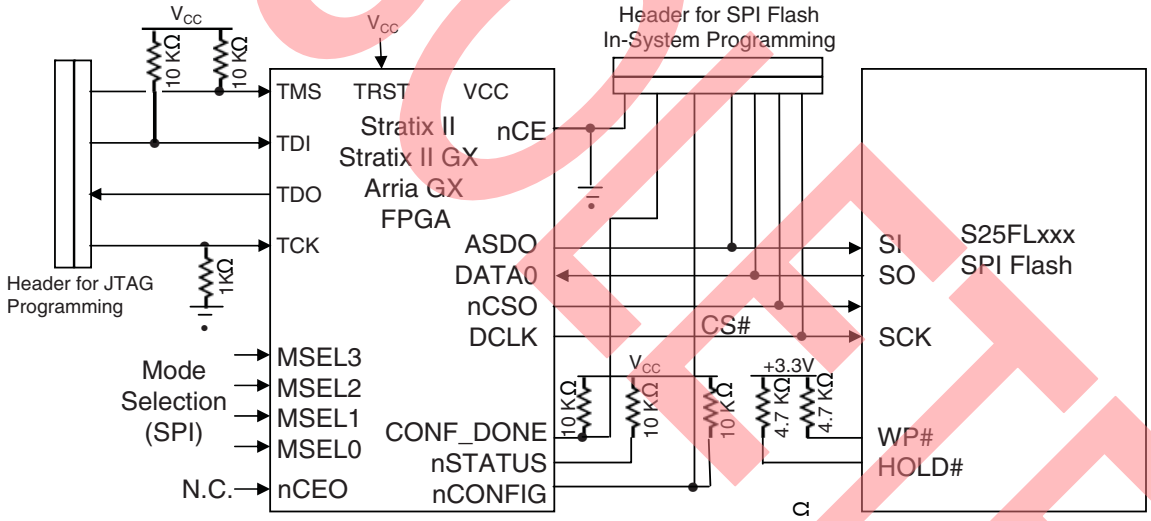


Figure 11. Pin Orientation for 10-Pin Male Header

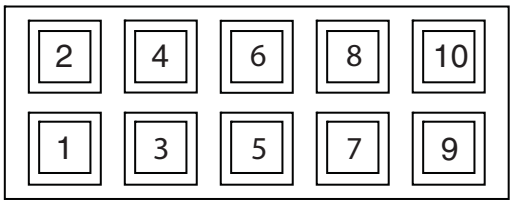


Table 12. Pin Assignments for Direct and JTAG Programming Headers

Pin	Direct Programming	JTAG Programming
1	DCLK/SCK	TCK
2	GND	GND
3	CONF_DONE	TDO
4	VCC (1)	VCC (2)
5	nCONFIG	TMS
6	nCE	VIO (3)
7	ASDO/SI	N.C.
8	nCS0/CS#	N.C.
9	DATA0/SO	TDI
10	GND	GND

Notes:

1. *Connect the download cable power pin to the same voltage used for the pull-up resistors connected to the direct programming header.*
2. *Connect the download cable power pin to the same voltage used for the pull-up resistors connected to the JTAG programming header.*
3. *VIO is a reference voltage for the output driver of the MasterBlaster download cable. For the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when the JTAG interface is used for active serial programming, otherwise this pin is a no connect.*

Table 13. Pin Descriptions for FPGA Configuration from SPI Flash (Sheet 1 of 2)

Pin Name	Type	FPGA	Description
MSEL[1:0] MSEL[2:0] MSEL[3:0]	Input Input Input	Cyclone / Cyclone II Stratix III Cyclone III / Stratix II / Arria GX	Mode Pins. Selects FPGA configuration scheme. These input pins must be hard wired to VCC or GND. These pins have internal pull-down resistors that are always active.
nCONFIG	Input	All FPGA families	Configuration Control. Pulling nCONFIG pin low during user-mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all its I/O pins. Transitioning this pin high starts a reconfiguration.
nSTATUS	Open-drain, bidirect. I/O	All FPGA families	nStatus I/O. The device drives nSTATUS low immediately after power-up and releases it after the Power-On Reset time. Status output. If an error occurs during configuration, nSTATUS is pulled low by the target device. Status input. If an external source drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device.
CONF_DONE	Open-drain, bidirect. I/O	All FPGA families	Status I/O. Status output. The target device drives the CONF_DONE pin low before and during configuration. Once the device receives all its configuration data without error and the initialization cycle begins, the CONF_DONE output is released by the device. Status input. This pin must have an external 10 KΩ pull-up resistor in order for the device to initialize. After the device receives all its configuration data, the CONF_DONE pin transitions high and the device initializes and enters user mode. Device configuration is unaffected by CONF_DONE being driven low after configuration and initialization has completed.
nCE	Input	All FPGA families	Active-Low Chip Enable. A low signal to nCE enables the device for configuration. nCE must be held low during configuration, initialization and user mode. Tie this pin low with a pull-down resistor.
nCEO	Output	All FPGA families	Cascade Chip Enable. Used to cascade to nCE pin of next device in multi-device configuration. In single-device configuration, this pin is left floating.
DATA0	Input	All FPGA families	Data Input. Serial configuration data from the SPI flash device is presented to the target device on the DATA0 pin in AS mode. After configuration, DATA0 is available as a user I/O pin. This pin has an internal pull-up resistor that is always active.
ASDO	Output	All FPGA families	Data Output. Control signal from the target device in AS mode to the SPI flash device used to read out configuration data. In AS mode, ASDO has an internal pull-up resistor that is always active.

Table 13. Pin Descriptions for FPGA Configuration from SPI Flash (Sheet 2 of 2)

Pin Name	Type	FPGA	Description
DCLK	Output	All FPGA families	Data Clock. In AS mode, DCLK provides the synchronous timing to SPI flash for sending configuration data to target device. It has an internal pull-up resistor that is always active.
nCSO	Output	All FPGA families	Chip Select Output. Enables the SPI flash Chip Select input to send configuration data. It has an internal pull-up resistor that is always active.
TDI	Input	All FPGA families	JTAG Test Data Input. Input instructions as well as test and programming data serially. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required, then connect this pin to Vcc to disable the JTAG circuitry.
TDO	Output	All FPGA families	JTAG Test Data Output. Output instructions as well as test and programming data serially. Data is shifted out on the falling edge of TCK. If the JTAG interface is not required, then leave this pin unconnected to disable the JTAG circuitry.
TMS	Input	All FPGA families	JTAG Test Mode Select. Provides the control signal to determine transitions of the TAP controller state machine. TMS transitions occur on the rising edge of TCK. If the JTAG interface is not required, then connect this pin to Vcc to disable the JTAG circuitry.
TCK	Input	All FPGA families	JTAG Test Clock. Provides the clock to the boundary scan circuitry. Operations occur on both edges of the clock. If the JTAG interface is not required, then connect this pin to GND to disable the JTAG circuitry.
TRST	Input	Stratix families	JTAG Test Reset. Provide an active-low input to asynchronously reset the boundary-scan circuitry. This pin is optional according to IEEE Std. 1149.1. If the JTAG interface is not required, then connect this pin to GND to disable the JTAG circuitry.

Table 14. Logic Level and Voltage Connections for Mode Select Pins (Sheet 1 of 2)

FPGA Family	Configuration Scheme (Note 1)	Mode Select Pin	Applied Logic Level	Voltage Connections
Stratix IV	Fast AS	MSEL2	“0”	Logic 1: VCCPGM Logic 0: GND
		MSEL1	“1”	
		MSEL0	“1”	
Stratix III	Fast AS	MSEL2	“0”	Logic 1: VCCPGM Logic 0: GND
		MSEL1	“1”	
		MSEL0	“1”	
Stratix II Stratix II GX / Arria GX	AS	MSEL3	“1”	Logic 1: VCCPD Logic 0: GND
		MSEL2	“1”	
		MSEL1	“0”	
		MSEL0	“1”	
	Fast AS	MSEL3	“1”	
		MSEL2	“0”	
		MSEL1	“0”	
		MSEL0	“0”	
Cyclone III	AS	MSEL3	“0”	Logic 1: VCCA Logic 0: GND
		MSEL2	“0”	
		MSEL1	“1”	
		MSEL0	“0”	
	Fast AS	MSEL3	“1”	
		MSEL2	“1”	
		MSEL1	“0”	
		MSEL0	“1”	

Table 14. Logic Level and Voltage Connections for Mode Select Pins (Sheet 2 of 2)

FPGA Family	Configuration Scheme (Note 1)	Mode Select Pin	Applied Logic Level	Voltage Connections
Cyclone II	AS	MSEL1	"0"	Logic 1: VCCIO Logic 0: GND
		MSEL0	"0"	
	Fast AS	MSEL1	"1"	
		MSEL0	"0"	
Cyclone	AS	MSEL1	"0"	Logic 0: GND
		MSEL0	"0"	

Note:

1. *All FPGA families operate up to 40 MHz, except the Cyclone family with 20 MHz maximum frequency.*

Table 15. Cyclone IV Logic Level and Voltage Connections for Mode Select Pins

FPGA Family	Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Voltage Connections (V)
Cyclone IV GX EP4CGX15, EP4CGX22, EP4CGX30 [except for F484 Package]	AS	—	1	0	1	Fast	3.3
		—	0	1	1	Fast	3.0, 2.5
		—	0	0	1	Standard	3.3
		—	0	1	0	Standard	3.0, 2.5
Cyclone IV GX EP4CGX30 [only for F484 package], EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150	AS	1	1	0	1	Fast	3.3
		1	0	1	1	Fast	3.0, 2.5
		1	0	0	1	Standard	3.3
		1	0	1	0	Standard	3.0, 2.5
Cyclone IV E	AS	1	1	0	1	Fast	3.3
		0	1	0	0	Fast	3.0, 2.5
		0	0	1	0	Standard	3.3
		0	0	1	1	Standard	3.0, 2.5

5 Power Management

Power management, including power ramp-up rate, ramp-up voltage differentials and power sequencing are beyond the scope of this application note. Refer to power management literature from Altera for this information.

6 References

- Altera Cyclone Device Handbook: Chapter 13 – Configuring Cyclone FPGAs (ver 1.7, Jan 2007)
- Altera Cyclone II Device Handbook: Chapter 13 – Configuring Cyclone II Devices (ver 1.2, Feb 2007)
- Altera Cyclone III Device Handbook: Chapter 10 – Configuring Cyclone III Devices (ver 1.1, Jul 2007)
- Altera Stratix II GX Device Handbook, Volume 2: Chapter 13 – Configuring Stratix II and Stratix II GX Devices (ver 4.5, Oct 2007)
- Altera Stratix III Device Handbook, Volume 1: Chapter 11 – Configuring Stratix III Devices (ver 1.3, Nov 2007). For example, Chapter 10 of Volume 1 of the Stratix III Device Handbook, titled "Hot Socketing and Power-On Reset" would contain the power management information required by the designer
- Altera Arria GX Device Handbook, Volume 2: Chapter 11 - Configuring Arria GX Devices (ver 1.1, Aug 2007)
- Altera Nios II Flash Programmer User Guide (ver 2.1, Feb 2010) http://www.altera.com/literature/ug/ug_nios2_flash_programmer.pdf
- Altera Parallel Flash Loader Megafunction User Guide (ver 1.1, Feb 2011) http://www.altera.com/literature/ug/ug_pfl.pdf

- Altera Stratix IV Device Handbook Volume 1: 10. Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices (ver SIV51010-3.3, April 2011) http://www.altera.com/literature/hb/stratix-iv/stx4_siv51010.pdf
- Altera Cyclone IV Device Handbook, Volume 1: 8. Configuration and Remote System Upgrades in Cyclone IV Devices (ver CYIV-51008-1.3, December 2010) http://www.altera.com/literature/hb/cyclone-iv/cyiv-51008.pdf
- Altera AN 370: Using the Serial Flash Loader with the Quartus II Software (ver 3.1, April 2009) http://www.altera.com/literature/an/an370.pdf

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**			02/20/2008	Initial version
*A			10/17/2008	Changes to Figure 3.10 and Tables 3.3, 3.4, 3.7, and 3.8
*B			04/05/2011	SPI Flash Connections to FPGAs section: Updated tables: SPI Flash Selection for Stratix III Family FPGA Devices SPI Flash Selection for Stratix II GX Family FPGA Devices SPI Flash Selection for Stratix II Family FPGA Devices SPI Flash Selection for Cyclone III Family FPGA Devices SPI Flash Selection for Cyclone II Family FPGA Devices SPI Flash Selection for Cyclone Family FPGA Devices SPI Flash Selection for Arria GX Family FPGA Devices Added table: Altera EPCS to Spansion SPI Compatible Device Mapping Added section: Active Serial Mode Programming of Spansion SPI Flash with Altera Quartus II V10.1 Added section: Programming Spansion SPI Flash via the Parallel Flash Loader (PFL) Megafunction Added section: Added References
*C			11/16/2011	Configuration Considerations and Methods: Moved section to go after Introduction SPI Basics: Moved section to go after Configuration Considerations and Methods SPI Flash Connections to FPGAs: Moved section to go after SPI Basics Updated section: Introduction: Modified last sentence Added paragraph Updated section: SPI Flash Connections to FPGAs Reordered section Added table: SPI Flash Selection for Cyclone IV E Family FPGA Devices Added table: SPI Flash Selection for Stratix IV Family FPGA Devices Logic Level and Voltage Connections for Mode Select Pins table: added Stratix IV Added table: Cyclone IV Logic Level and Voltage Connections for Mode Select Pins Updated section: References Updated section: SPI Flash Connections to FPGAs Removed paragraph: “Spansion does not support Altera's Remote System Update (RSU) feature and recommends that it be disabled in software.” Updated notes to two figures: Cyclone III/IV FPGA Configuration from Spansion SPI Serial Flash Connection and Cyclone III/IV FPGA Configuration with Both ISP and JTAG Programming Capability
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*F	5798790	AESATMP8	07/05/2017	Updated logo and Copyright.
*G	6120751	SZZX	04/03/2018	Obsoleting the spec.

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