AN96614

Migrating from SPI EEPROM to Cypress's SPI F-RAM™

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AN96614 provides an overview about advantages and differences to be considered when migrating from a SPI EEPROM to Cypress's high-reliability and energy-efficient SPI F-RAM solution.

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1 Introduction

EEPROMs are frequently used for nonvolatile storage of a system's data. However, a slow nonvolatile write performance and limited write endurance of the EEPROMs limit their usages in systems that need to execute frequent writes to the nonvolatile memory at bus speed. Many system designs have tried to resolve issues associated with EEPROMs by using a wear-leveling technique to increase the effective endurance, but at the cost of increased EEPROM density and software overheads. The other alternative method to save critical system data is to store data in the scratchpad RAM and then transfer the stored data into the nonvolatile memory, such as EEPROMs or flash, at power down by using a backup power source. Both of these methods are highly inefficient because of increased number of components, board space, hardware design complexities, and the software overheads.

Cypress's SPI F-RAM is a serial, nonvolatile memory employing an advanced ferroelectric process and offers the world's most energy-efficient, high-performance, and high-reliability nonvolatile RAM solution. Cypress's SPI F-RAMs are available in both industrial and automotive grade temperatures.

Cypress's F-RAM has fast random access SRAM memory cells and provides virtually infinite (10^{14}) read/write endurance cycles, orders of magnitude higher than an EEPROM. The F-RAM performs write operations at the bus speed without incurring any write delays (NoDelay™) unlike serial EEPROMs and flash memories. Data is directly written into the F-RAM array; the next bus cycle can start immediately without checking the readiness of the device before subsequent access.

The serial SPI F-RAM devices are available as drop-in replacements to the standard SPI EEPROM devices. This application note shows the differences between an industry-standard SPI EEPROM and Cypress's SPI F-RAM solution. These differences need to be considered when migrating from an SPI EEPROM-based solution to Cypress's SPI F-RAM solution. This application note references the M95M01 and AT256B SPI EEPROM datasheets for comparison.

For more details on SPI F-RAM designs, refer to the application note AN304 - SPI Guide for F-RAM™.

For more details on the benefits of Cypress's F-RAM over a serial EEPROM, refer to the application note AN87352–F-RAM™ for Smart E-Meters.

2 Benefits of SPI F-RAM over EEPROM

2.1 Faster Memory

- Random access: No page reads/writes needed.
- Full memory write at bus speed without any internal page program delay after each page write.

2.2 Easier Design

- No software overhead for managing page boundary as with EEPROM
- Virtually infinite (10^{14}) read/write endurance cycles do not require wear leveling
- Available in industry-standard packages

2.3 Data Security

- Reliable, advanced ferroelectric process
- No requirement of a battery or capacitor backup to store the last moment data

2.4 Additional Features

- Cypress's F-RAM is world's most energy-efficient, fast nonvolatile RAM
- 151 years of data retention at 65 ºC
- Pb-free technology

3 Migrating from SPI EEPROM to SPI F-RAM

Cypress's SPI F-RAMs are available in two industry-standard packages: 8-pin SOIC and 8-pin DFN. These standard and versatile package options make Cypress's SPI F-RAMs drop-in replacements for the majority of the EEPROMs on the same footprint without compromising the system's performance. In addition, Cypress's F-RAM solution provides performance advantages such as higher data throughput, NoDelay™ write, and energy-efficient operation.

The following sections highlight all key differences and compatibilities between an SPI EEPROM and an SPI F-RAM.

3.1 Pin and Package Compatibility

Cypress's SPI F-RAMs are pin- and package-compatible with SPI EEPROMs. Table 1 shows the pin mapping and Table 2 shows the package comparison of SPI EEPROMs and SPI F-RAMs.

Table 1. SPI EEPROM and SPI F-RAM Pin Mapping

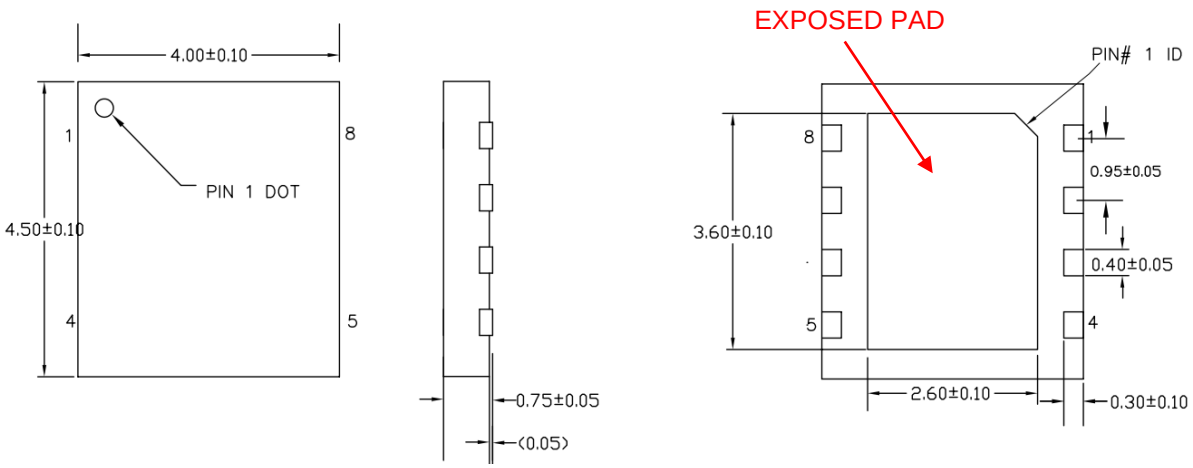
Pin Description	Pin Name	
	SPI EEPROM	Cypress's SPI F-RAM
Chip select	$\overline{SS}$ / $\overline{S}$ / $\overline{CS}$	$\overline{CS}$
Serial clock	C/SCK	SCK
Serial data input	D/SI	SI
Serial data output	Q/SO	SO
Write protect	$\overline{W}$ / $\overline{WP}$	$\overline{WP}$

Pin Description	Pin Name	
	SPI EEPROM	Cypress's SPI F-RAM
Hold	$\overline{HOLD}$	$\overline{HOLD}$
Power supply	V_{CC}/V_{DD}	V_{DD}
Ground	V_{SS}/GND	V_{SS}

Table 2. SPI EEPROM and SPI F-RAM Package Comparison

Feature/Function	SPI EEPROM	SPI F-RAM	Comments
DFN EXPOSED PAD	No connect	No connect	The EXPOSED PAD of F-RAM 8-pin DFN package is an NC (No connect) pad; therefore, it can be either floating or connected to V_{SS}/V_{DD}. Cypress doesn't recommend soldering the F-RAM DFN EXPOSED PAD on the PCB.
Package options	8-pin DFN, 8-pin SOIC (150 mils), 8-pin SOIC (208 mils), 8-pin PDIP, 8-pin TSSOP, 8-pin dBGA, 8-pin UDFN, 8-WLCSP, 8-pin MSOP	8-pin DFN, 8-pin SOIC (150 mils), 8-pin SOIC (208 mils),	The standard 8-pin DFN and 8-pin SOIC packages of EEPROMs can be replaced by the SPI F-RAMs. Other SPI EEPROM packages are incompatible with the SPI F-RAM and so will require changes to the PCB.

Figure 1. SPI F-RAM 8-pin DFN (4 mm × 4.5 mm × 0.75 mm) Package Outline



The SPI F-RAM EXPOSED PAD is not connected to the die hence should be left floating. Ensure that the EXPOSED PAD of the SPI F-RAM DFN package is not soldered on the PCB when migrating to SPI F-RAM from SPI EEPROM. Doing so will cause the SPI F-RAM die to be exposed to excessive heat, which can result in bit failures and margin loss.

3.2 Command (OPCODE) Compatibility

Table 3 shows the list of opcodes supported in SPI EEPROMs and SPI F-RAMs. Opcodes specific to EEPROM cell operations such as RDID (ABh), PE0 (42h), SE0 (D8h), which are shown in Table 3, are don't care commands for SPI F-RAMs; these are ignored by the SPI F-RAM when executed. The SPI F-RAM cannot replace the SPI EEPROM that has these special features if the application uses these features.

Table 3. OPCODE Comparison

Command OPCODE (Hex)	Command Description	SPI EEPROM	SPI F-RAM	Comments
WREN (06h)	Set write enable latch	√	√	Identical functionality.
WRDI (04h)	Reset write enable latch	√	√	
RDSR (05h)	Read Status Register	√	√	
WRSR (01h)	Write Status Register	√	√	Advantage: F-RAM doesn't require a nonvolatile write delay of 5 ms after the Status Register write.
READ (03h)	Read memory data	√	√	Identical functionality.
WRITE (02h)	Write memory data	√	√	Advantage: The address counter in the SPI EEPROM burst write rolls over at the EEPROM page boundary. EEPROM requires a nonvolatile write delay of 5 ms after every byte/page write. The SPI F-RAM burst write operation allows writing the entire memory at bus speed without any write delay. The address counter rolls over at the last memory location.
FSTRD (0Bh)	Fast read memory data	X	√	Not supported in EEPROM
SLEEP (B9h)	Enter sleep mode	√	√	Identical functionality
RDID (9Fh)	Read device ID	X	√	Not supported in EEPROM.
SNR (C3h)	Read serial number	X	√	
RDID (ABh)	Release from deep power down (Not available as standard instruction)	√	X	These commands are not the standard SPI EEPROM commands. These commands are supported only in specific EEPROMs. These commands are not supported in the SPI F-RAMs.
PE0 (42h)	Page erase	√	X	
SE0 (D8h)	Sector erase	√	X	
RDID (83h)	Reads the page dedicated to identification	√	X	
WRID (82h)	Writes the page dedicated to identification	√	X	
RDLS (83h)	Reads the lock status of the identification page	√	X	
LID (82h)	Lock the identification page in read-only mode	√	X	

3.3 Status Register Compatibility

The Status Register access in the SPI EEPROM and the SPI-FRAM are identical except that EEPROMs allow reading the Status Register in a loop without resending the Read Status Register command (RDSR). The host controller can poll the EEPROM Status Register in a loop to determine the “Ready” or the “Write In Progress” status ($\overline{RDY}$ / WIP). In contrast, the SPI F-RAM is always ready for the next instruction immediately after the ongoing instruction completes; therefore, in any case, the SPI F-RAM does not need reading the Status Register continuously. This will be an improvement in the firmware when using the SPI F-RAM.

Reading the SPI F-RAM Status Register will always return a “Ready” status. When migrating from the SPI EEPROM to SPI F-RAM, the firmware must ensure that either it reads only one byte per Status Register read command, or if it reads multiple bytes then firmware ignores all bytes except the first byte. Table 4 shows the Status Register bits definitions for SPI EEPROMs and SPI F-RAMs and their compatibilities.

Table 4. Status Register Comparison

Status Register	SPI EEPROM	SPI F-RAM	Comments
Bit0	$\overline{RDY}$ / WIP	Don’t Care (0)	The SPI EEPROM sets this bit to ‘1’ when it is busy during a page write operation. The SPI F-RAM always returns ‘0’ indicating it is ready. Therefore, migrating to the SPI F-RAM does not require any firmware change.
Bit1	WEL	WEL	Identical behavior.
Bit2	BP0	BP0	
Bit3	BP1	BP1	
Bit4	Don’t Care (0)	Don’t Care (0)	
Bit5	Don’t Care (0)	Don’t Care (0)	
Bit6	Don’t Care (0)	Don’t Care (0/1)	This bit is the read-only bit in the SPI F-RAM. Some SPI F-RAMs return ‘0’ upon read. (Example: FM25C160B) Some SPI F-RAMs return ‘1’ upon read. (Example: FM25V20A)
Bit7	SRWD	WPEN	Identical behavior.

Note: Bits 4-6 are ‘don’t care’ bits. The default value of these three bits can be ignored when migrating from the SPI EEPROM to the SPI F-RAM.

Figure 2. SPI EEPROM Status Register Read

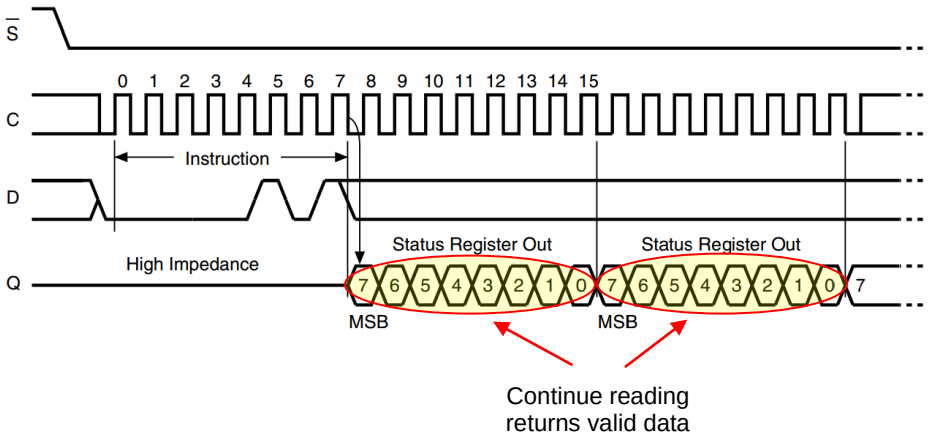
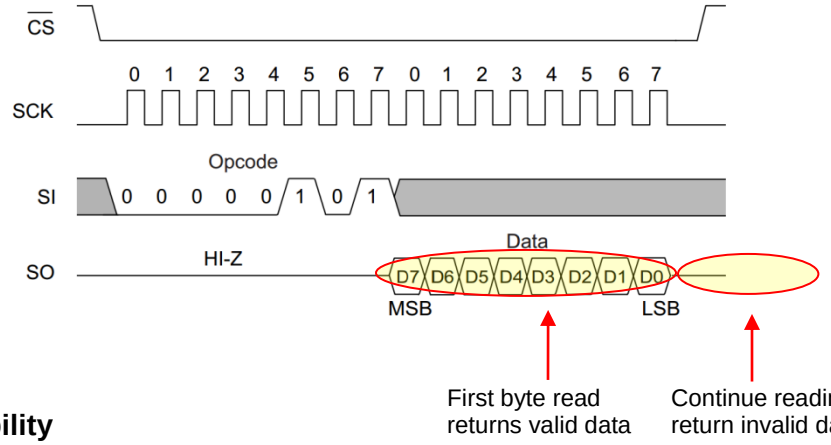


Figure 3. SPI F-RAM Status Register Read



3.4 Hold Compatibility

The $\overline{HOLD}$ pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the $\overline{HOLD}$ pin LOW while SCK is LOW, the current operation will pause. Taking the $\overline{HOLD}$ pin HIGH while SCK is LOW will resume the paused operation. The transitions of $\overline{HOLD}$ must occur while SCK is LOW.

The following are the differences in the $\overline{HOLD}$ behavior between the SPI EEPROMs and the SPI F-RAM:

- The SPI F-RAM allows toggling the SCK and the $\overline{CS}$ pin during a hold state, as shown in Figure 4.
- Some SPI EEPROMs do not allow $\overline{CS}$ toggling in the hold state. Toggling the $\overline{CS}$ during hold can reset the communication in these devices.
- Some SPI EEPROMs allow entering the hold state by toggling the $\overline{HOLD}$ pin LOW when the $\overline{CS}$ is LOW and the SCK is HIGH. Similarly, these devices allow exiting the hold state by toggling the $\overline{HOLD}$ pin HIGH when the $\overline{CS}$ is LOW and the SCK is HIGH. See Figure 5.

Figure 4. SPI EEPROM $\overline{HOLD}$ Timing

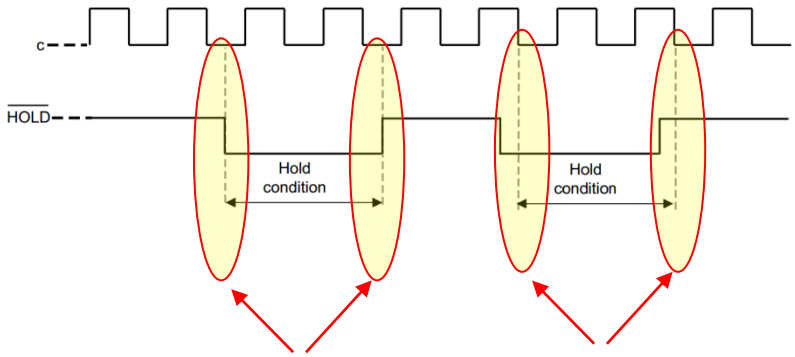
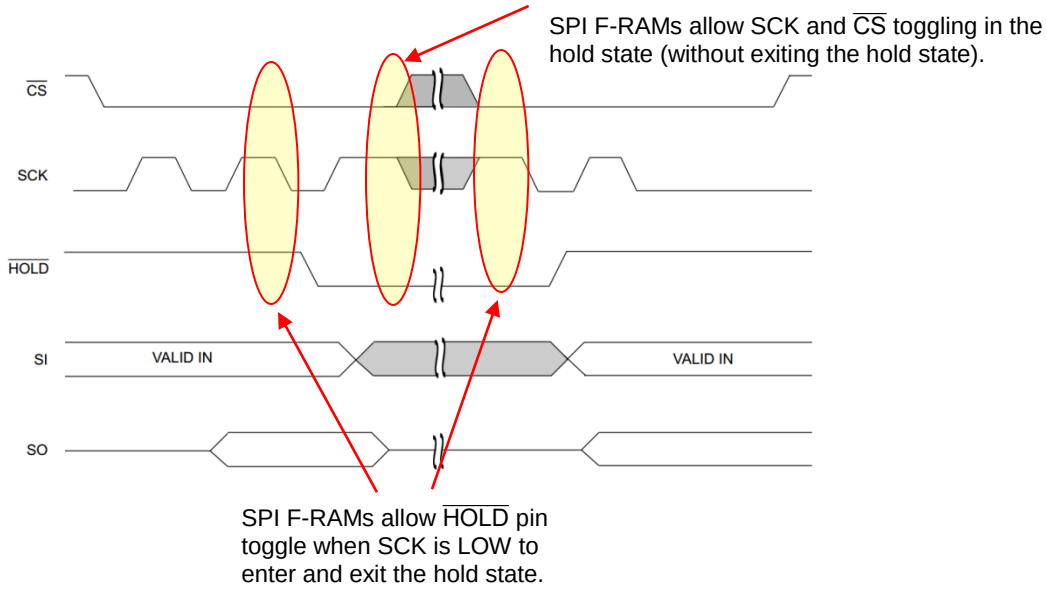


Figure 5. SPI F-RAM $\overline{HOLD}$ Timing



3.5 Parameter Compatibility

Table 5 summarizes the key parameters that need to be evaluated for system-level compatibility when migrating from the SPI EEPROM to Cypress's SPI F-RAM.

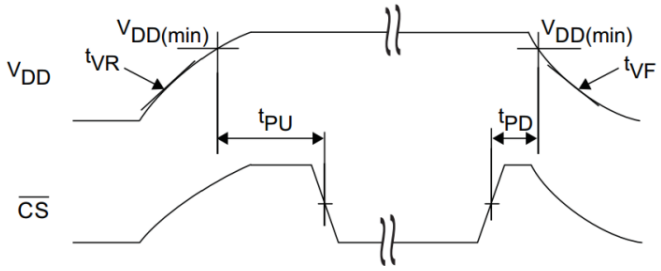
Table 5. Key Parameters Checklist

Parameter	Description	SPI EEPROM	SPI F-RAM	Comments
DC Parameters				
V_{DD}	Power supply voltage	1.5 V to 3.6 V 1.7 V to 5.5 V	2.0 V to 5.5 V	The SPI EEPROMs support a wider operating voltage range. When migrating to the SPI F-RAM, the system must ensure that the SPI F-RAM operating voltage is within its operating range.
V_{IH}	Input HIGH voltage	Varies	0.7 × V_{DD} to V_{DD} + 0.3 V	The SPI F-RAM follows CMOS logic standard. System must ensure that the logic levels are within operating range of both the SPI host and the SPI F-RAM for proper operation.
V_{IL}	Input LOW voltage	Varies	-0.3 V to 0.3 × V_{DD}	
V_{OH}	Output HIGH voltage	Varies	2.4 V (min), I_{OH} = -1 mA; V_{DD} - 0.2 V (min), I_{OH} = -100 µA	The SPI F-RAM output driver supports standard output drive strength which makes it compatible with majority of the host controllers. Systems must ensure that the logic levels are within operating range of both the SPI host and SPI F-RAM for proper operation.
V_{OL}	Output LOW voltage	Varies	0.4 V (max), I_{OL} = +2 mA; 0.2 V (max), I_{OL} = +150 µA	

Parameter	Description	SPI EEPROM	SPI F-RAM	Comments
AC Parameters				
f_{SCK}	SPI clock frequency	Up to 20 MHz	Up to 40 MHz	Migrating from the SPI EEPROM to SPI F-RAM does not require firmware changes. However, because the SPI F-RAM supports a higher access speed, firmware upgrades can improve the data throughput when using the SPI F-RAM.
Power Parameters				
t_{VR}	V_{DD} power-up ramp rate	Varies	30 to 50 µs/V	When migrating to the SPI F-RAM, the system must ensure that the V_{DD} power ramp rate is within the spec of the SPI F-RAM, Figure 6.
t_{VF}	V_{DD} power-down ramp rate	Varies	30 to 100 µs/V	

Other device parameters such as device current in different operating modes, output load, start-up time, power ramp (power-up and power-down), ESD profile and packages that differ between the SPI EEPROM and SPI F-RAM can warrant some system-level analysis before replacing the SPI EEPROM with the SPI F-RAM.

Figure 6. SPI F-RAM Power Cycle Timing



4 Firmware Compatibility

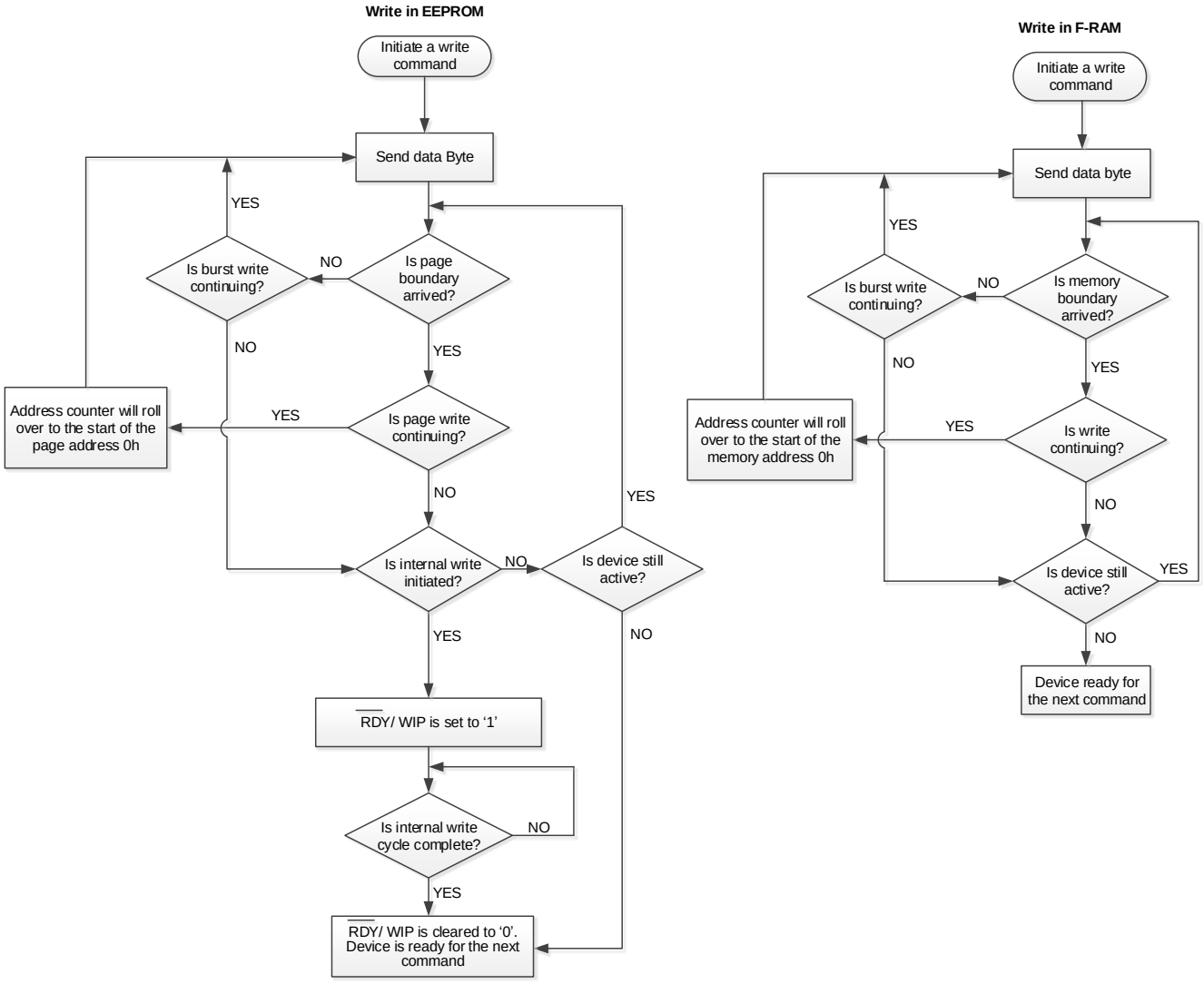
The SPI host controller firmware for the SPI EEPROM access will work as-is for the SPI F-RAM except for the unsupported features/opcodes. This section discusses various operations in EEPROMs that can be improved in the system by firmware updates when migrating to the SPI F-RAM solution.

4.1 Multiple Pages in EEPROMs versus Single Page in F-RAM

EEPROMs are written or programmed on a page-by-page basis. A typical page size of an EEPROM device is 1/512th of the memory size. This means that to write the full EEPROM memory, the host controller needs to initiate 512 page-write operations. The host controller also needs to track the count of the total data bytes written in an individual page to prevent a counter roll over.

The F-RAM does not support page architecture; therefore, the entire memory array can be treated as one page. The entire F-RAM array can be written in the burst mode with a single write command. Once the internal counter reaches the last F-RAM location, the counter rolls over to the start address 0h. Because the SPI F-RAM the write operation contains a single page, the host controller is required to keep track of just one counter for the SPI F-RAM, as opposed to tracking multiple counters for the page count and the byte count in a page. The SPI F-RAM simplifies firmware design by reducing the number of execution steps. Figure 7 demonstrates writing in SPI EEPROM versus writing in SPI F-RAM.

Figure 7. Write Operation in EEPROM and F-RAM



4.2 Page Write Delay

EEPROMs typically require a page write delay of 5 ms to transfer its buffer data into the nonvolatile EEPROM cells. The EEPROM page size varies between densities or between different vendors product for the same density. The system firmware must be designed to take care of the page size variation and the page write delay between different EEPROM parts.

The page write delay is not required in the SPI F-RAM; therefore, the write delay can be removed in the firmware to improve the system's nonvolatile write performance when migrating to the SPI F-RAM.

4.3 $\overline{\text{RDY}}$ / WIP Bit in Status Register

SPI EEPROMs define the Status Register bit0 as Ready ($\overline{\text{RDY}}$) or Write in Progress (WIP). When an EEPROM page write is in progress, the Status Register bit0 is set to '1', indicating that EEOROM is busy. The host controller polls the Status Register $\overline{\text{RDY}}$/WIP bit for the EEPROM status before initiating a new write or read access.

5 Summary

Migrating from the SPI EEPROM to Cypress's SPI F-RAM will improve the system performance, reliability, and energy-efficiency. Cypress's SPI F-RAM's industry-standard pin and package configuration, SPI instruction set (OPCODE), and electrical compatibility simplify the migration. Differences between two devices are highlighted throughout this application note. These differences need to be considered but will typically not be gating for migration in most applications.

6 Related Documents

6.1 Application Notes

- AN304 - SPI Guide for F-RAM™
- AN87352 - F-RAM™ for Smart E-Meters

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*A	5848806	HARA	08/18/2017	Updated logo and copyright.

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