Cypress Roadmap: Timing Solutions
Q2 2020
# Clock Synthesizer Roadmap

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<tr>
<th>Product Family</th>
<th>Features</th>
<th>(Prod) [EOL]</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
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<tr>
<td></td>
<td></td>
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<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
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<tr>
<td>CY27430</td>
<td>4-PLL; Maximum Frequency: 700 MHz 12 Outputs; Dif! &amp; SE²; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter⁴ 1.8 V/2.5 V/3.3 V; Ind²; 48-QFN</td>
<td>EOL</td>
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<tr>
<td>CY27410</td>
<td>4-PLL; Maximum Frequency: 700 MHz 8 Outputs; Dif! &amp; SE; PCIe 3.0; VCXO; EMI; 0.7-ps RMS Jitter 1.8 V/2.5 V/3.3 V; Auto A² ⁴; 48-QFN</td>
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<tr>
<td>CCY254x/CY251x</td>
<td>1-4 PLL; Maximum Frequency: 200 MHz 3-9 Outputs; I²C; EMI; Low Power⁶ 100-ps CCJ; Ind; 1.8 V/2.5 V/3.0 V/3.3 V 8-SOIC; 8/16/20-TSSOP; 24-QFN</td>
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<tr>
<td>CY229x/CY2238x</td>
<td>3-4 PLL; Maximum Frequency: 166 MHz 3-8 Outputs; CMOS; Low Power 200-ps PPJ; VCXO; Ind; 3.3 V/5 V 8/16/20-SOIC; 16-TSSOP</td>
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<tr>
<td>CY2429x</td>
<td>1-PLL; Maximum Frequency: 200 MHz 2-5 Outputs; HCSL, CMOS; EMI 75-ps CCJ; PCIe 1.1; Ind; Auto A 3.3 V; 16-TSSOP; 32-QFN</td>
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<tr>
<td>CY2239x</td>
<td>3-4 PLL; Maximum Frequency: 400 MHz 5-8 Outputs; LVPECL, CMOS; I²C 400-ps PPJ; VCXO; 3.3 V Ind; Auto A E¹; 16-TSSOP; 32-QFN</td>
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<tr>
<td>CY22800/801/CY2581x</td>
<td>1-PLL; Maximum Frequency: 200 MHz 1-3 Outputs; CMOS; EMI 110-ps CCJ; VCXO; Ind; 3.3 V; 8-SOIC; 8-TSSOP</td>
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<tr>
<td>CY22050/150</td>
<td>1-PLL; Maximum Frequency: 200 MHz 6 Outputs; CMOS; I²C 250-ps PPJ; Ind 2.5 V/3.3 V; 16-TSSOP</td>
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</tbody>
</table>

1 Differential and single-ended outputs  
2 Voltage-controlled crystal oscillation  
3 Electro Magnetic Interference reduction using Lexmark profile  
4 Integrated phase noise across 12-kHz to 20-MHz offset  
5 Industrial grade: -40°C to +85°C  
6 AEC-Q100: -40°C to +85°C  
8 AEC-Q100: -40°C to +105°C  
9 Power management options  
10 Cycle-to-cycle jitter  
11 Peak-to-peak period jitter  
12 AEC-Q100: -40°C to +125°C

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**Products supported by Longevity Program unless noted**
### Oscillator Roadmap

<table>
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<tr>
<th>Product Family</th>
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<th>(Prod) [EOL]</th>
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</table>
| CY294x         | 1-PLL; Maximum Frequency: 2.1 GHz  
1 Output; Diff & SE; 40/100 GbE;  
VCXO; 0.11-ps RMS Jitter; Ind;  
8-LCC (7 x 5, 5 x 3.2); 16-QFN |  |  |  |  |  |  |
| CY51x7         | 1-PLL; Maximum Frequency: 2.1 GHz  
1 Output; Diff & SE; 40/100 GbE;  
VCXO; 0.11-ps RMS Jitter; Ind;  
1.8 V/2.5 V/3.3 V; WA/DF/DIE |  |  |  |  |  |  |
| CY2Xx (FleXO™) | 1 PLL; Maximum Frequency: 690 MHz  
1 Output; LVCMOS, LVDS, LVPECL  
Frequency Margining: 0.6-ps RMS Jitter; Ind;  
6-LCC (7 x 5, 5 x 3.2); 8-TSSOP |  |  |  |  |  |  |
| CY25701        | 1-PLL; Maximum Frequency: 166 MHz  
1 Output; CMOS; EMI; 85-ps CCJ;  
Ind; 3.3 V/5.0 V; WA/ER |  |  |  |  |  |  |
| CY2037/ 5037   | 1-PLL; Maximum Frequency: 133 MHz  
1 Output; CMOS; 100-ps CCJ; Ind;  
3.3 V/5.0 V; WA/ER |  |  |  |  |  |  |
| CY5077         | 1-PLL; Maximum Frequency: 166 MHz  
1 Output; CMOS; 75-ps CCJ; Ind;  
1.8 V/2.5 V/3.0 V/3.3 V; WA/ER |  |  |  |  |  |  |
| CY5057         | 1-PLL; Maximum Frequency: 170 MHz  
1 Output; CMOS; EMI; <200-ps CCJ;  
Ind; 3.3 V/5.0 V; WA/ER |  |  |  |  |  |  |

1 Differential and single-ended outputs  
2 Voltage-controlled crystal oscillation  
3 Integrated phase noise across 12-kHz to 20-MHz offset  
4 Industrial grade: -40°C to +85°C  
5 Electromagnetic interference reduction using Lexmark profile  
6 Cycle-to-cycle jitter

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3 Differential and single-ended outputs  
4 Industrial grade: -40°C to +85°C  
5 Electromagnetic interference reduction using Lexmark profile  
6 Cycle-to-cycle jitter

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**Products supported by Longevity Program unless noted**

- **Concept**
- **Samples**
- **Production**
- **EOL - LTB**
- **EOL - LTS**

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**Timing Solutions - DMIT**
# Clock Buffer Roadmap

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<tr>
<th>Product Family</th>
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<tr>
<td><strong>High Performance</strong></td>
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<tr>
<td>CY2DPx/CPx</td>
<td>Maximum Frequency: 1.5 GHz 2-10 Outputs; LVPECL; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 8-SOIC; 32-TQFP</td>
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<tr>
<td>CY2DMx/DLx</td>
<td>Maximum Frequency: 1.5 GHz 2-10 Outputs; LVDS, CML; 2.5 V/3.3 V 0.11-ps Additive Jitter; Ind 8/20-TSSOP; 32-TQFP</td>
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<tr>
<td>CY230x/EP0x (Zero Delay)</td>
<td>Maximum Frequency: 220 MHz 2-9 Outputs; LVCMOS; 2.5 V/3.3 V 0.22-ps CCLP; Ind; Auto A 8/16-SOIC, 16-TSSOP, WAFAER</td>
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<tr>
<td>CY230xNZ/ 2994x (Non-Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4-18 Outputs; LVCMOS 100-ps Op-Op Skew; Ind 2.5 V/3.3 V</td>
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<tr>
<td>CY23FS04/08/FP12 (Zero Delay)</td>
<td>Maximum Frequency: 200 MHz 4-12 Outputs; LVCMOS; Fail Safe 200-ps CCJ; Ind; 2.5 V/3.3 V 16/28-SOIC</td>
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<tr>
<td>CY23S0x (Zero Delay)</td>
<td>Maximum Frequency: 133 MHz 5-9 Outputs; LVCMOS Spread Aware; 90-ps CCJ; Ind; 2.5 V/3.3 V</td>
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<tr>
<td>CY7B99x (RoboClock™)</td>
<td>Maximum Frequency: 200 MHz; 8-13 Outputs Configurable Skew; 2.5 V/3.3 V/5.0 V 50-ps CCJ; Ind; 24-SOIC; 32-PLCC; 32/44/52,100-TQFP; 100-BGA</td>
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</table>

1 Additive RMS phase jitter
2 Additive RMS phase jitter
3 Cycle-to-cycle jitter
4 Industrial grade: -40°C to +85°C
5 AEC-Q100: -40°C to +85°C

Products supported by Longevity Program unless noted

4 Timing Solutions - DMIT
### Timing Solutions Portfolio

**Programmable | High-Performance | EMI Reduction | Automotive**

#### Clock Synthesizers

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<th>Production</th>
<th>EOL</th>
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<tr>
<td>CY27410</td>
<td>4-PLL; Max Freq: 700 MHz</td>
<td>QFN</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY27430</td>
<td>4-PLL; Max Freq: 700 MHz</td>
<td>QFN</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY29430</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
<td>QFN</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY2242x/CY251x</td>
<td>4-PLL; Max Freq: 200 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY229x/CY2238x</td>
<td>4-PLL; Max Freq: 166 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY2280x/801/CY2581x</td>
<td>1-PLL; Max Freq: 200 MHz</td>
<td>SSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY22050/150</td>
<td>1-PLL; Max Freq: 200 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<td>CY2941x/2x</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
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<td>VQFN</td>
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<tr>
<td>CY51x7</td>
<td>1-PLL; Max Freq: 2.1 GHz</td>
<td>QFN</td>
<td>Q100:</td>
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<td>CY29507</td>
<td>1-PLL; Max Freq: 166 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY5057</td>
<td>1-PLL; Max Freq: 170 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
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<tr>
<td>CY25701</td>
<td>1-PLL; Max Freq: 166 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY2037/ 5037</td>
<td>1-PLL; Max Freq: 133 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
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<td>CY250701</td>
<td>1-PLL; Max Freq: 166 MHz</td>
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<td>CY25077</td>
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<td>Q100:</td>
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<tr>
<td>CY2308/5080/5012</td>
<td>Zero Delay) Max Freq: 200 MHz</td>
<td>TSSOP</td>
<td>Q100:</td>
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<tr>
<td>CY2308/5080/5012</td>
<td>Zero Delay) Max Freq: 200 MHz</td>
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<td>Q100:</td>
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#### Clock Buffers

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<tr>
<th>Model</th>
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<th>Production</th>
<th>EOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY2DPx/CPx</td>
<td>Max Freq: 1.5 GHz</td>
<td>QFN</td>
<td>Q100:</td>
<td>VQFN</td>
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<tr>
<td>CY2Dmx/DLx</td>
<td>Max Freq: 1.5 GHz</td>
<td>QFN</td>
<td>Q100:</td>
<td>VQFN</td>
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1. Differential and single-ended outputs
2. Voltage-controlled crystal oscillation
3. Electromagnetic interference reduction using Lexmark profile
4. Integrated phase noise across 12-kHz to 20-MHz offset
5. Industrial grade: -40°C to +85°C
6. AEC-Q100: -40°C to +85°C
7. AEC-Q100: -40°C to +105°C
8. Additive RMS phase jitter
9. Power management options
10. Cycle-to-cycle jitter
11. Peak-to-peak period jitter
12. AEC-Q100: -40°C to +125°C

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Additional details on availability and performance can be found in the Timing Solutions Portfolio brochure available for download from the CYPRESS website.
CY27410: High-Performance 4-PLL Clock Generator

**Applications**
Multifunction printers, digital TVs, Blu-ray recorders, home gateways, femtocells, routers and switches

**Features**
- **Twelve Outputs**
  - Eight configurable (differential or single-ended)
  - Four single-ended
- **Specifications**
  - High frequency: 700-MHz differential, 250-MHz single-ended
  - RMS phase jitter <0.7 ps (typical)
  - Reference clock support for PCIe 3.0, SATA 2.0 and 10 GbE
  - Industrial temperature grade
- **Additional Features**
  - Pin select and I²C programming
  - Configurable as zero or non-zero delay buffer
  - Glitch-free frequency switching
  - Frequency Select option to choose from eight pre-programmed configurations
  - Early/late clocks
  - PLL cascading
  - Voltage-controlled frequency synthesis (VCFS)
- **RoHS-Compliant Package**
  - Available in a 7 mm x 7 mm 48-pin QFN package

**Collateral**
**Datasheet:** 4-PLL High-Performance Clock Generator (CY274X)
CY2941x/2x: High-Performance 1-PLL Programmable Oscillator

Applications
Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

Features
- Outputs
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\) and CML\(^4\) outputs
- Specifications
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Pin select and \(\text{I}^2\text{C}\) programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- RoHS-Compliant Packages
  - Available in a 5 mm x 7 mm, 5 mm x 3.2 mm 8-pin LCC\(^9\) package

Collateral
Datasheet: 1-PLL High-Performance Programmable Oscillator (CY2941x/2x)

1 Low-voltage positive emitter coupled logic
2 Low-voltage differential signaling
3 High-speed current steering logic
4 Current mode logic
5 The uncertainty of the clock rising and falling edge timing
6 \(\text{I}^2\text{C}\) input
7 Voltage input pin for VCFS
8 Frequency select inputs
9 Leadless ceramic chip carrier
CY29430: High-Performance 1-PLL Clock Synthesizer

Applications
Routers, switches, base stations, storage area networks, network backplanes, wireless infrastructure, military/aerospace, video, test and measurement

Features
- Outputs
  - LVPECL\(^1\), LVDS\(^2\), HCSL\(^3\), CML\(^4\) and LVCMOS outputs
- Specifications
  - High frequency: 2.1-GHz differential, 250-MHz single-ended
  - RMS phase jitter\(^5\): ~110 fs typical (12-kHz to 20-MHz frequency offsets) for output greater than 150 MHz
  - Voltage-controlled frequency synthesis (VCFS) with tuneable pull range of 50 ppm to 275 ppm
  - Frequency Select option to choose from four pre-programmed configurations
  - Pin select and \(I^2C\) programming
  - VDD support: 1.8 V, 2.5 V, and 3.3 V
  - Industrial temperature grades (-40°C to +105°C)
- RoHS-Compliant Package
  - Available in a 3 mm x 3 mm 16-pin QFN\(^9\) package

Collateral
Datasheet: 1-PLL High-Performance Clock Synthesizer (CY29430)

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1 Low-voltage positive emitter coupled logic
2 Low-voltage differential signaling
3 High-speed current steering logic
4 Current mode logic
5 The uncertainty of the clock rising and falling edge timing
6 \(I^2C\) input
7 Voltage input pin for VCFS
8 Frequency select inputs
9 Quad flat no-leads