

Supporting ACA-Dock Feature in Smartphone and Tablet Docks with HX3 USB 3.0 Hub Controller – KBA96321

1. Introduction

Accessory Charger Adapter Dock (ACA-Dock) enables charging and simultaneous data transfer for a mobile phone or a tablet (acting as an OTG² Host) with support for Battery Charging Specification Version 1.2 (BC v1.2). The <u>CY4613 Development kit</u> helps you evaluate the HX3 – the industry's only USB 3.0 Hub controller with the ACA-Dock feature. The <u>CYUSB3324</u> and <u>CYUSB3328</u> parts of the HX3 product family support ACA-Dock feature.

When a USB ACA-Dock-capable phone or tablet is connected to the CY4613 board's upstream (US) port, it is charged by the US port using HX3's ACA-Dock feature. At the same time, the connected phone or tablet enumerates the CY4613 hub, and devices connected to the downstream (DS) ports of CY4613 work as expected.

2. Supporting BC v1.2-Compliant, ACA-Dock-Capable Phones

A mobile phone or tablet connected to the US port of HX3 monitors the resistor (RID_A) value connected to the ID pin (Refer Figure 1). If the RID_A value matches the resistance value expected by the USB OTG host in the phone or tablet, the host allows the enumeration of HX3 and devices connected to the DS port of HX3. At the same time, the connected mobile phone or tablet is charged by the US port of HX3.

Figure 1 shows the HX3 hub system in the ACA-Dock mode as implemented in the CY4613 board. The CY4613 supports the RID_A (CY4613 schematics: R25) of 124 k Ω (standard RID_A value as per the BC v1.2 specification) by default. Refer to Step 9 of the CY4613 Quick Start Guide to configure the CY4613 for ACA-Dock functionality. When a BC v1.2-compliant OTG-capable phone, such as Sony Xperia (Neo V, P, or S), is connected to the CY4613 board's US port, the phone is charged, and simultaneously enumerates the hub and works like a normal host controller.

1: USB On-the-Go is a USB-IF specification that requires portable devices to function as a Host when connected to devices and to function as a device when connected to a Host.



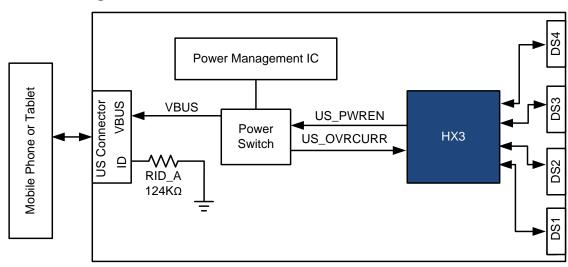


Figure 1. HX3 Controller in ACA-Dock Mode in CY4613

3. Supporting ACA-Dock Capable Phones with Proprietary RID_A Values

The CY4613 board has been tested with popular tablets and phones available in the market with proprietary RID_A values. By changing the RID_A resistor (<u>CY4613 schematics</u>: R25) value on the CY4613 board, you can connect different phones and tablets to the CY4613 board in the ACA-Dock mode.

Table 1 provides examples of phone/tablet models and which support proprietary RID_A values. Figure 2 shows the HX3 hub system in the ACA-Dock mode, with modifications required to support a proprietary RID_A.

Manufacturer	Models	RID_A Value
Google	Nexus 7 Tablet	120 kΩ
Samsung	Galaxy Note Pro Tablet 12.2	80 kΩ - 85 kΩ
Samsung	Galaxy Note 2, Note 3	71 kΩ - 74 kΩ supported in Rev04 2 CY4613
Samsung	Galaxy S3, S4 phone	71 kΩ - 74 kΩ supported in Rev04 2 CY4613

Table 1. Examples of Phones and Tablets that Support Proprietary RID_A Values

2: Refer Appendix



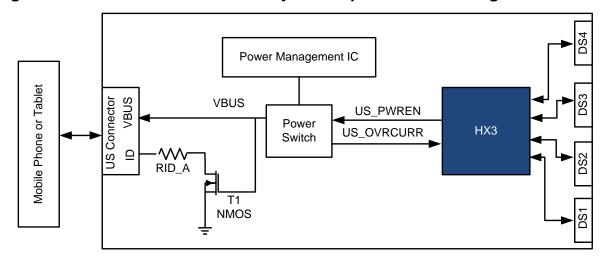


Figure 2. Recommended ACA-Dock System Implementation Using HX3 Controller

Some mobile phones or tablets (for example, Samsung Galaxy Note Pro Tablet 12.2) require the RID_A termination resistor to be floating when VBUS is powered OFF as shown in Figure 2. For this implementation, the transistor T1 (Part Number: BSN20-70 or equivalent) is required. Transistor T1 is not implemented on the CY4613 board and RID_A is directly connected to ground (as in Figure 1). However, it is highly advised to use the transistor T1 in ACA-Dock system designs.

4. HX3 and PSoC® 4-Based ACA-Dock Solution Supporting Various RID_A Values

In order to enable the ACA-Dock functionality for various phones and tablets that support either standard or proprietary RID_A resistor value, a solution which varies the value of resistor RID_A is required. This solution can be implemented by interfacing HX3 with a PSoC 4 (PSoC supporting ARM® Cortex®-M0 core and programmable mixed-signal hardware IP). Figure 3 shows the block diagram of the solution implementation; Figure 4 shows the Solution Demo Board.

Schematics and layout of the HX3 and PSoC 4-Based ACA-Dock Solution is available at http://www.cypress.com/?rid=107154. For additional information and to request a demo, contact Cypress at https://www.cypress.com/?rid=107154. For additional information and to request a demo, contact Cypress at https://www.cypress.com/?rid=107154. For additional information and to request a demo, contact Cypress at https://www.cypress.com/?rid=107154.



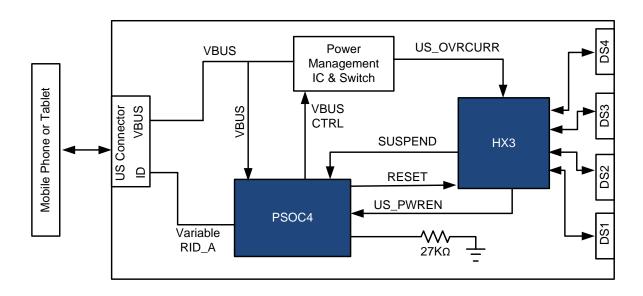


Figure 3. HX3 and PSoC 4-Based ACA-Dock Solution Block Diagram

The function and purpose of the signals shown in Figure 3 are as follows:

- 1) **SUSPEND**: The SUSPEND pin is held HIGH when HX3's US port is not connected to any host controller. The SUSPEND pin is pulled LOW only when HX3 is successfully enumerated by the host connected to the US port. PSoC 4 monitors the SUSPEND pin to determine successful enumeration. The enumeration process takes up to one second.
- 2) **ID pin of US USB Connector**: The ID pin of the US port is connected to the output of the iDAC in the PSoC 4. PSoC 4 will vary the current driven on the ID pin to emulate varying RID_A values.
- 3) **US_PWREN**: HX3 informs the PSoC 4 of the overcurrent event on the US port. PSoC 4 controls the power switch on the VBUS line.
- 4) **VBUS**: The VBUS line is usually driven to 5 V by the USB Host except in the ACA-Dock mode. The PSoC 4 is designed to monitor the VBUS line and ensure that the ACA-Dock does not drive the VBUS signal until the USB Host has stopped driving the VBUS line.

5) **RESET**: PSoC 4 has the capability to RESET the HX3.



Upstream port Downstream Port 4 LEDs to IDENTIFY RID VALUE USED TO ENABLE ACA-DOCK PSOC4A CY8C4245AXI-483 HX3 CYUSB3324-88LTXC Downstream Port 2 Downstream Port 1 Downstream Port 3

Figure 4: HX3 and PSOC 4 Based ACA-Dock Solution Demo-Board



The algorithm implemented on PSoC 4 is as follows:

Step 1:

On initial power-on or reset, PSoC 4 will ensure the power management IC and switch is OFF (VBUS driven by USB Host) and holds the variable RID_A at GND. PSoC 4 monitors the VBUS line to identify the US connect event (VBUS = 5 V). As soon as a US connect event is detected, Step 2 is initiated.

Step 2:

The PSoC 4 solution has implemented three popular RID values as default (72 k Ω , 80 k Ω , and 124 k Ω). PSoC 4 varies the current to emulate various RID_A values and monitors the SUSPEND signal. If enumeration (SUSPEND = 0) is successful for any one of these values, the PSoC 4 device locks the RID value. PSoC 4 then waits for the USB Host to stop driving VBUS (VBUS = Floating) before allowing the power management IC to drive VBUS.

If enumeration is not successful (SUSPEND = 1), Step 4 is initiated.

Note The PSoC 4 firmware can be updated to support additional RID values as required.

Step 3:

PSoC 4 monitors the voltage across the RID to identify the US disconnect event. If a disconnect event is detected, HX3 and PSoC 4 will automatically reset.

Step 4:

If the connected phone or tablet is not ACA-Dock-capable, PSoC 4 will set RID = GND (OTG Mode which supports enumeration without US charging). If enumeration (SUSPEND = 0) is successful, PSoC 4 device locks the RID value. If enumeration is not successful (SUSPEND = 1), PSoC 4 will stop driving current on the RID line and wait for a disconnection event to occur.



5. Smartphones and Tablets Proven to support ACA-Dock or OTG Mode Operation

HX3's ACA-Dock solutions (CY4613 Development Kit and HX3 and PSoC 4-based Solution) have been proven through testing by third-party testing at Allion Labs. Based on test results, the following 27 mobile devices across 9 Brands have been proven to support ACA-Dock or OTG Mode operation on HX3.

Table 2: ACA-Dock Phones Proven with HX3 (14 Models)

Brand	Device Models	# of Mobile Devices Supported
Asus	PadFone Infinity A86, Nexus 7	2
DELL	XPS 10	1
Sony	Xperia Neo V, P, and S	3
	Xperia TX LT29i, Xperia Arc	2
Samsung	Galaxy Note 2, Note 3, Note 4	
	Galaxy Note Pro Tablet 12.2	
	Galaxy S3, S4	6



Table 3: OTG Mode Phones Proven with HX3 (13 Models)

OEMs	Brand	# of Mobile Devices Supported
Asus	Zen Phone 5	1
ACER	Iconia W510-1666 Tablet	1
hTC	New One M8	1
LG	D838 (G Pro 2), Nexus 5 Optimus Pad G-Slate, T-Mobile Tablet	4
ОРРО	N1T	1
Samsung	S5 (SM-G900I)	1
Sony	Xperia Z Ultra C6802, Xperia Z2 Phone Xperia Z2 tablet	3
Zotac	Tegra Note7	1



6. Appendix:

Question: How do I identify a Rev04 CY4613 board?

Answer: The revision number is printed on the back of the CY4613 board as shown in Figure 5.

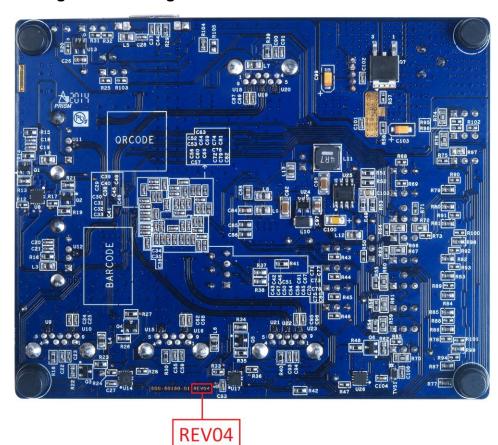


Figure 5: Marking of Revision Number on CY4613 Board



Question: How is the Rev04 CY4613 different from the previous CY4613 boards?

Answer:

Rev04 CY4613 Board:

Supports two RID_A values: 124 k Ω and 73.2 k Ω

RID_A selection jumper (J27) is a 3-pin jumper

The RID_A can be set to 124 k Ω by setting jumper J27 to connect Pin 1 and Pin 2.

The RID_A can be set to 73.2 k Ω by setting jumper J27 to connect Pin 2 and Pin 3.

Earlier versions of CY4613 Board:

Supports RID_A value of 124 $k\Omega$

RID_A selection jumper (J27) is a 2-pin jumper.

RIA_A can be set to 124 k Ω by setting jumper J27 to connect Pin 1 and Pin 2.



1) Related Categories:

Keywords: HX3, ACA-Dock, ACA Dock, ACAdock, upstream charging, Battery charging, BC V1.2, SmartPhone charging, Smart phone charging, Tablet charging

Product Family: USB Super Speed Hubs

Related Tags: [Select the Tags by clicking the checkbox associated to the Tags]

Clocks & Buffers Tags

☐ Adapter	Algorithm	Bitmap	Buffer	☐ Bypass	☐ CLKMAKER
☐ CML	☐ CY3670	☐ CY3672	☐ CY3675	☐ CY36800	☐ Cascade
☐ Charge Pump	☐ Clock Tree	Clocks	☐ Clocks and Buffers	☐ ComLink	☐ Crystal Oscillators
☐ CyClock	☐ CyClockWizard	☐ CyberClocks	☐ CyberClocks Online	☐ Cycle to Cycle	DCXO
☐ Delay	☐ Deterministic Jitter	☐ Differential	Divider	☐ Duty Cycle	☐ EMI
☐ Enhanced Performance	☐ Ent	☐ Entrant	☐ FNOM	☐ Factory	☐ Failsafe
☐ Fanout	☐ FastEdge	☐ Feedback	Field	Flexo	Frequency
☐ Frequency Margining	☐ Function Select	Generators	☐ Ground Bounce	HPB	□HSTL
☐ Hershey Kiss	☐ I2C	☐ IBIS Model	☐ Impedance	☐ Input	☐ InstaClock
☐ Inverted	☐ Jed	☐ Jedec	Jitter	LVCMOS	LVDS
LVPECL	Layout	Lexmark Profile	☐ Loop Bandwidth	☐ MoBL	☐ Modulation Rate
Multiplier	□NZDB	☐ Non-Volatile Memory	□ОТР	☐ Offset	☐ Oscillator
Output	☐ Overvoltage	☐ PCI Express	☐ PLL	☐ PPM	☐ PREMIS
Period	☐ Phase	☐ Phase Noise	☐ Power Supply Noise	☐ Program	☐ Programmable
☐ Propagation	☐ Pullability	RMS	Rambus	Random Jitter	Reference
Rise Fall Time	RoboClock	☐ Schematic	☐ Serial	☐ Signal Integrity	Skew
Socket	☐ Specialty Clocks	☐ Spread %	☐ Spread Aware	☐ Spread Profile	☐ Spread Spectrum
Synthesizer	TCXO	☐ TIE	☐ Termination	☐ Thermal	Translator
Undervoltage	UniClock	☐ Unit Interval	□ vco	□ vcxo	☐ Volatile Memory
☐ Voltage Droop	□xcg	□ XDR	□xo	☐ Xtal	□ZDB



Zepto													
Lighting & Power Co	ontro	l Tags											
	D			. Da sudatas		2004			\ 7				
		egulator		Regulator	CY3			CY326	07	CY3268			
	olor Mi			ent Sense	DAL			DMX	-1	FN Pins			
		ic Controller		SFETs	MPF		Latara	Modul	ators	PrISM	D l. (
☐ Programming ☐ SS	SDM		☐ Sch	ematics	☐ SWI	tching Regi	ulators	☐ Trip		□ Voltage	Regulator		
Wireless/RF Tags													
☐ 2.4 GHz		☐ 8DR		Antenna		☐ Audio				gileHID		☐ Bridg	 je
CY3271		☐ CY3630		☐ CY4636		☐ CY467	72		CYFI			CYF	ISNP
CYRF6936		☐ CYRF79	36	Channel		☐ DDR			☐ DSSS			GFS	K
HID		HUB		□IRQ		☐ Interfe	rence A	voidance	dance			Link	Budget
Mouse		□ Node		☐ PMU		☐ PN Cc	de		☐ PRoC			☐ PRo	C-CS
☐ PRoC-EMB		☐ PRoC-T	Т	☐ PRoC-USB		☐ PRoC	-UI	□ P		wer Amplifie	er	☐ Prea	ımble
☐ Pseudo Noise code		□RF		RSSI		Range)	Rer		mote		SCD	,
SDR		SOP		SPIM		☐ Star-N	letwork	Protocol	tocol Streaming			☐ Trac	kpad
Wireless		☐ Wireless	USB [☐ Wireless \	JSB LP	☐ Wirele	ss USB	LS	☐ Wi	reless USB	LR	☐ Wire	less USB NL
☐ Wireless Capacitive T	ouch												
		•											
Memory Tags													
													Ī
Address Bus	☐ A	sync	☐ Auto	motive		Autos	tore		BH	IE / BLE	BUSY		
☐ Battery Backup		☐ Burst ☐ Bus Contention		☐ Clock				PR	☐ Data Bu	IS			
☐ Data Integrity	☐ Data Retention ☐ Data		☐ Data	Datasheet		☐ Dual F	Port			ho Clocks	☐ FIFO		
☐ FPGA	F	lags	Flow	through		☐ Fullfle	Х		FR	AM	HOLD		
☐ HD-FIFO	☐ HSB ☐ I2C				□INT			☐ Im Match	pedance ing	☐ Interfac	e		



☐ Interleaving	☐ JTAG ☐ □ S	TAG		MSL	Migration Path
MoBL	☐ Models ☐ N	NoBL	ODT	☐ Obsolete ☐	PCB
☐ PLL / DLL	☐ Packaging ☐ F	Parallel	☐ Parity	☐ Part Decoder ☐	Part Difference
☐ Password Protection	Configuration	Pipeline	☐ Power Consumption	Power On State	Processor
□QDR	Qualification Reports	Quality	RECALL	RTC	Race Condition
Read	☐ SER ☐ S	SPCM	SPI	SRAM	Serial
☐ Signal Integrity	☐ Sync ☐ ☐	Technology	☐ Termination	☐ Timing ☐	☐ Vcap
□ Vddq	☐ Voltage Levels ☐ \	/ref	☐ Width / DepthExpansion	Write	nvSRAM
uPower					
Interface Tags					
☐ 10B/8B Decoder	3 Level Inputs	ALDEC	☐ ATM	☐ Altera	BIST
BSDL	Biasing	CDR	CML	☐ CPLD	☐ CY3900i
☐ CY3950i	CYUSBISRPC	☐ Cable	☐ Cable Driver	☐ Channel Bonding	☐ Clock Multiplier
☐ Clocking Modes	☐ Coaxial Cable	☐ Copper Cable	☐ Coupling	☐ Crystal	☐ Current
☐ DVB	☐ Data Character	☐ Data rate	☐ Delta39K	☐ Deserialize	☐ Deserializer
☐ Dual Channel	☐ EPLD	⊠ EPROM	☐ ESCON	☐ Elasticity Buffer	☐ Equalizer
☐ Error	☐ Evaluation Board	☐ FPGA	☐ Fiber Optics	☐ Flash370i	Framer
☐ Framing Character	☐ Framing Mode	☐ Gigabit Ethernet	Hex	☐ High Speed Serial Link	ks Hotlink
Hotlinkl	☐ HotlinkII	□IP	☐ Isr	☐ Jtag	☐ LFI
LVTTL	☐ Logic Level	☐ Loop Back	☐ Macrocell	☐ Max340	☐ Model
☐ Non-Volatile	OC-1	☐ OC-2	☐ OC-3	☐ Operating System	☐ PAL
☐ PECL	☐ PLD	☐ PLL	☐ Parallel Input	☐ Parallel Output	☐ Parity
☐ Phase Align Buffer	☐ PoF	☐ Point To Multi Point	☐ Point To Point	☐ Power Supply	□ Programming
Quad Channel	☐ Quantum38K	Receiver	☐ Recovered Clock	☐ Redundant Outputs	☐ Reference Clock
Report File	Reprogrammable	SMA	SMPTE	☐ SMPTE-259M	☐ SMPTE-292M
SONET	SPICE	SPLD	STAPL	SVF	Serial Input
☐ Serial Output	Serializer	Simulator	Size	☐ Special Character	☐ Specification
ПТТІ	☐ Temperature	☐ Third Party Tool	☐ Transceiver	☐ Transmitter	☐ USBISRPC Cable

13



☐ Ultra37K	User Guide	□VHDL	Verilog	□ Voltage	□ Warp
☐ Word Sync Sequence			-	_	
PSoC 1 Tags		·			
☐ ADC	ADCINC	☐ Analog	☐ Analog Bus	☐ API	☐ Assembly Language
☐ Boot.asm	☐ Bootloader	☐ BSDL Files	☐ Build Errors	☐ Calibration	☐ Capsense
☐ Clock	☐ Clock Synchronization	☐ Cloning	☐ Column Clock	☐ Communication	☐ Comparator
☐ Compiler	☐ Counter	☐ CPU Speed	☐ Crystal	☐ CT Block	☐ DAC
☐ Debugging	☐ Decimator	☐ Delta Sigma ADC	☐ Development K	it Digital	☐ Dynamic Reconfiguration
☐ ECO	☐ EEPROM	☐ Errata	Filter	☐ Flash	☐ Flash Security
☐ Global Resources	☐ GPIO	☐ Hex File	☐ I2C	☐ I2C-USB Bridge	☐ ICE Cube
☐ Installation	☐ Internet Explorer	☐ Interrupt	☐ ISR	☐ ISSP	☐ Large Memory Model
LCD	License	☐ MAC	☐ MiniProg1	☐ MiniProg3	☐ Mux
☐ Mux Bus	OCD	☐ Offset	☐ Pod	☐ Port and Pins	☐ Power Management
☐ Production Programmer	☐ PWM	☐ RAM	RTC	□SAR	☐ SC Block
SMP	☐ SPI	System Level Design	☐ Timer	☐ UART	USB
☐ USBUART	☐ Watchdog	☐ Amplifier UM	☐ Analog Referen	ce Analog UM	☐ Build Tools
☐ Communication UM	☐ CRC UM	CYFI	☐ Device Programming	☐ Digital UM	☐ DTMF
☐ Fan Controller UM	☐ Firmware UM	☐ FMEA	☐ Port Expander	☐ PSoC Power System Architecture	□Voltage Sequencer UM
PSoC 3/4/5 Tags					
Component Tags					
☐ Analog Hardware Mux	☐ Analog Mux	☐ Boost Converter	☐ Bootloader / Bootloadable	☐ CAN	☐ CapSense_CSD
☐ Character LCD	Clock	☐ Comparator	Control / Status	☐ Counter	□CRC



☐ DAC	☐ Debouncer	☐ Delta Sigma ADC	☐ DFB	☐ DFB Assembler	☐ Die Temperature
☐ Digital Comparator	☐ Digital Multiplexer	☐ DMA	☐ EEPROM	emFile SPI Mode	☐ EMIF
☐ Ezl2C Slave	☐ Fan Controller	Filter	☐ Frequency Divider	☐ Glitch Filter	Global Signal Reference
☐ Graphic LCD	☐ I2C /I 2S	□iAP	☐ Interrupt	LIN	☐ Logic Gates
☐ Lookup Table	☐ Manual Routing	☐ MDIO	Mixer	☐ Opamp	□PGA
Ports and Pins	☐ Power Monitor	☐ PRS	☐ PWM	Quadrature Decoder	Resistive Touch
RTC	☐ RTD Calculator	☐ Sample / Track and Hold	☐ SAR ADC	☐ SAR Sequencer	☐ Segment LCD
☐ SGPIO	☐ Shift Register	☐ Sleep Timer	☐ SM / PMBus	SPDIF	☐ SPI
Sync	☐ Thermistor Calculator	☐ Thermocouple Calculator	□TIA	☐ Timer	☐ TMP05 Interface
TrimMargin	□UART	□ UDBClkEn	USBFS	USBMIDI	USBUART (CDC Interface)
☐ Voltage Fault Detector	☐ Voltage Sequencer	☐ Vref	☐ WaveDAC		
General Tags					
☐ Analog Bus	☐ Analog Global Bus	☐ Analog Mux Bus	☐ API	☐ Application Specific	☐ Assembly Language
☐ Bootloader Host	☐ Boundary Scan / BSDL	☐ Bridge Control Panel	☐ Build Settings	Clock	☐ Compiler - GCC
Compiler - KEIL	☐ Compiler - MDK	☐ Compiler - RVDS	☐ Cortex-M0	☐ Cortex-M3	☐ Creator Registration
Custom Component Interconnect	☐ Datapath Configuration Tool	☐ Debugging	☐ DMA Wizard	□ DVK	□ ECO
☐ Errata	☐ Error Message	☐ Flash	☐ Hex File	☐ Installation	☐ ISSP / HSSP
☐ KEIL Registration	Linux Platform	☐ Low Power Modes	☐ LVD / HVD	☐ MFi	☐ MiniProg3
Optimization	☐ Programmer COM	☐ PSoC Creator	☐ PSoC Programmer	Reset	RTOS
Schematic	Silicon	Software Download	□STA	☐ Supply Voltage	System Reference Guide
☐ Verilog	☐ Watchdog	☐ Windows Platform			
Kit Tags					
☐ CAN / LIN EBK	☐ CapSense Expansion EBK	CY8CKIT-001 Kit	CY8CKIT-030 / 050 Kit	CY8CKIT-042 Kit	☐ Digital Audio EBK
☐ First Touch Kit	LCD Segment Drive EBK	☐ MFI EBK	☐ Power Supervisor EBK	PSoC 3/4/5 Processor Module	☐ Thermal Management EBK



Touch Sensing Tags

ADC	☐ Air gap	☐ Backlighting	☐ Bleeder Resistor	Bootloader	CMOD
☐ CSA	CSD	☐ CSD Parameters	☐ CSD2X	☐ CSDADC	☐ CSDAUTO
☐ CY3203A	☐ CY3213A	☐ CY3214	☐ CY3218	☐ CY3280-20x34	☐ CY3280-20xx6
☐ CY3280-21x34	☐ CY8C20x34	CY8C20xx6	☐ CY8C21x34	CY8C21xxx-CapSense Express	☐ CY8C24x94
☐ CY8CMBR2044	☐ CapSense Express	☐ Circuit Housing	☐ Conductive Objects	☐ Configuration	☐ Diplexing
Dynamic Reconfiguration	☐ EEPROM	□ ЕМІ	ESD	☐ Errors	☐ FR4
Filters	☐ Finger Threshold	☐ Flex PCB	☐ I2C	☐ I2C-USB Bridge	□IDAC
☐ IMO and Prescaler	□ ІТО	☐ Layout Guidelines	☐ Metal	□ Noise	Overlay
☐ PSoC3 CapSense	☐ Parasitic Capacitance	☐ Pathfinder	☐ Power Consumption	☐ Proximity	SNR
☐ SPI	☐ Scanning Techniques	Schematic	Sensors	Shield	Sliders
☐ SmartSense	☐ Tuning	UART	☐ Water	☐ Water Proofing	

USB Controllers Tags

☐ 8051	☐ AN2131	☐ AT2LP	ATA / ATAPI	ATA Commands	☐ Asynchronous
☐ Auto Mode	☐ Bandwidth	☐ Blaster	☐ Bulk Transfer	☐ Bus Power	☐ C#
☐ C++	☐ CAT5	☐ CF Card	☐ CY3216	☐ CY3649	☐ CY3654
☐ CY3655	☐ CY3660	☐ CY3662	☐ CY3664	☐ CY3674	☐ CY3681
☐ CY3684	☐ CY3685	☐ CY3686	☐ CY4605	☐ CY4606	☐ CY4611B
☐ CY4615	□ CYUSB	Clock	☐ Compliance	☐ Control Center	☐ Control Transfer
☐ Crystal	☐ CyConsole	☐ DLL	☐ Debug	Descriptors	Driver
☐ EEPROM	☐ EZ-HOST	☐ EZ-OTG	☑ EZ-USB	☐ Emulation	☐ EnCoreII
☐ EnCoreIII	☐ EnCoreV	☐ Encore	☐ Endpoint	☐ Enumeration	☐ Errata
☐ FIFO	□FX	☐ FX1	☐ FX2	☐ FX2LP	Firmware
☐ Firmware Debug	☐ Flags	Framework	☐ Full Speed	☐ GPIF	HDD



HID	☐ HX2	☐ HX2LP	☐ Hi-Lo Programmer	☐ High Speed	☐ Host Application
⊠ Hub	☐ I2C	☐ ICE	☐ IN Transfer	☐ Interrupt Transfer	☐ Interrupts
☐ Isochronous Transfer	☐ Keil	☐ Keyboard	☐ Layout	Library	Loader
☐ Low Speed	☐ M8A		☐ Manual Mode	☐ Mass Storage	☐ Memory
Mouse	□ NX2LP	☐ NX2LP-Flex	☐ Nand Flash	☐ Nand Manufacturing Utility	OTP
OUT Transfer	☐ Port IO	Register	Renumeration	Report	□ Reset
SFR	SIE	☐ SL811HS	SPI	☐ SX2	
	Screamer	☐ Script	☐ Self Power	☐ Slave FIFO	Streaming
SuiteUSB	Synchronous	☐ TX2	☐ TX2UL	☐ Tetra Hub	☐ Throughput
Timer	UART	□UDMA	USBFS	USBUART	USBSerial
☐ Vendor Command	☐ Video Class	WHQL	□WLK	☐ cyapi	uVision
SuperSpeed					
☐ FX3	ADMux	☐ ARM926EJ -S	☐ Bootloader	☐ DMA	☐ Eclipse
☐ FX3 GPIO	☐ FX3 Power Management	☐ FX3 Power supply	☐ FX3 SDK	☐ GPIF II	☐ HS-OTG
☐JTAG	☐ LPP	☐ MSC	☐ Oscillator	RTOS	☐ SD Card
Slavefifo	☑ USB 3.0	USB Compliance Test	USB Host	UVC	
☐ FX3S	☐ eMMC	SDIO	☐ S-Ports	☐ Bay	☐ Benicia
⊠ HX3	□ ASSP	□ Battery charging	☐ Bootloader	☐ Cortex-M0	☐ EEPROM
GPIOs	☐ HX3 Power Management		⊠ I2C	☐ In-system programming	Oscillator
☐ USB 3.0 hub	☐ USB Shared Link™				



Knowledge Base Article Type: [Select the category by clicking the checkbox associated]

KB Type-1	KB Type-2			
	ByteCraft			
Committee	☐ Imagecraft			
Compiler	☐ Keil			
	HiTech			
	☐ Training/Things you should know			
	Component Architecture			
	☐ Component/Project management			
Component Dovelopment	□ Datapath			
Component Development	☐ Analog components			
	☐ Digital components			
	☐ Component software/tools			
	☐ Component Testing			
☐ Development Kits	☐ FirstTouch Kit			
☐ Development Tools				
Device Drivers	☐ Pullability			
Device Drivers	☐ Mass Storage			
Device Programming	☐ PSoC Programmer			
□ Documentation				
□ General				
	☐ Digital			
	☐ Specifications			
	☐ Analog			
☐ Known Problems and Solutions				
	□ 8051			
Microcontrollers	☐ M8			
	☐ M8C			
Modules				



☐ Platforms	☐ MacOS X
	Windows
Dreteeds	□ HID
Protocols	⊠ I2C
Quality	
☐ Reference Designs	
Software	☐ PSoC Designer
	☐ PSoC Creator
□ Hear Madulas	☐ Analog
User Modules	☐ Digital



DOCUMENT HISTORY

Document Title: Supporting ACA-Dock Feature in Smartphone and Tablet Docks with HX3 USB 3.0 Hub Controller – KBA96321

Document Number: 001-96321

Rev.	ECN No.	Orig. of Change	Description of Change
**	4657458	RAJM	Created new KBA.

Distribution: WEB Posting: None