AN60631

PSoC® 3 and PSoC 5LP Clocking Resources

Author: Max Kingsbury
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Associated Part Family: All PSoC® 3 and PSoC 5LP Parts
Software Version: PSoC® Creator™ 2.1 SP1 or higher
Related Application Notes: AN54439, AN80248

AN60631 covers PSoC® 3 and PSoC 5LP's highly versatile and reconfigurable clocking system. This application note describes PSoC 3 and PSoC 5LP's oscillators and clock sources, phase-locked loop (PLL), and clock distribution network. However, it does not cover the details of the external crystal oscillators (ECOs). For those details, see AN54439 - PSoC® 3 and PSoC 5LP External Crystal Oscillator.

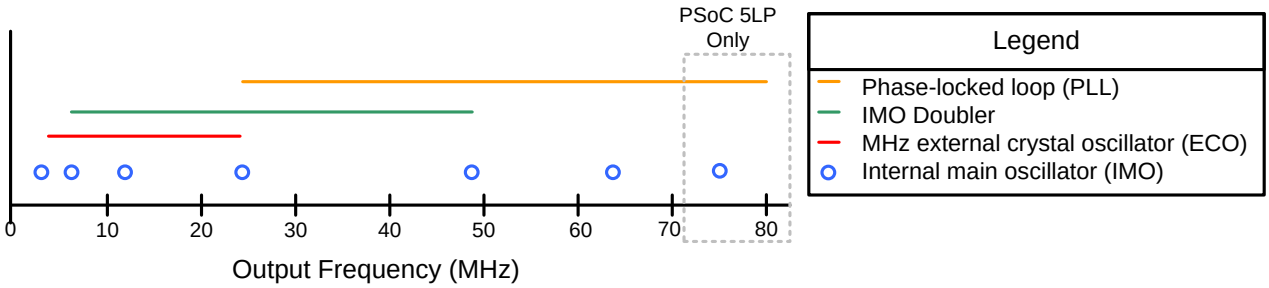
Introduction

Clocks play a critical part in microcontroller operation. They are used to synchronize internal signals, ensure error-free communication with other digital devices, and drive the conversion of signals to and from the analog domain. These roles make the configuration of the different clocks used inside of a microcontroller very important.

Clock Sources

PSoC 3 and PSoC 5LP contain many clock sources that vary in frequency and accuracy. This section describes each potential clock source in detail. Figure 1 shows the clock source options in the MHz range.

Figure 1. PSoC 3 and PSoC 5LP Clock Source Options in the MHz Range



Note All clock source frequencies are not available in all parts.

Internal Main Oscillator (IMO)

The IMO is PSoC 3 and PSoC 5LP's main clock source. It is trimmed at the factory for operation at 3, 6, 12, 24, 48, 62, and 74 MHz. Some frequencies are unavailable in certain devices. The IMO has higher accuracy at lower operating frequency. It has a built-in doubler to allow the generation of a new clock signal at twice the frequency of the input. This input can come from the IMO itself, or from an external source, such as the MHz ECO.

Note The IMO doubler should be used with caution, as its output can have frequency inaccuracy and duty cycle distortion, even when it is sourced with a high accuracy input.

The IMO's accuracy can be improved by trimming at run-time, as documented in AN80248.

Phase-Locked Loop (PLL)

The PLL allows designers to generate a clock signal from the existing clocks in the system. It produces an output frequency equal to the input frequency multiplied by the ratio P/Q, where P can range from 4 to 256, and Q can range from 1 to 16. The gain range is therefore 0.25 to 256 times the input frequency.

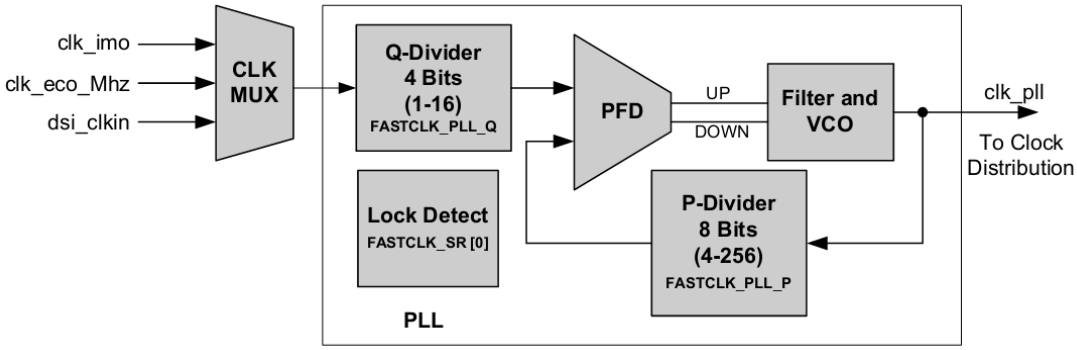
The PLL uses a voltage-controlled oscillator (VCO) to generate the new output clock. This clock is divided by P, and compared to the input clock divided by Q by the phase frequency detector (PFD). The PFD output is filtered, and used to trim the VCO. This achieves an output

clock that is equal in frequency to the input clock multiplied by P and divided by Q. This topology is shown in Figure 2.

The PLL input, output, and intermediate frequencies are limited to certain ranges. The PLL can generate frequencies between 24 and 80 MHz, given an input clock between 1 and 48 MHz. The intermediate signal, equal to the input frequency divided by Q, must be between 1 and 3 MHz.

Note The exact limitations on the input, output, and intermediate frequency of the PLL vary between parts, and may be found in the applicable device datasheet.

Figure 2. PSoC 3 and PSoC 5LP PLL Topology



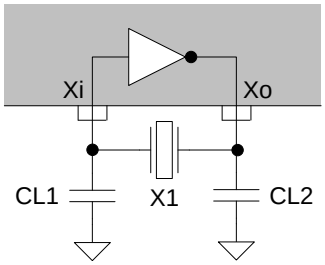
The PLL introduces no frequency inaccuracy, and consumes less power at a given output frequency than the IMO. Thus, when a clock is desired within the operational range of the PLL, it is recommended that the IMO be run at the minimum speed of 3 MHz, and the PLL be used to generate the desired output frequency. The resulting PLL output clock will be within the accuracy specification percentages of the input clock.

The PLL may be configured during design time using PSoC Creator's "Clocks" design wide resources tab. The PLL may be reconfigured at runtime using register writes or the provided API. PLL reconfiguration APIs are provided by PSoC Creator in all PSoC 3 and PSoC 5LP projects. These APIs are documented in the System Reference Guide.

MHz-range ECO

The MHz ECO contains an internal Pierce Oscillator circuit that can be used with an external crystal or ceramic resonator to generate frequencies within its operating range of 4-25 MHz. This circuitry is shown in Figure 3. ECOs typically offer much more accurate clock frequency generation than built-in oscillators. The accuracy of the ECO is determined by the specifications of the crystal or resonator used, along with its loading capacitors. Typical MHz resonator accuracies range in the tens of parts per million (PPM). The MHz ECO in particular is especially useful for high-speed communication where clock accuracy is critical, such as in CAN or I^2S communication, or digital audio reproduction.

Figure 3. PSoC 3 and PSoC 5LP ECO Topology



32.768-kHz ECO

The 32.768 kHz ECO contains an internal Pierce Oscillator circuit that can be used with an external crystal resonator to generate a 32.768 kHz clock signal. The kHz ECO has a dedicated 15-bit counter may be used to derive a once per second interrupt. The kHz ECO is especially useful for accurate timekeeping using PSoC 3 and PSoC 5LP's real-time clock (RTC).

Note AN54439 - PSoC® 3 and PSoC 5LP External Crystal Oscillators further explains usage of the MHz and kHz ECOs.

Internal Low-Speed Oscillator (ILO)

The ILO is a low-speed, low-power clock source that is used to time system resources such as the watchdog timer and fixed function counters. The ILO actually contains two clock-generation sources, operating at 1 kHz and 100 kHz nominally. The ILO also contains a divide by 3 block that can be used to generate a 33 kHz output from the 100 kHz source. This 33 kHz output is useful for comparison to a 32-kHz crystal output.

The ILO is not as accurate as the IMO, and should not be used for precise timekeeping. Its accuracy can be found in the device datasheet, and is roughly -50%/+100% using the factory trim. However, the ILO has very low current consumption, which makes it an ideal choice for systems that sleep and periodically wake up.

The ILO's accuracy can be improved by trimming at run-time, as documented in AN80248.

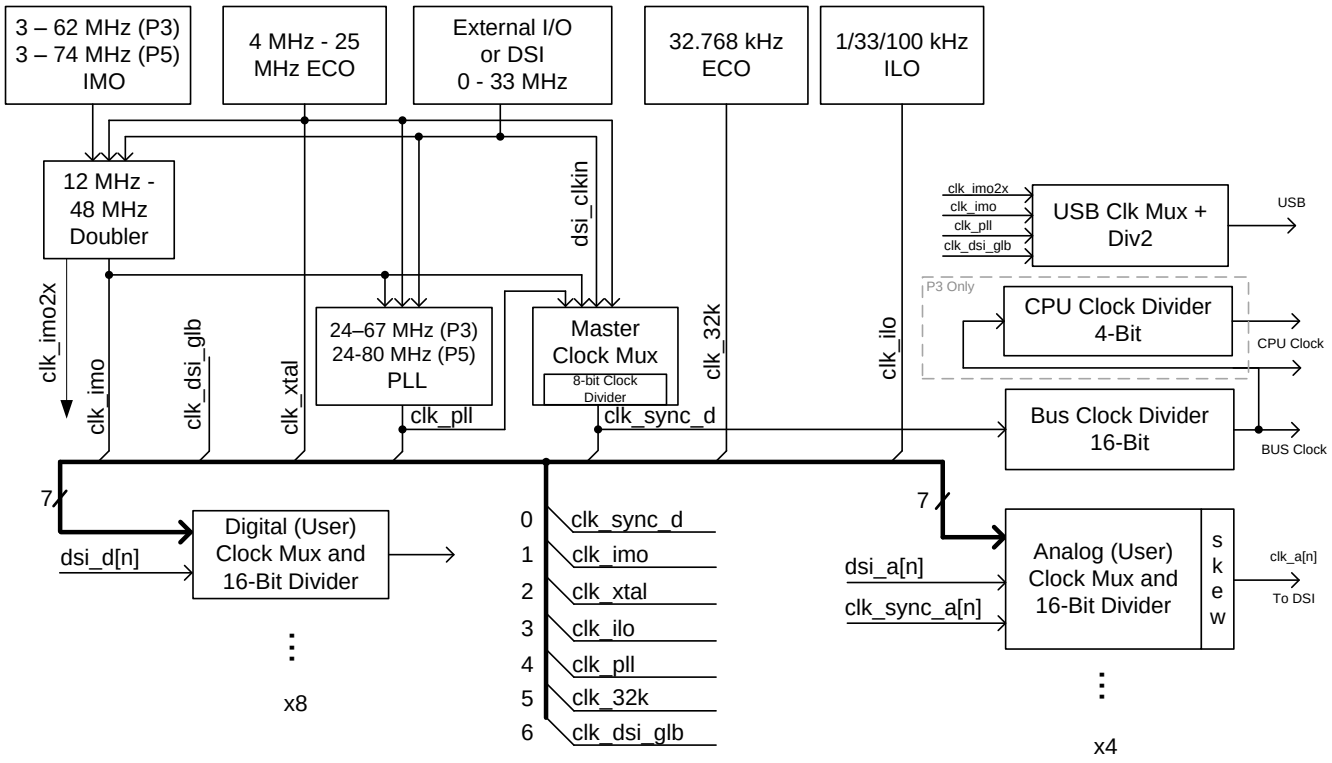
USB Clock

PSoC 3 and PSoC 5LP's clocking architecture allows the device to automatically trim the IMO to the USB traffic from an attached host. This feature allows the PSoC 3 or PSoC 5LP to achieve a USB accurate clock using only the IMO and USB traffic with a host as a reference. This accuracy is achieved by adjusting the IMO's trim setting after measuring the IMO frequency, using host USB start of frame events as a timing reference.

Clocking Tree

PSoC 3 and PSoC 5LP's clocks can be understood in the context of the clock tree. The clock tree divides down and distributes clock signals in the part. PSoC 3 and PSoC 5LP's clock propagation is shown in Figure 4.

Figure 4. PSoC 3 and PSoC 5LP Clock Propagation Diagram



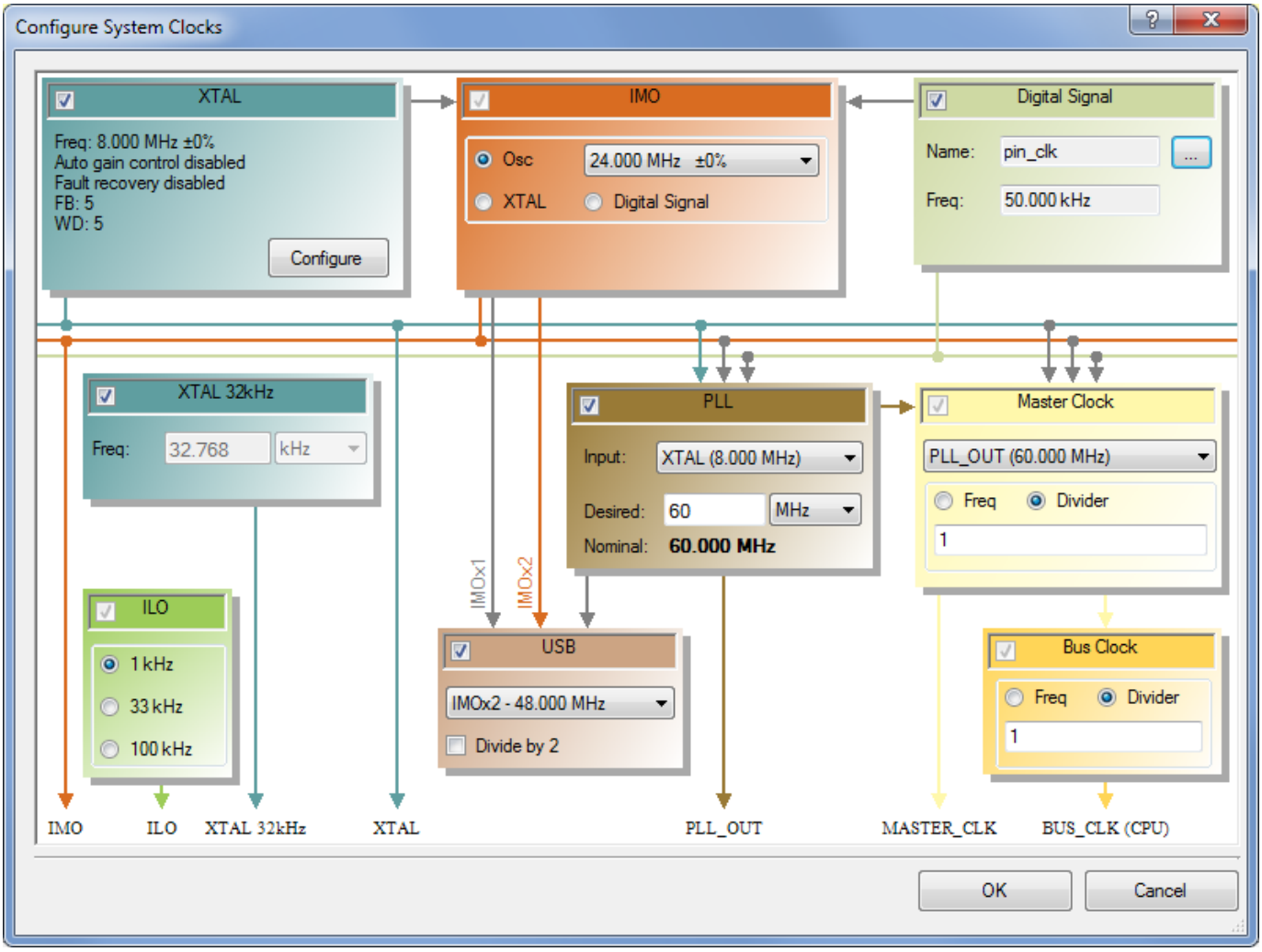
As shown at the bottom of Figure 4, there are seven clock nets that make up the PSoC 3 and PSoC 5LP primary clock routing system. These clock signals are distributed throughout the part on a 7 net bus. They may be used as the source for all 12 user clocks. The master clock, or "clk_sync_d", is used to synchronize all clocks in the system. The bus clock is always an integer division of the master clock, and is synchronized to the master clock. All peripheral clocks must operate at or below the bus clock's frequency.

PSoC Creator also contains a representation of the PSoC 3 and PSoC 5LP clocking tree. It is shown in Figure 5. This dialog box can be viewed by opening the design wide resources, selecting the "clocks" tab, and configuring any of the system clocks, by clicking the "Edit Clock…" button, or by double-clicking any of the clocks. This diagram does not show the configuration of the user clocks.

PSoC 3's 8051 CPU operates on a clock derived from the bus clock. The CPU has an internal 4 bit divider that may be used to reduce the bus clock by up to a factor of 16. This divider is controlled by the SFR_USER_CPUCLK_DIV register.

PSoC 5LP's Cortex M3 CPU operates directly on the bus clock. It does not have a CPU clock divider.

Figure 5. PSoC Creator “Configure System Clocks” Dialog



PSoC 3 and PSoC 5LP Digital Signal Interconnect (DSI), User Clocks, and System Clocks

The digital signal interconnect (DSI) is a system that allows digital signals to be routed throughout PSoC 3 and PSoC 5LP. PSoC 3 and PSoC 5LP have three varieties of configurable DSI clocks. There are two “System” DSI clocks that are used for internal purposes. There are also 12 “User” clocks that can be used in PSoC 3 and PSoC 5LP’s analog and digital peripherals. Both of the system clocks are signals from the DSI system, and their outputs are used within the clocking system. The user DSI clocks come from either the DSI or the system clock bus, and are distributed throughout the chip along with the other DSI signals.

The clocking system contains a single clock input from the DSI system that is unique among DSI signals in that it may be used as an input to the PLL, master clock mux, and IMO doubler. It is shown as “dsi_clkin” in Figure 4. It is also shown in Figure 5 as “Digital Signal.”

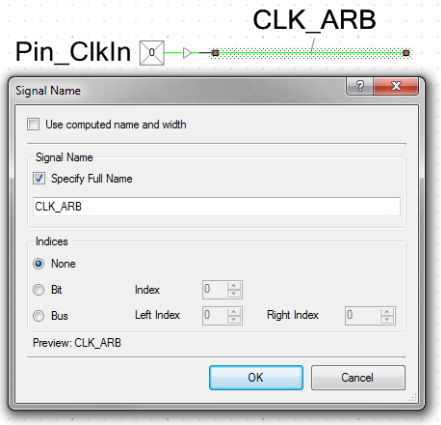
PSoC 3 and PSoC 5LP also have a single-system DSI clock that is distributed on the clocks bus along with the master clock, IMO clock, and other clock sources. It is shown as “clk_dsi” in Figure 4.

Finally, PSoC 3 and PSoC 5LP contain user clocks, which may be generated from digital signals in the part. These user clocks are routed along with the non-clock DSI signals throughout PSoC 3 and PSoC 5LP’s digital and analog resources. They are shown in the lower left and lower right of Figure 4. They are not shown in Figure 5.

Using a DSI Signal as a Clock Input

All of the DSI clocks in PSoC 3 and PSoC 5LP may be sourced from arbitrary DSI signals. To use digital signals as clock sources in the DSI, they should be named in the PSoC Creator schematic interface. This is accomplished by right-clicking the wire, selecting “Edit Name and Width”, and entering the desired name. This is shown in Figure 6.

Figure 6. Setting a Signal Name in PSoC Creator

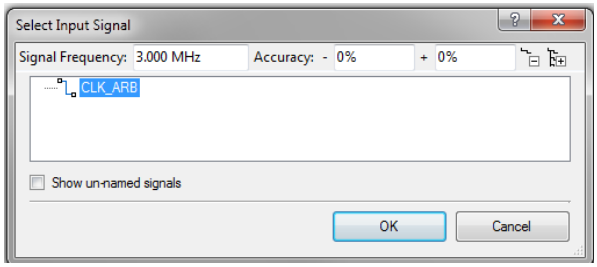


Note When using a pin input as the master clock, it should be ensured that the pin input is not synchronized. This is shown in Figure 10.

DSI System Clocks

The “dsi_clkin” may be configured using PSoC Creator in the “Configure System Clocks” dialog. After a signal has been assigned a name in the schematic, the user may go to the clocks tab of the design wide resources, click on the “…” button in the “Digital Signal” block (shown in the upper-right of Figure 5). Then select the signal name of the source of the clock. This dialog is shown in Figure 7.

Figure 7. Setting the Design Wide Clock’s Source



At this point, “dsi_clkin” may be used as the source of the PLL or master clock, in addition to the user clocks. This may be carried out using the “Configure System Clocks” dialog in PSoC Creator.

On the other hand, the “clk_dsi” signal requires no manual configuration to be used in PSoC Creator projects. If needed in a project, it will be configured behind the scenes by the IDE. Besides direct register writes, there is no way for the user to configure it.

Analog and Digital User Clocks

There are 12 “user clocks” that are distributed throughout the part. They are divided into 8 digital and 4 analog clocks. These two domains differ in their distribution about the chip, and their generation options. The analog clocks can be skewed to improve performance of sampled analog peripherals, but the digital clocks cannot. The hardware for the generation of digital and analog user clocks is shown in Figure 8 and Figure 9.

Figure 8. Digital User Clock Generation

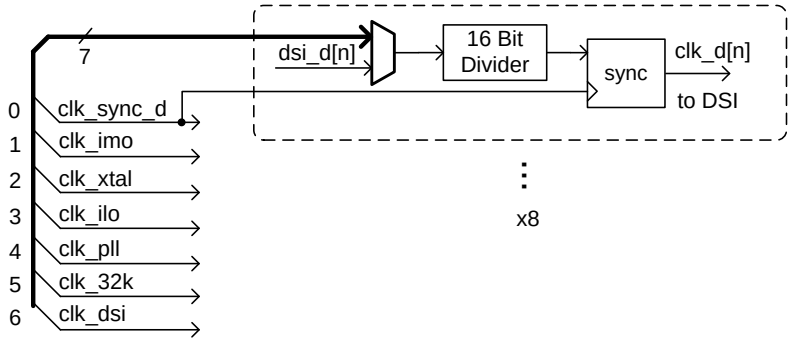
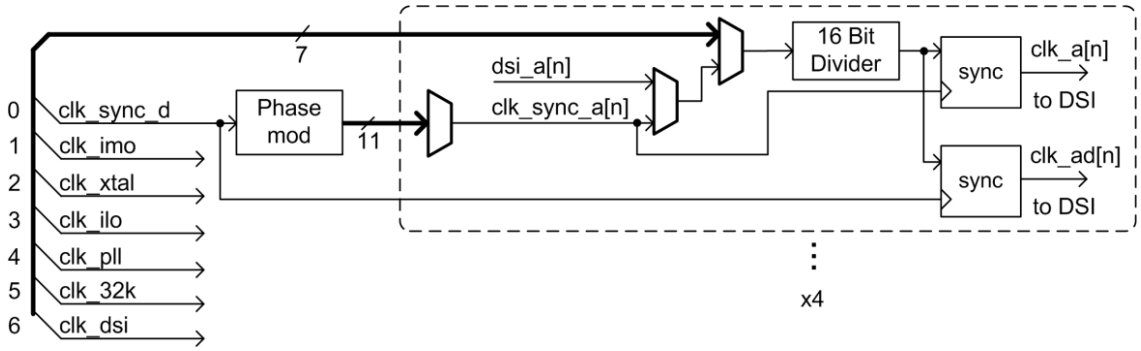


Figure 9. Analog User Clock Generation



Each user clock contains a dedicated input mux and a 16-bit divider. User clocks may be resynchronized with the master clock after division, if desired. Analog user clocks may also be resynchronized with a phase-shifted version of the master clock.

The input options for user clocks can be seen in Figure 8 and Figure 9. They include all 7 signals normally carried on the clock bus, as well as dedicated DSI signals. These dedicated signals include one dedicated DSI signal for each user clock, and one dedicated phase-shifted version of the master clock for each analog user clock.

There are three ways to create user clocks:

- In the design wide resources by clicking the “Add Design-Wide Clock” button. This action will always consume a user clock resource.
- In the schematic, the user may place a clock from the Component Catalog menu. The clock can be found in the “Cypress” tab in the “System” section. If the clock component’s configuration uses the “New” option, then it consumes a user clock resource. If it uses the “Existing” option, then it does not consume a user clock resource.
- User clocks may also be consumed by components that create their own internal clocks, such as ADCs and UARTs.

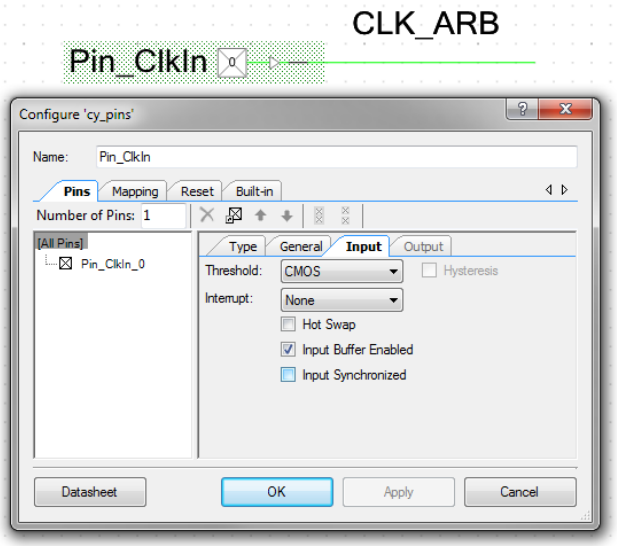
Note See the Clock component datasheet for more information about user clocks.

Note Depending upon its configuration, the PSoC 3 and PSoC 5LP user clock system may suppress the initial two to four clock edges of a signal. This issue can be avoided by “priming” the clock tree with an arbitrary waveform. See the PSoC 3 and PSoC 5LP TRMs for more details.

Clocks and I/O

Clock signals can be derived from inputs at the PSoC 3 and PSoC 5LP I/O pins. These inputs can be used as the main system clock, or simply as clocks in the PSoC Creator schematic. DSI clocks may be derived from I/O signals using the same steps shown in section Using a DSI Signal as a Clock Input. If the pin input is to be used as the master clock, the input should be unsynchronized, as shown in Figure 10.

Figure 10. Generating a PSoC 3 or PSoC 5LP Clock from an I/O



Clocks may be routed out of the part using a nearly identical method. This can be useful if external active components have less accurate clock sources than PSoC 3 or PSoC 5LP, or their behavior should be synchronized with that of PSoC 3 or PSoC 5LP's resources, or for debugging.

Note PSoC 3 and PSoC 5LP's I/Os have maximum input and output frequency ratings, which are given in the device datasheet. The output minimum frequency is always 0 Hz, and the output maximum frequency ranges from 3.5 to 33 MHz depending upon drive mode and supply voltage settings.

Inputs and outputs to the PSoC 3 may be synchronized to the master clock. PSoC 3 and PSoC 5LP's GPIOs offer a double input synchronization feature, and a single output synchronization feature. Both may be enabled or disabled as desired using the pin component's customizer. If a signal from a pin is to be used as the master clock, it is important that it be desynchronized.

Note See the PSoC 3 and PSoC 5LP TRMs for more details on signal synchronization.

Clocks and Low Power Modes

PSoC 3 and PSoC 5LP's low power modes are most easily described by which clocks may operate:

- In active and alternative active modes, all clocks may operate.
- In sleep mode, only the kHz frequency clocks, the 32.768 kHz ECO and ILOs, may operate.
- In hibernate mode, no clocks may operate.

Clocks in Active and Alternative Active

The best way to reduce active mode current consumption is to disable resources. The second best way is to reduce the clock speed of resources. If the designer has turned off all silicon resources that they are not using, then the remaining method for reducing current consumption is to reduce the frequencies of the various clocks in the part.

The master clock is the fastest clock in the system, and should match the fastest clock used for a peripheral or the CPU. The clocking tree is a large consumer of clock dependent current. Reducing the master clock frequency can have great benefits to current consumption.

Component operating frequencies should also be reduced if possible. Components for things such as digital communication cannot be slowed and maintain the same operation, but it is worth considering decreasing the operational frequency of other resources, such as timers, ADCs, and digital filters.

Entering Low Power Modes

When entering sleep and hibernate modes, it is essential that PSoC 3 and PSoC 5LP's clock tree be properly configured. When entering these modes, the IMO must be used as the master clock source. The PLL and MHz ECO must be turned off. These steps may be carried out by simply using the APIs automatically provided by PSoC Creator. To save and restore the clock configuration around low power events, use the *CyPmSaveClocks()* and *CyPmRestoreClocks()* APIs. These APIs are documented in depth in the System Reference Guide.

Exiting Low Power Modes

Upon exiting sleep and hibernate modes, PSoC 3 and PSoC 5LP will always be configured to use the IMO as the master clock source. There are two options for IMO frequency at startup: normal and fast start IMO. If, in the register FASTCLK_IMO_CR, the third bit ("FIMO_EN") is set, the 48 MHz nominal fast start IMO output is used. If this bit is not set, then the IMO is configured to run at the frequency selected when it was put to sleep.

After exiting sleep and hibernate modes, firmware should re-enable clock sources such as the PLL and MHz ECO, if they are to be used. It should also reconfigure the IMO if a different frequency is desired. This can be carried out using the *CyPmRestoreClocks()* API mentioned previously.

IMO and ILO Trimming

The IMO and ILO both generate a clock output that is controlled by trim registers. Their trim values at various frequencies are determined in the factory, and stored in flash. This is how accurate clock generation is achieved at various fixed frequencies.

Both the IMO and the ILO trim registers can be modified during operation to improve frequency accuracy. If a reference clock source is available, this can improve the accuracy of the IMO and ILO outputs significantly.

PSoC 3 and PSoC 5LP IMO and ILO trimming at runtime are discussed in detail in AN80248, which also provides an example project.

Implementing a system to trim clock sources at run time requires measuring clock error against a reference clock source, and modifying trim to improve the error. Measuring error with a reference clock source can be implemented multiple ways. If the signals are slow, such as the ILO, a simple software counter can be implemented. A software counter uses an interrupt to increment a count, and the count is checked and cleared every second or so. Thus, the detected frequency is equal to the count. For faster clocks, digital hardware should be used. PSoC 3 and PSoC 5LP's Counter component provides the perfect tool for counting the number of MHz frequency clock edges in a given period of time. The low frequency reference clock should be used as the capture input to the Counter.

The IMO is trimmed using registers IMO_TR1 and IMO_TR0. The 3 highest bits of IMO_TR0 make up the least significant bits (LSB) of the 11 bit total trim. The 8 bits of IMO_TR1 are the most significant bits (MSB). The IMO's frequency range from maximum to minimum trim is approximately -33%/+25%. At 11 bits total, this results in resolution of about 333 PPM per bit. At 333 PPM per bit, trim can achieve 167 PPM or lower error every time. Compared to the ±1% or ±2% accuracy of the IMO across temperature at 3 MHz, a runtime trimmed system could be much more accurate.

The ILO's 1 kHz and 100 kHz outputs are trimmed independently. Their trims are both stored in the ILO_TR0 register. The 100 kHz output's trim makes up the 4 MSBs of the register, and the 1 kHz output's trim is in the 4 LSBs. The output range from maximum to minimum trim is approximately -80%/+70%. At 4 bits, this results in a resolution of about 10% per bit. At 10% per bit, trim can achieve 5% or less error every time. Compared to the –50%/+100% accuracy of the ILO across temperature, a runtime trimmed system could be much more accurate. A standard "ILO Trim" component may be placed in the user's schematic. This component allows the user to call a function which trims the ILO to be within +/-10% instead of the initial accuracy of -50%/+100%. See the "ILO Trim" component data sheet for more information.

Summary

PSoC 3 and PSoC 5LP's powerful clocking systems offer nearly infinite configuration possibilities. Understanding this clock system will help optimize your project for maximum performance.

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**	2901619	MAXK	03/30/2010	New application note
*A	3206913	MAXK	03/27/2011	Added IMO trim information Updated abstract Added ECO detail Added low power mode detail Updated electrical specifications
*B	3348446	MAXK	08/22/2011	Clarified text. Updated electrical specs in clock propagation diagram.
*C	3558896	MAXK	03/22/2012	Added information about clock input pin synchronization Updated for Creator 2.0
*D	3714572	MAXK	08/16/2012	Added PSoC 5 Updated Diagrams and PLL Description
*E	3819235	MAXK	11/22/2012	Updated for PSoC 5LP.
*F	4341009	MEH	4/7/2014	Minor grammatical changes
*G	4670664	MEH	03/04/2015	Updated Figures 1 and 4 to reflect the 80 MHz clock option for 5LP. Clarified some of the clock terminology
*H	5730137	AESATP12	05/16/2017	Updated logo and copyright.

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