Programmable Threshold Comparator Datasheet CMPPRG V 3.3

Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	flash	RAM	
CY8C29/27/24/22xxx, CY8C23x33, CY7C64215, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52						
	0	1	0	52	0	1

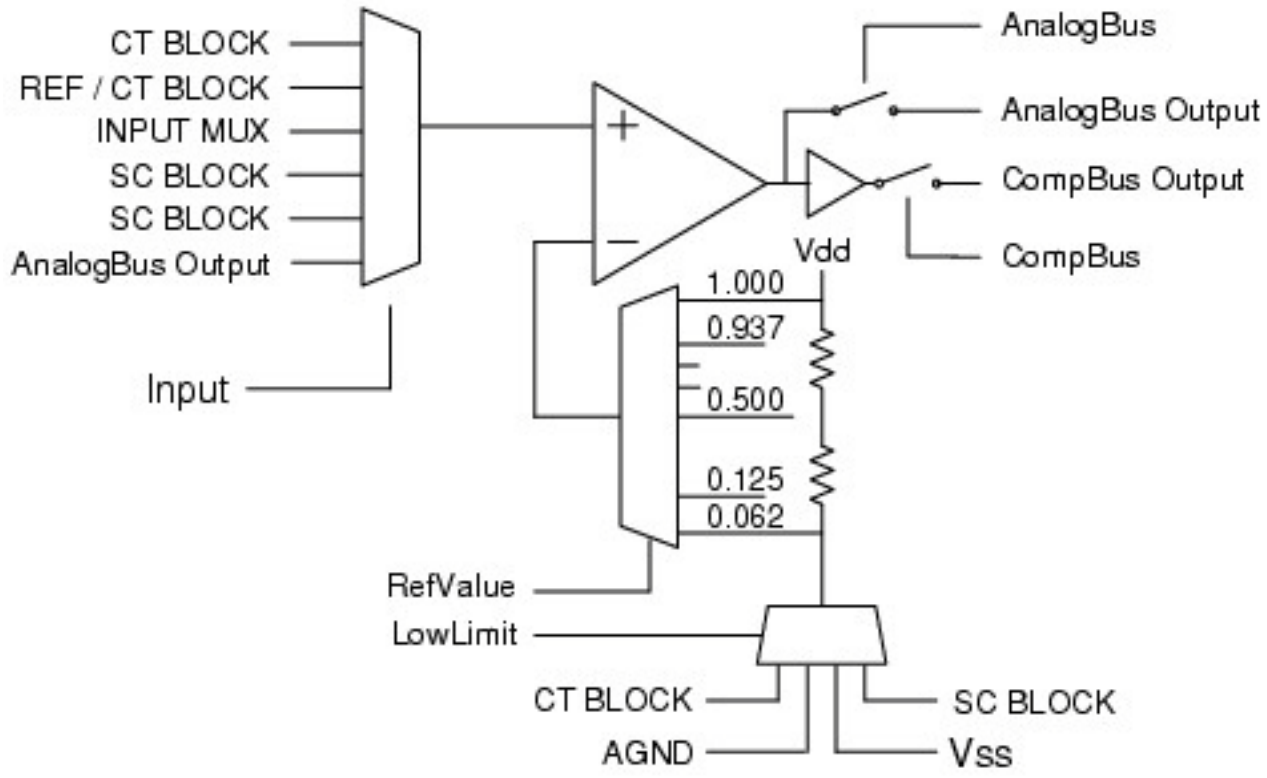
For one or more fully configured, functional example projects that use this user module go to www.cypress.com/psocexampleprojects.

Features and Overview

- Programmable threshold and reference
- Direct connection to digital PSoC block and interrupt
- Programmable speed and power

The CMPPRG User Module provides a comparison of the selected input against a programmable reference threshold. This user module has considerable flexibility in input and reference connections. Speed of the comparator is adjusted by programming the power level of the opamp in the PSoC block.

Figure 1. CMPPRG Block Diagram



Functional Description

The comparator is formed from a continuous time opamp with the internal compensation capacitor disabled. The positive input is connected to the input multiplexer. The negative input is connected to the tap of a resistive divider between Vdd and the selected reference, LowLimit.

The threshold value of the comparator is determined by the following equation.

Equation 1

$$V_{Threshold} = LowLimit + (Vdd - LowLimit) \cdot RefValue$$

When LowLimit is connected to AGND, there is an error term due to offset voltage from the analog ground buffer within the PSoC block. When LowLimit is connected to Vss, this error term is zero and thresholds will be slightly more accurate.

The input range and the RefValue (effective threshold) are limited, by the common mode input range of the continuous time opamp. See the DC and AC Electrical Characteristics section for Input Voltage Range and Output Swing parameters. An additional amplifier follows the continuous time opamp, to provide full logic levels and fast rise times for digital blocks.

The output polarity follows the inputs (i.e., a positive input greater than the negative input to the comparator results in a positive output logic level). The response time of the comparator is determined by the amount of over-drive and the power level programmed.

The output of the comparator can be accessed in two ways, the direct analog output from the comparator can be switched onto the AnalogBus, then passed to an analog buffer to drive an output pin. The comparator logic output can be switched onto the CompBus to drive the enable inputs of digital blocks, the interrupt controller, and a register that can be read by the CPU.

The analog column clock is required to latch the output of the comparator to the comparator register (CMP_CR0). The frequency of the column clock should be selected to be at least two to four times faster than the bandwidth of the incoming comparator signal. If the analog column clock is set to low, the comparator may not catch fast input transients.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25°C, Vdd = 5.0V, Power HIGH, Opamp bias LOW, LowLimit = Vss.

Table 1. 5.0V CMPPRG DC Electrical Characteristics, CY8C29/27/24/22xxxFamily of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Threshold				
Ref=0.75	0.87	--	%	Deviation from nominal relative to Vdd
Ref=0.5	0.40	--	%	
Ref=0.125	0.44	--	%	
Voltage Gain	10	--	V/mV	
Input				
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
Operating Current				
Low Power	148	--	µA	
Med Power	545	--	µA	
High Power	2100	--	µA	

Table 2. 5.0V CMPPRG AC Electrical Characteristics, CY8C29/27/24/22xxxFamily of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Response Time[2]				100 mV step at input
Low Power	5.0	--	µs	Internal
Med Power	3.5	--	µs	
High Power	1.2	--	µs	

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25°C, Vdd = 3.3V, Power HIGH, Opamp bias LOW, LowLimit = Vss.

Table 3. 3.3V CMPPRG DC Electrical Characteristics, CY8C29/27/24/22xxxFamily of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Threshold				
Ref=0.75	0.41	--	%	Deviation from nominal relative to Vdd
Ref=0.5	0.33	--	%	
Ref=0.125	0.85	--	%	
Voltage Gain	10	--	V/mV	
Input				
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
Operating Current				
Low Power	136	--	µA	
Med Power	524	--	µA	
High Power	2100	--	µA	

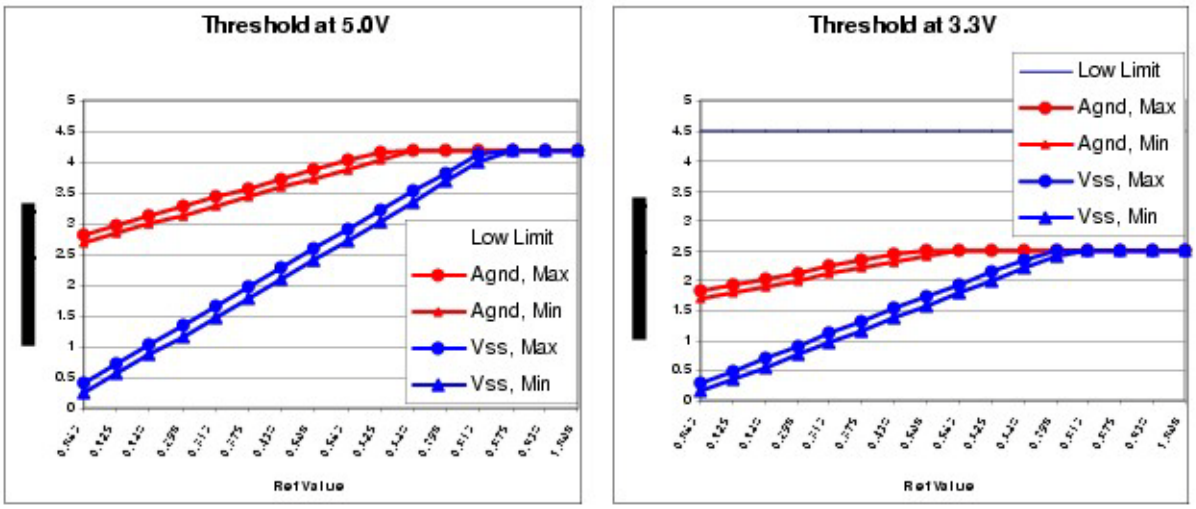
Table 4. 3.3V CMPPRG AC Electrical Characteristics, CY8C29/27/24/22xxxFamily of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Response Time[2]				100 mV step at input
Low Power	5	--	µs	Internal
Med Power	2	--	µs	
High Power	0.6	--	µs	

Electrical Characteristics Notes

1. Includes I/O pin.
2. Based upon device simulation.
3. Typical values represent parametric norm at +25°C. Limits are guaranteed by testing or statistical analysis.
4. Reference input offset voltage algebraically added to selected reference voltage low limit.
5. Response time on internal connection to digital blocks includes load of internal analog bus if enabled.

Figure 2. Threshold Voltage versus RefValue, Power = HIGH



Placement

The COMP block maps freely onto any of the continuous time PSoC blocks in the device. However, if the COMP AnalogBus output and the CompBus output are enabled onto their respective buses, care must be exercised to ensure that no other user module tries to drive the same buses.

Parameters and Resources

Input

The Input is selectable from one of six sources. These include the pin input multiplexer, analog CT block outputs, SC block outputs, internal reference, and the analog output bus. The specific inputs available vary with the placement of the user module on the chip as shown in the Device Editor.

LowLimit

The reference LowLimit is selected from Analog Ground (AGND), Vss, connection to a continuous time PSoC block, and connection to a switched capacitor PSoC block. AGND and Vss provide for selection of fixed thresholds. Connection to adjacent CT or SC block provides an adjustable threshold. Specific selection of reference from PSoC blocks is made in the Device Editor.

If the adjacent CT block used as LowLimit source, this block should be used in Gain mode (Gain bit of CR0 register should be “1"). E.g. PGA UM gain should be equal to or greater than 1. Because LowLimit input connected directly to adjacent block’s opamp output and if this block is in Loss mode then the received LowLimit value is not correct (does not match the calculated value).

RefValue

The reference level is programmable in 6.25 percent steps between the reference LowLimit and Vdd. When the reference low limit is selected at Vss and operating from a 5.00 volt supply, this sets reference values of 0.3125 volts to 5.00 volts, in 0.312 volt steps. When the reference low limit is selected as AGND and analog ground is selected in PSoC Designer to be AGND +/- BandGap, the reference can be set at AGND (2.600 V) + 0.150 volts to 5.00 volts, in 0.150 volt steps.

CompBus

The COMP block comparator output may be routed to the input bus of the digital PSoC blocks or to an interrupt. The CompBus must be enabled to make any of these connections.

AnalogBus

The COMP block opamp output may be routed to the AnalogBus to provide a direct logic-out signal. This signal is routed to an I/O pin through the Analog Buffer, so the rise time is limited by the slew rate of the analog buffer. The rise time is approximately 3 µs. This may be acceptable for some slow logic applications.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include" files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X prior to the call if those values are required after the call. This “registers are volatile" policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API function may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

CMPPRG_Start

Description:

Performs all required initialization for this user module and sets the power level for the continuous time PSoC block. The comparator output will be driven.

C Prototype:

```
void  CMPPRG_Start(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  CMPPRG_Start
```

Parameters:

bPowerSetting: One byte that specifies the power level to the analog PSoC block. Following reset and configuration, the PSoC block assigned to the comparator is powered down. Symbolic names provided in C and assembly, and their associated values, are given in the following table.

Symbolic Name	Value
CMPPRG_OFF	0
CMPPRG_LOWPOWER	1
CMPPRG_MEDPOWER	2
CMPPRG_HIGHPOWER	3

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

CMPPRG_SetPower

Description:

Sets the power level for the continuous time PSoC block. The comparator output will be driven. May be used to turn the block off and on.

C Prototype:

```
void  CMPPRG_SetPower(BYTE bPowerSetting)
```

Assembler:

```
mov   bPowerSetting
lcall  CMPPRG_SetPower
```

Parameters:

bPowerSetting: One byte that specifies the power level to the analog PSoC block. Following reset and configuration, the PSoC block assigned to the comparator is powered down. Symbolic names provided in C and assembly, and their associated values, are given in the following table.

Symbolic Name	Value
CMPPRG_OFF	0
CMPPRG_LOWPOWER	1
CMPPRG_MEDPOWER	2
CMPPRG_HIGHPOWER	3

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

CMPPRG_SetRef

Description:

Sets the reference value for the comparator.

C Prototype:

```
void  CMPPRG_SetRef(BYTE bRefValue)
```

Assembler:

```
mov   A, bRefValue
lcall  CMPPRG_SetRef
```

Parameters:

bRefValue: Symbolic names provided in C and assembly and their associated values are given in the following table. The values provide a comparator threshold at LowLimit + RefValue*(Vdd-LowLimit).

Symbolic Name	Value	Symbolic Name	Value
CMPPRG _REF1_000	F0h	CMPPRG _REF0_437	60h
CMPPRG _REF0_937	E0h	CMPPRG _REF0_375	50h
CMPPRG _REF0_875	D0h	CMPPRG _REF0_312	40h
CMPPRG _REF0_812	C0h	CMPPRG _REF0_250	30h
CMPPRG _REF0_750	B0h	CMPPRG _REF0_188	20h
CMPPRG _REF0_688	A0h	CMPPRG _REF0_125	10h
CMPPRG _REF0_625	90h	CMPPRG _REF0_062	00h
CMPPRG _REF0_562	80h	*CMPPRG _REF0_042	14h
CMPPRG _REF0_500	70h	*CMPPRG _REF0_021	04h

* These values are only applicable for the CY8C29/27/24/22xxxfamily of devices.

Return Value:

None

Side Effects:

Comparator output will be driven. RefValue will be momentarily reset to 0.62, during routine, then programmed to desired value. This may result in false reading from the comparator while the RefValue is being changed. The A and X registers may be altered by this function.

CMPPRG_Stop

Description:

Powers the user module off. The outputs will not be driven.

C Prototype:

```
void  CMPPRG_Stop(void)
```

Assembler:

```
lcall  CMPPRG_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

Sample Firmware Source Code

The sample code given here creates a comparator with the RefValue (threshold) set to 0.500, over-riding the threshold value set in the PSoC Designer Device Editor.

```
;;-------------------------------------------------------------------
;; Sample Code for the CMPPRG
;; Turn on power and set RefValue (threshold) to 0.500.
;;     Sets RefValue to Vlowlimit + 0.5* Vdd-Vlowlimit
;;     = 3.75 V with 5.00 V supply
;;-------------------------------------------------------------------

export _main

include "m8c.inc"
include "CMPPRG.inc"

_main:

mov  A, CMPPRG_REF0_500           ; specify RefValue
call CMPPRG_SetRef                ; update amplifier gain

mov  A, CMPPRG_MEDPOWER           ; specify Comparator power level
call CMPPRG_Start                 ; and turn it on
; Place user code here
ret
```

The same project written in C is as follows.

```
//-------------------------------------------------------------------------
//  Sample C Code for the CMPPRG
//  Turn on power and set RefValue (threshold) to 0.500.
//    Sets RefValue to Vlowlimit + 0.5* Vdd-Vlowlimit
//    = 3.75 V with 5.00 V supply
//
//-------------------------------------------------------------------------
#include <m8c.h>        // Part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

void main(void)
{
   CMPPRG_SetRef(CMPPRG_REF0_500);       // Set RefValue
```

```
    CMPPRG_Start(CMPPRG_MEDPOWER);         // Set power level and
                                           // turn it on
     // Place user code here
}
```

Configuration Registers

The basic topology of the comparator sets most of the bits in the register configuration for the analog CT block that is used. Specific inputs available for comparison and reference are determined by user module placement.

Table 5. Block COMP, Register: CR0

Bit	7	6	5	4	3	2	1	0
Value	RefValue				1	0	LowLimit	

RefValue is the reference value chosen as a percentage of Vdd-LowLimit and is set in PSoC Designer. It is modified by calling the SetRef entry point in the API. LowLimit is the lower limit of the reference value range and is set in PSoC Designer.

Table 6. Block COMP, Register: CR1

Bit	7	6	5	4	3	2	1	0
Value	Analog Bus	Comp Bus	1	0	0	Input		

AnalogBus determines whether the COMP PSoC block drives the analog bus. CompBus determines whether the COMP PSoC block drives the comparator bus. The value of these bit-fields are determined by the choice made in user module Placement mode of the Device Editor subsystem.

Table 7. Block COMP, Register: CR2

Bit	7	6	5	4	3	2	1	0
Value	0	1	0	0	0	0	Power	

Power is set to ‘Off’ following the device reset and configuration. It is modified by calling Start, SetPower, or Stop entry points in the API.

Table 8. Block COMP, Register: CR3

Bit	7	6	5	4	3	2	1	0
Value	0	0	0	0	LPCMPEN	0	0	EXGAIN

LPCMPEN: Set to enable low power comparator mode.

EXGAIN: This bit is set automatically when either the 0.042 or 0.021 compare values are selected.

Version History

Version	Originator	Description
3.3	DHA	Added Version History.

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.