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Spec No: 001-53490

Spec Title: AN53490 - CAPSENSE(R) EXPRESS(TM) - DESIGN TO PRODUCTION

Replaced by: None

AN53490

CapSense® Express™ – Design to Production

Author: Vibheesh B
Associated Project: No
Associated Part Family: CY8C201xx
Software Version: PSoC Designer™ 5.0 + SP5
For a complete list of the application notes, click here.

The CapSense® Express™ family of touch sensing devices easily integrates into various products. They often replace existing mechanical switches and push buttons with little or no impact on the rest of the design. This application note describes methods and tips on how to smoothly design these devices; it also helps you make a robust design with CapSense Express.

Contents

1 Introduction

CapSense® is a widely accepted technology used to replace conventional mechanical switches. Cypress's new CapSense Express is a high performance fixed function CapSense enabled device that does not require any programming effort, unlike other CapSense-enabled PSoC® devices. CapSense Express is an extremely configurable and flexible device, which does not require any external components for each sensor; it only requires an optional external capacitor for increased sensitivity. It incorporates a robust sensing technology, which is highly immune to noise and environmental conditions.

When designing a system with CapSense many factors contribute to the overall performance. All these parameters are discussed here with suggestions and methods of analysis to help you build a solid, robust design. The following table lists the available CapSense Express devices.

Table 1. CapSense Express Device Selection List

Device	Total I/O	I^2C	Package	Order Information
CY8C201A0	10	I^2C	16-QFN	CY8C201A0-LDX2I
			16-SOIC	CY8C201A0-SX2I
CY8C20110	10	I^2C	16-QFN	CY8C20110-LDX2I
			16-SOIC	CY8C20110-SX2I
CY8C20180	8	I^2C	16-QFN	CY8C20180-LDX2I
			16-SOIC	CY8C20180-SX2I
CY8C20160	6	I^2C	16-QFN	CY8C20160-LDX2I
			16-SOIC	CY8C20160-SX2I
CY8C20140	4	I^2C	16-QFN	CY8C20140-LDX2I
			16-SOIC	CY8C20140-SX2I
CY8C20142	4	I^2C	8-SOIC	CY8C20142-SD1I
CY8C20121	4	I^2C	8-SOIC	CY8C20121-SX1I
CY8C20111	2	I^2C	8-SOIC	CY8C20111-SX1I

2 Overview

The following topics are discussed in this application note:

- The recommended design shapes for CapSense Express design
- Possible sources of noise and how to avoid them in the layout
- How to select good overlay for your product
- How to find the optimum value of C_{INT} Capacitor for the design
- Performance of the CapSense Express device against major noise sources and test results
- Considerations for mass production of your CapSense Express design and useful statistical analysis and tuning suggestions
- Configuring CapSense Express in production
- Known constraints of the device and workarounds

3 A Good CapSense Sensor Design

A capacitive sensor can be designed by placing a copper pad on the PCB connected to PSoC, which is surrounded by ground. Having ground around the sensor reduces the noise affecting the sensor and at the same time, increases the parasitic capacitance of the sensor. Parasitic capacitance (C_P) is the unavoidable and usually unwanted capacitance that exists between the sensor pad and circuit ground because of their proximity to each other. This is the same capacitance sensed by CapSense Express when no finger is present. During the finger touch, the total capacitance increases due to the capacitance added by the finger, which is defined as finger capacitance (C_F). CapSense Express has a complicated equation describing how C_P and C_F are related to the signal. But for a fixed value of C_P and for small amounts of added C_F, the signal is proportional to C_F. A finger touch that results in increase of capacitance (thereby producing a higher signal in the system) is directly proportional to the area of the sensor, relative permittivity of the overlay, and inversely proportional to thickness of overlay.

A design with lesser C_P generates better signal or increases the dynamic range of system at properly tuned conditions. The CapSense Express device can measure maximum (full-scale reading) 30 pF of parasitic capacitance. The sensitivity of the CSA sensors roll off for C_P values above 30 pF.

4 CapSense Best Practices

Following CapSense best practices help the design to have high noise immunity, lower C_P, and higher signal to noise ratio (SNR). The easy way to reduce C_P is to keep ground away from the sensor, which in turn increases the noise. So it is a tradeoff between keeping best noise immunity and getting the best signal. From the basic parallel plate capacitance equation (mentioned in the section Right Overlay for CapSense), the following equation for C_P is derived:

Equation 1 $C_P \propto \frac{S_S+L_T+W_T}{D_A}$

Table 2. Parameters Affecting Sensor C_P

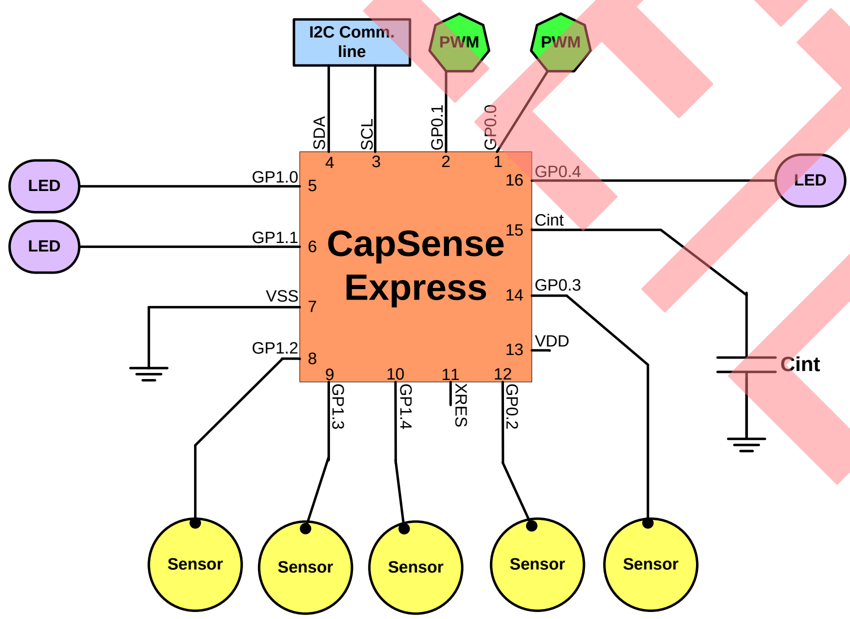
Symbol	Parameter	Effects
S_S	Size of the sensor	Proportionally affects the area of cross section with ground
L_T	Length of the trace	Proportionally affects the area of cross section with ground, because the traces are surrounded by ground
W_T	Width of the trace	Proportionally affects the area of cross section with ground
D_A	Annular gap (Sensor to ground clearance)	Inversely proportional to capacitance from basic formula

C_P can be reduced by narrowing or shortening traces, avoiding very large sizes for sensors pads, providing sufficient clearance between sensor and ground, and reducing the number of via holes and having a proper size for sensor pads.

5 Sensor and Device Placement

Minimize the trace length from CapSense Express to the sensor by keeping the sensor close to the CapSense Express device. Mount the device and components on the bottom layer of the PCB and the CapSense sensors on the top layer for easy routing and overlay placement. Place the device in the middle of all sensors so that the all sensors have shortest trace length from sensor to device.

Figure 1. Best Pin Assignment Picture



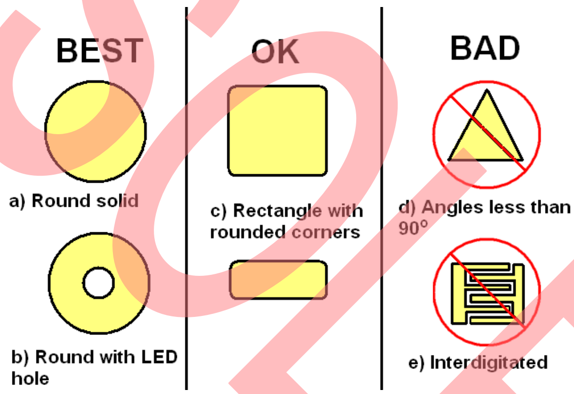
Isolate any switching signal such as PWM, I^2C communication lines, and LEDs from the sensor and sensor traces. Do this by keeping them away and placing hatched ground between CapSense traces and non-CapSense traces to avoid cross talk. Figure 1 shows a suitable pin assignment for a CapSense design.

In this pin assignment, all CapSense inputs are assigned from one or two sides of the chip; PWM, LED, and I^2C signals are from the other side of the chip. This enables easier routing and helps to maintain distance between the CapSense traces and non-CapSense traces. Even though the CapSense Express device can be made to work correctly with connectors, do not use any kind of connector between the sensor and device because connectors increase C_P and decrease noise immunity.

6 Button and Slider Designs

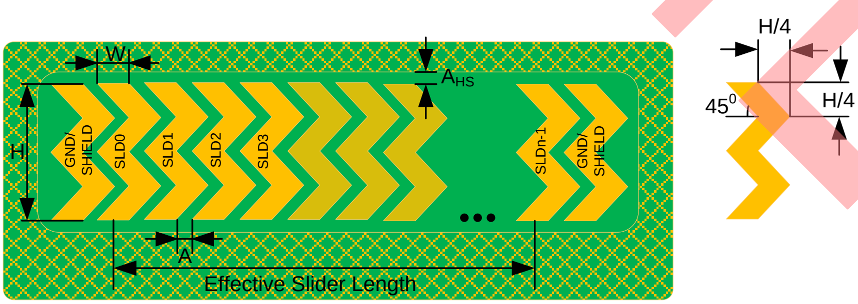
The best shape for buttons is round. Rectangles with curved corners can be used for sensors. Do not use shapes with angles less than 90 degrees for CapSense sensor design and traces (because it concentrates charge in the corners). Avoid sharp corners in the CapSense sensor and the traces. The diameter of buttons can be from 5 mm to 15 mm with 10 mm being suitable for majority of applications that work with a finger. A 15 mm diameter helps when using thicker overlays. The annular gap (clearance between the button and hatched ground) must be equal to the overlay thickness limited to between 0.5 mm and 2 mm. For example, 1 mm overlay design should keep 1 mm annular gap and 3 mm overlay design keeps a gap of 2 mm. The spacing between the two buttons can be defined such that if one button is pressed, the finger should not reach the annular gap of the other button.

Figure 2. Recommended Button Shapes



All the best practices for a button are applicable to slider designs too. In CapSense Express, a slider design should have either 5 or 10 sensors and all sensors should have zigzag (saw tooth) pattern as shown in Figure 3. One finger touch affects more than one sensor. The slider can be semi-circular and other shapes where the first and last slider segments are not touched by a single finger touch. Diplexing and radial (circular) slider features available in other CapSense devices are not available with the CapSense Express part.

Figure 3. Recommended Slider Segment Design



The recommended dimensions for slider design are given in the following table:

Table 3. Dimensions for Slider Design

Parameter	Acrylic Overlay Thickness	Min	Max	Recommended
Width of the segment (W)	1 mm	2 mm	-	8 mm[1]
	3 mm	4 mm	-	
	4 mm	6 mm	-	
Height of the segment (H)	-	7 mm[2]	15 mm	12 mm
Air gap between segments (A)	-	0.5 mm	2 mm	0.5 mm
Air gap between the hatch and the slider (A_{HS})	-	0.5 mm	2 mm	Equal to overlay thickness

7 Layout and Routing

Efficient routing results in lower parasitic capacitance and higher noise immunity for the design. The width of the trace should be 7 mil (0.1777 mm). CapSense traces should be surrounded by hatched ground with trace to ground clearance of 10 to 20 mil (0.254 to 0.508 mm). One inch trace (25.4 mm) on FR4 PCB according to the suggestion mentioned here has approximately 2 pF of capacitance. Hence the maximum recommended trace length is 8 inches or 203 mm. (A design having 8-inch trace length approximately consumes 75 percent of the measurement range of CapSense Express). CapSense traces should be routed on the bottom layer and should not use more than two via holes as they increase the C_P. The hatched ground should have 10 percent density on the signal layer (bottom) and 15 percent density on the other layer (top) for best performance. Increasing the density of ground filling increases the C_P. Table 4 lists all limitations and guidelines for layout.

Table 4. Layout Limitations

Parameter	Limit or suggestion
Recommended width of CapSense trace	7 mil (0.177 mm)
Recommended maximum length of trace	Less than or equal to 8000 mil (8 inches, 203 mm)
Trace to hatched ground clearance	10 to 20 mil (0.254 to 0.508 mm)
CapSense trace to CapSense trace clearance	10 to 20 mil (0.254 to 0.508 mm)
Recommended layer for CapSense trace routing	Bottom layer (Signal layer)
Recommended layer for capacitive sensor placement	Top layer (Sensor layer)
On 4-layer boards	CapSense Sensors on Top layer CapSense traces on second layer Hatched ground (10% filling) on the third layer Fourth layer is free for general signal routing (No hatched ground is required)

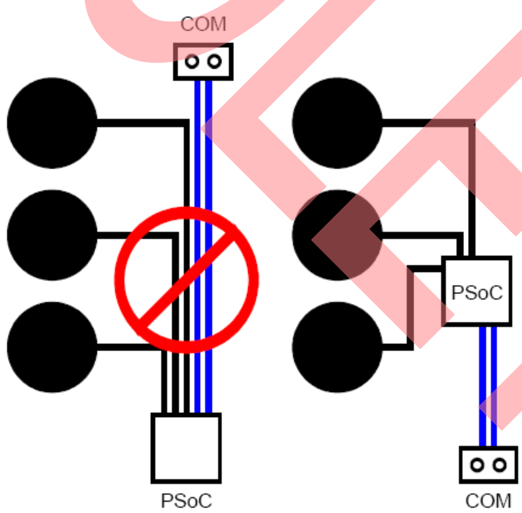
[1] The recommended slider-segment width is based on an average human finger diameter of 9 mm. Refer to the section "Slider-Segment Shape, Width, and Air Gap" in "Getting Started with CapSense Design Guide" for more details.

[2] The minimum slider segment height of 7 mm is recommended based on a minimum human finger diameter of 7 mm. Slider height may be kept lower than 7 mm if the overlay thickness and CapSense tuning is such that an SNR ≥ 5:1 is achieved when the finger is placed in the middle of any segment.

Parameter	Limit or suggestion
Hatched ground recommendation on top layer	7 mil (0.177 mm) trace and 45 mil (1.143 mm) distance between traces (15% filling)
Hatched ground recommendation on bottom layer	7 mil (0.177 mm) trace and 70 mil (1.778 mm) distance between traces (10% filling)
Sensor to hatched ground clearance (annular gap)	If overlay thickness less than 0.5 mm, it should be equal to 0.5 mm If overlay thickness is between 0.5 mm and 2 mm, it should be equal to overlay thickness. If overlay thickness is more than 2 mm, it should be equal to 2 mm
Preferred PCB	FR4 material with a thickness 0.5 mm to 1.6 mm performs better The design can also be implemented in the flex PCBs. In this case higher C_{INT} capacitor may be required as flex PCBs usually have higher C_P. (Shin-Etsu polymer Co. Ltd. makes flex PCB based sensors for CapSense applications)
Maximum number of via hole recommend on CapSense traces	Less than or equal to 2
Via hole position	On the edge of the sensor such that trace length is reduced
Via hole size	10 mil (0.254 mm) or lesser suggested
Placement of series resistors	As close as possible to CapSense Express pin

Apart from the suggestions mentioned in this section, multiple CapSense traces can be routed in parallel, closer, or underneath another CapSense trace with minimum 10-mil clearance. A CapSense trace and a non-CapSense signal should not be routed in parallel, closer, or underneath the CapSense sensor or traces as this can create cross talk. Figure 4 shows an example of both bad and recommended signal routing of a design with communication interface and CapSense.

Figure 4. CapSense and Non CapSense Signal Routing



If any non-CapSense signal needs to cross over a CapSense signal, it should be at 90º such that the area of overlapping is minimized. A CapSense trace should not be routed underneath the sensor or annular gap (sensor to hatched ground clearance) because activating the sensor with the finger creates noise (minor signal) to the sensor trace routed underneath.

Figure 5. CapSense and Non CapSense Signal Routing on Multilayer PCB

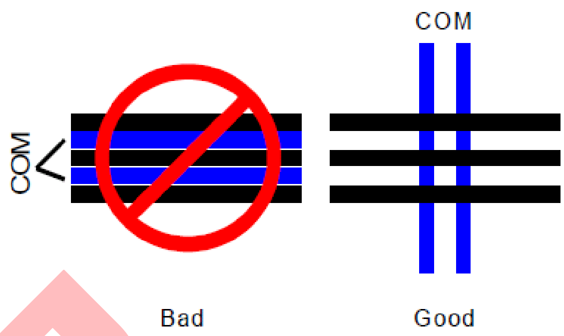


Figure 6 shows a good layout for two buttons with LED backlight and a five-segment slider layout design by following the best practices. Figure 7 shows the bottom layer of the same design.

Figure 6. Top Layer of an Excellent Button and Slider Layout

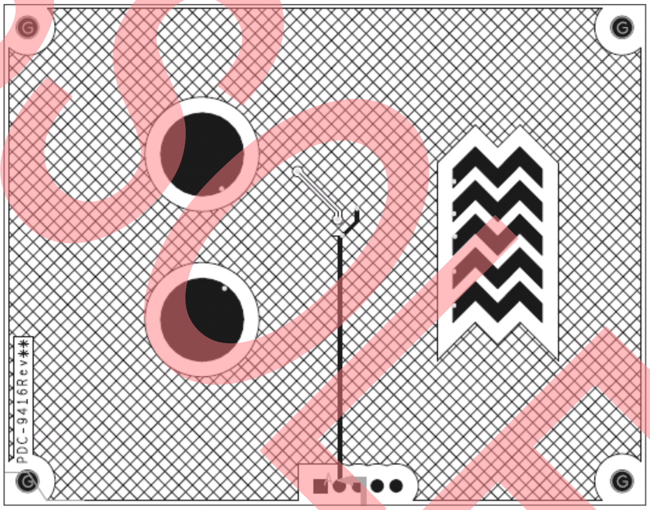
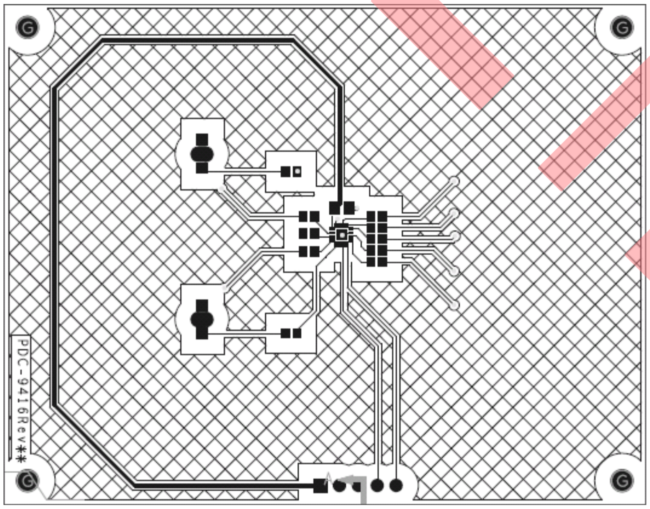


Figure 7. Bottom Layer of an Excellent Button and Slider Layout



7.1 Right Overlay for CapSense

In CapSense, the overlay is the material that is placed over the sensor and protects the sensor from direct contact with the sensed element – the human finger.

Conductive material cannot be used as an overlay; the presence of conductive material such as metal or water (CapSense Express is not water-tolerant) can create false triggering (false detection) in CapSense Express. Some metallic finish paints contain metal particles and must not be used in the overlays.

If any adhesive is used to stick the overlay on the PCB, it should not contain conductive particles. 3M™ makes good quality transparent acrylic adhesive such as 200MP, which is qualified for use in CapSense applications (the product numbers are 467MP and 468MP).

The dielectric constant of air is very low (as mentioned in Table 5) and, therefore, an air gap between the overlay and sensor degrades the performance of the sensor.

If the sensor pad and the human finger are considered the two plates of a parallel plate capacitor, the overlay becomes the dielectric material between the capacitor plates. The following is a basic capacitor equation:

Equation 2 $Capacitance\,(C) = \frac{\varepsilon_0 * \varepsilon_r * A}{D}$

Capacitance is directly proportional to the dielectric constant of the material, area of plates (A), and inversely proportional to the distance between the plates (D). Considering Equation 2:

- Use of overlay material with higher dielectric constant increases the signal strength, which helps achieve better SNR and enables use of thicker overlays.
- To increase the signal strength or SNR, decrease the overlay thickness (D).
- Increase the button diameter to increase the signal (Increasing button size more than 15 mm is not helpful due to area of contact of finger).

Table 5 . Dielectric Constants of Common Overlay Materials

Overlay	Dielectric Constant (ε_r)	Overlay Thickness for 12 kV ESD Protection
Air	1.0	10
Glass	7.6 – 8.0	1.5
Acrylic	2.8	0.9
ABS	2.4 – 4.1	0.8
Wood-Dry	1.2 – 2.5	3
Gypsum	2.5 – 6.0	-
Mylar	3.2	0.4
Lexan (poly carbonate)	2.9 – 3.0	0.8
Mica	7.0	-
Fiber	5.0	-

ESD protection increases with an increase in the overlay thickness. Table 5 lists the thickness of overlay required to protect the CapSense sensors from 12-kV ESD.

7.2 The Integrating Capacitor (C_{INT})

CapSense Express has a 100 pF internal C_{INT}. A design using overlay less than 1.5 mm thickness can be made to work with this internal C_{INT} capacitor (no external capacitor required). A proper CapSense Express design requires 5:1 SNR, and to achieve this, design may need to use the external capacitor. A design may not be able to meet 5:1 SNR due to the following factors.

- Lower amplitude of signal (finger response) which may be because of higher overlay thickness, smaller sensor size, or higher parasitic capacitance of the sensor

- Exposure to high level of noise, which may be due to power supply fluctuation or external high emission devices such as RF transmitter, inverters, and so on

In these two cases, it is recommended to use the external C_{INT} to increase the signal strength. Note that Increasing the C_{INT} capacitor value increases the signal strength and scan time of the sensor. X7R or NPO type capacitors are recommended for C_{INT} for stability over temperature.

Figure 8. Signal Increase with Respect to Value of C_{INT}

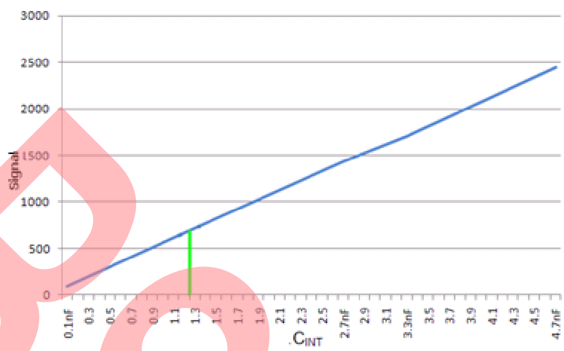
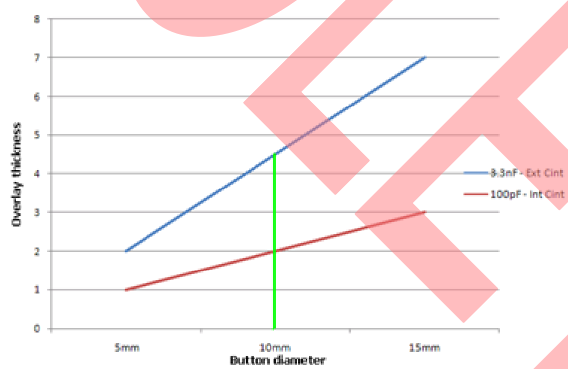


Figure 8 shows the increase in signal on a sensor with respect to values of C_{INT} Capacitor. The data is collected from a sensor designed by following the best practices with 10 mm diameter, 1 mm acrylic overlay, and approximately 10 pF C_P. Typical value of the capacitor is marked with a green line.

Figure 9 shows the maximum recommended thickness of acrylic overlay for CapSense Express design at various conditions. The data is captured from a layout design following best practices, having 2.5 inch of trace length, and IDAC value set to 20. The typical button diameter of 10 mm is marked with a green line.

Figure 9. Recommended Maximum Overlay Thickness



The recommendation in Figure 9 also holds good for different types of overlays mentioned in Table 5 considering their dielectric constants.

8 External Noise Sources

CapSense Express is highly immune to external noise but some of the external noise can significantly decrease the SNR. The guideline for considering external noise source is that the noise injected from the external source should be less than the 30 percent of the finger response of the sensor.

The types of noise, which generally affect CapSense designs are as follows:

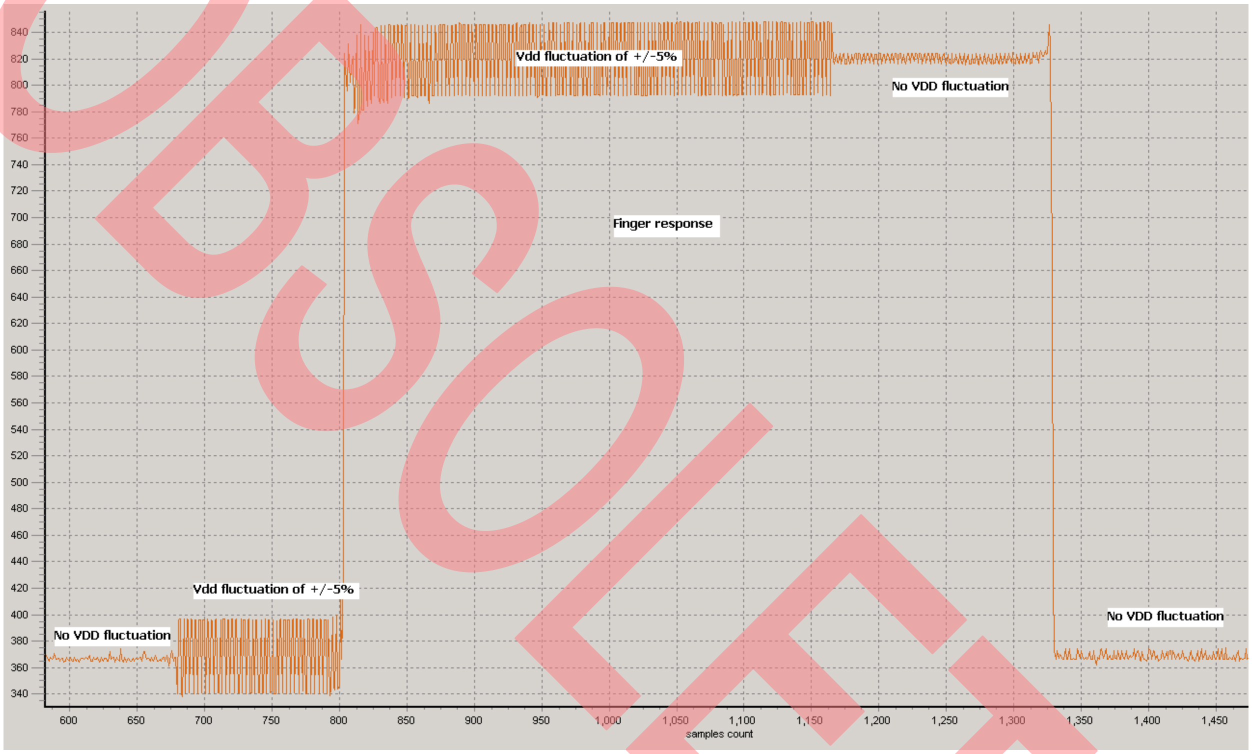
- Power supply transient noise
- Finger conducted AC noise

- Drift due to temperature variation
- Electro Static Discharge (ESD)
- Radiated RF noise and switching noise

8.1 Power Supply Transient Noise

The noise appearing in the raw count of the CapSense Express device when power supply is fluctuating is known as power supply transient noise. It is very important for the CapSense Express device to have stable power supply. The acceptable limit of power supply variation of the CapSense Express is ±5 percent at 5 V, 3.3 V, and 2.7 V operating range.

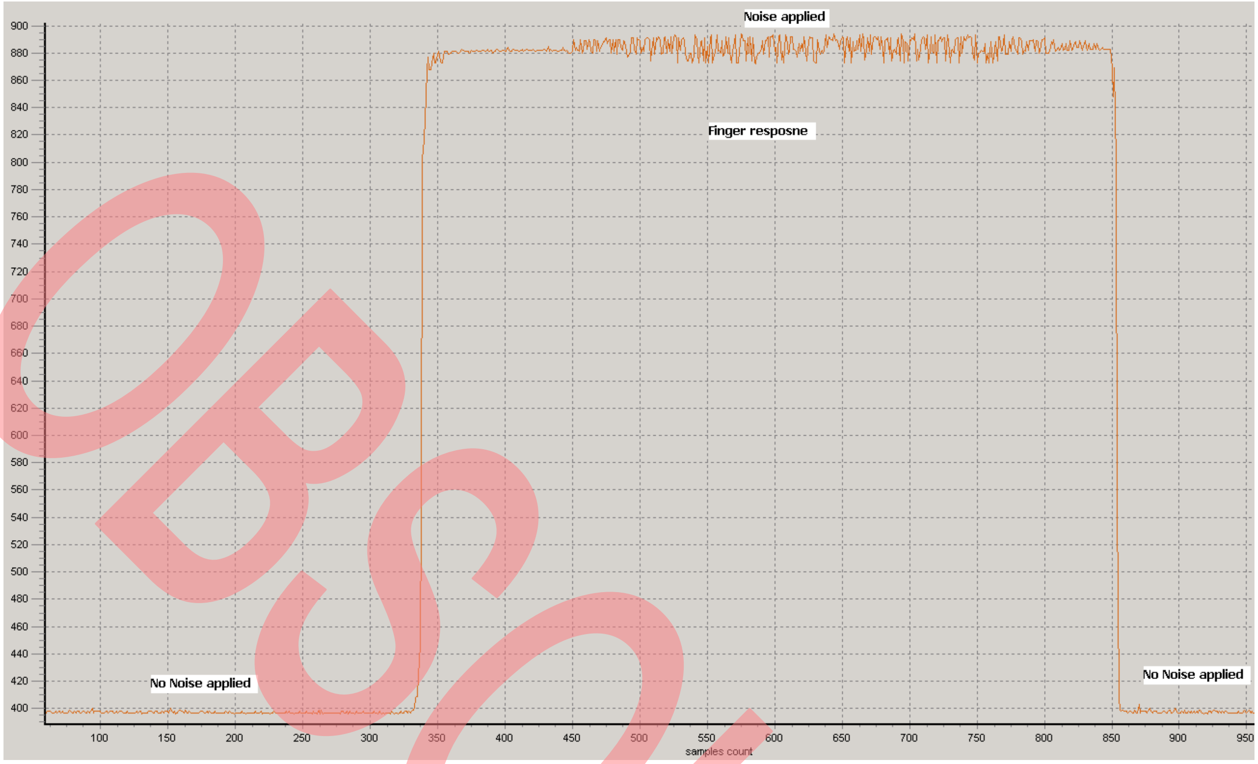
Figure 10. Noise in the CapSense Raw Count Due to VDD Transient



8.2 Finger Conducted AC Noise

In some cases, low frequency AC noise can affect a circuit when it is operated close to such noise sources. CapSense Express is tested against two such sources. The power system ground of the power supply powering CapSense can inject AC noise of 50 Hz or 60 Hz (depending on the country of use) to CapSense sensor.

Figure 11. Noise in CapSense Raw Count Due to Finger Conducted AC Noise



8.3 Drift Due to Temperature Variation

Capacitance can vary with respect to the change in temperature. If the baseline update rate is slow (baseline update threshold value is high) or temperature variation is fast, in some cases the temperature variation can create false triggers. CapSense Express is tested for -40º to +80º operation. X7R or NPO type capacitors are recommended for C_{INT} for stability over temperature.

8.4 Electro Static Discharge (ESD)

The CapSense buttons were tested per the requirements of EN55024 (Amds. A1:2001, A2:2003), method IEC61000-4-2. The tests performed are air discharge of ±15 kV to horizontal ground plane, air discharge of ±4 kV to exposed circuit ground pin, and contact discharge of ±12 kV on overlay. Refer to the CapSense design guide Getting Started with CapSense at www.cypress.com for CapSense design guidelines in compliance with EMC standards.

8.5 Radiated RF Noise and Switching Noise

Immunity to RF radiated noise is a mandatory requirement for a design used in mobile phones or products having radio transmitters.

Keep noise sources very far from the CapSense device, sensors, and traces. One way to deal with RF noise is to add a 560 ohm resistor on all CapSense inputs and 300 ohms on all other GPIO inputs and I^2C lines to dampen the RF radiated noise. Unused I/Os should be configured to strong drive mode GPIO and drive logic ‘0’ to the pin. Refer to the CapSense design guide Getting Started with CapSense for EMC/EMI compatibility information.

If there are any high emission circuits such as SMPS or inverter, they should be shielded to limit the radiation to CapSense system. A multimedia keyboard on the laptop or functional keys on a desktop monitor may need to be placed behind the LCD inverter, which can induce noise to CapSense.

The CapSense scan can be stopped when the noise source is active. For example, in a mobile phone or radio, CapSense scanning can be stopped when the transmitter is active such that the noise from transmitter does not affect the CapSense. Sending 0x0A command to the 0xA0 register stops the CapSense scan. Refer to CY8C201xx Register Reference Guide or CY8C20111/CY8C20121 datasheet for more information.

The CapSense Express uses CSA technology. Cypress has fully programmable CapSense enabled devices with CSD technology, which has pseudo random sequence (PRS) and is highly immune to external noises and low emission.

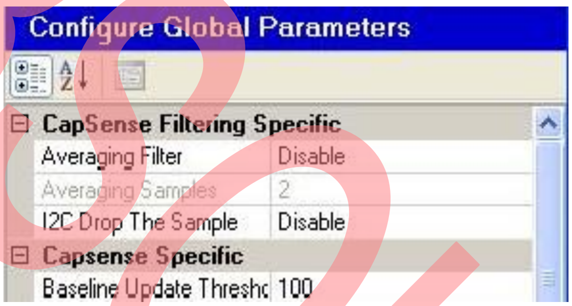
8.6 Filters in CapSense Express

CapSense Express offers the option to apply two types of filters on the raw count to reduce the noise. They are drop the sample' filter and 'average' filter.

The 'I2C drop the sample' filter reduces the noise caused by I2C data transfer to the CapSense. It does so by dropping the scanned data sample if there was an I^2C data transfer between CapSense Express and the master during the last scan. If this filter is enabled, data streaming should be at an interval of 10 ms or more, so that there is sufficient time to scan through all sensors; otherwise an excessive number of data scans are dropped.

The average filter accumulates specified number of consecutive scans or samples and finds their average. The options available are 2, 4, 8, and 16 samples. If the averaging number is higher, the immunity to noise is more. But it slows down the response time. The options to enable the filters mentioned in this section are available in the configuration/tuning window shown in Figure 12.

Figure 12. Filtering Options in the CapSense Express



8.7 Configuring Sleep in CapSense Express

The sleep mode is not supported by CY8C20111 and CY8C20121. There are two sleep modes in the other CapSense Express devices – normal sleep mode and deep sleep mode. A sleep control pin is mandatory to enable sleep mode in CapSense Express. Therefore, the user has one less GPIO for his or her design. Most applications use one GPIO as an interrupt output from CapSense Express to the Host to signal a button press condition. It is beneficial if the sleep control pin can also be configured for Interrupt function. This requires configuring the sleep control pin as a bidirectional pin (GPIO). For more information on sleep control, refer to AN44209 – CapSense Express Power and Sleep Considerations.

8.8 Tuning CapSense Express

A reliable working of the CapSense Express design depends on how well the device is tuned for the overlay, button size, and environment conditions. Any CapSense design should have a minimum 5:1 SNR to detect a finger press properly without false detection. Higher SNR results in higher reliability and performance. For slider designs, higher SNR avoids jitter in the reported centroid (slider position). Methods to improve the SNR include adherence to CapSense best practices for hardware design as discussed in the previous pages, and the proper tuning of the CapSense device.

Here are some tips to tune a CapSense device:

- Refer to application note AN42137 to learn how to configure, change the parameters, and apply changes to the device using PSoC Designer before reading the tuning procedure that follows.
- IMO Clock: The recommended clock for CapSense is IMO/1. But in some cases when C_P is high the fastest clock does not provide enough time to charge the sensor capacitor (This is based on the 5*RC constant) and results in reduced sensitivity. If the sensors in a particular design have higher C_P, then reduce the clock.
- Settling Time: Select a value from Table 6 for settling time based on the design.

Table 6. Recommended Minimum Settling Time Values

VDD	IMO/1	IMO/2	IMO/4	IMO/8
2.7 V	40	80	160	255
3.3 V	160	255	255	255
5 V	160	255	255	255

- Setting higher settling time than required only increases the scan time of sensor, but lesser value than what is required reduces the sensitivity.
- Disable the external C_{INT} (CapSense Express by default uses internal C_{INT}) and tune the design by changing the IDAC register value to meet 5:1 SNR. Start with an IDAC value of 14.
- Decreasing the IDAC value increases the signal level considerably. Using higher IDAC reduces the finger response, but it also reduces noise and scan time.
- While using internal C_{INT}, the minimum IDAC value should be 4.
- If the minimum 5:1 SNR is not met using internal C_{INT}, enable and populate an external C_{INT} of 1.2 nF capacitor and retune the device, starting with an IDAC value of 35. The minimum recommended value of IDAC with external C_{INT} enabled is 20.
- If the design is not capable of making 5:1 SNR again by tuning IDAC register, use higher value of C_{INT}. In this case, increase the value of C_{INT} to the next possible value and repeat the tuning process.
- Repeat the previous step until the design meets 5:1 SNR. Higher SNR results in a more stable design.
- For optimum working of the CapSense Express device, it is also important to set parameters such as finger threshold and noise threshold properly. In general, set the finger threshold to 75 percent of finger response, set hysteresis to 15 percent of finger response, and set noise threshold to 40 percent of finger response. CapSense design guide Getting Started with CapSense describes in detail how to set these parameters.

8.9 Validating a Design for Mass Production

In a mass production, the PCB or components may be sourced from multiple fabrication houses and vendors. This can present new challenges such as:

- Parasitic capacitance (C_P) of the sensors and the dielectric of the PCB material may vary from board to board based on the quality and process.
- The tolerance of C_{INT} capacitor can result in a variation in SNR.
- CapSense Express internal IDAC has variation of +/-15 percent from device to device.
- The tolerance of overlay thickness and variations in its dielectric constant.

All these variations can affect the failure rate of the CapSense Express designs during the testing process.

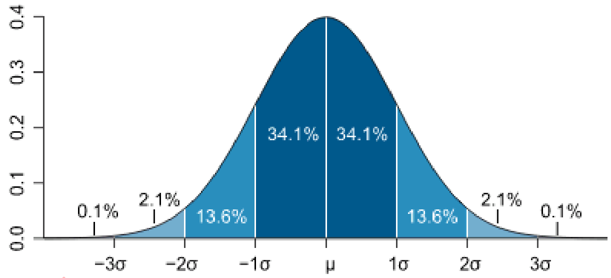
8.10 Reducing Failure Using Standard Deviation

An easy way to control failure of boards due to the variations mentioned in the previous section is to apply some basic statistical methods to CapSense boards and retune the finger threshold and related parameters accordingly.

The result of this analysis can also be used to qualify vendors for the production.

In statistics, standard deviation is a simple measure of the variability of a data set, that tells you how tightly all the various data samples are clustered around the mean of data set. A low standard deviation indicates that the data points are very close to the same value (the mean); high standard deviation indicates that the data is “spread out” over a large range of values. Lower standard deviation indicates better quality of PCB.

Figure 13. Graph of Normally Distributed Data



Statistical analysis obtained from a set of random boards helps to predict the variation of data that exists in the entire set of boards. If the average of the data set is denoted by μ and standard deviation by σ, then basic theorem says that 68.2 percent of data falls between the μ - σ and μ + σ. Similarly, 95.4 percent of data is between μ - (2×σ) and μ + (2×σ) and so on.

After analyzing finger response (difference count) from a set of random boards, if the finger threshold is at μ - σ point, then 84.1 percent of boards have finger response above μ - σ. This means 15.9 percent boards can fail during the test process due to the variation in the quality of the PCB. Setting the finger threshold at μ - 2σ can reduce the failure rate further. Table 7 shows the failure rate at different σ points.

Table 7. Failure Percentage Based on σ

Sigma Point	Percentage of Pass	PPM of Failure
μ - 1σ	84.134%	1,58,660
μ - 2σ	97.724%	22,755
μ - 3σ	99.865%	1,350
μ - 4σ	99.996%	35

This data means if the finger threshold is set to -3σ point, the 99.86 percent of boards will pass.

8.11 Finding Standard Deviation

This procedure mentions how to find the -3σ point and how to readjust CapSense Express tuning to compensate for process variation. This procedure should be repeated for sensors having finger response (different shape, size, and track length). The following example considers data collected from 30 random boards.

- The first step is to collect random boards, which are:
  - 30 samples from same batch to qualify or retune the batch
  - 30 samples from multiple batches of same PCB vendor
  - 30 samples from multiple batches from multiple vendors
- Collecting more samples make this method more accurate.
- Tune one of the boards from the random samples according to the steps mentioned in the section Tuning CapSense Express. Configure all the 30 boards with the same settings.
- Collect the finger response (Difference Count) and noise from all 30 sample boards.
- If 'x' denotes value of finger response in the data set captured from a button of all 30 boards, find the average (μ = avg (x)) in the data set.
- From value x, subtract the average (μ) and then find the square of each result. ($[x – μ]^2$; repeat for all 30 values).
- Repeat the previous step $(x – μ)^2$ for all 30 values.
- Now, sum up all those squared values and divide by N-1, where 'N' is the total number of board or data (that is, 30).
- Find the square root; the result is the standard deviation.

Equation 3 $$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \mu)^2}$$

- If you are using Microsoft Excel, the command STDEV (A1:A30) can be used to find the standard deviation and AVERAGE (A1:A30) to find average. A spreadsheet, attached with this application note, can help find the standard deviation if data for 30 boards are entered. Table 8 shows an example of this procedure.
- To find the lowest SNR that the design may have in a given set of data, the smallest value of finger response, and highest value of noise should be considered.
- Find the least value of finger response using this method:
  FingerThresholdLOW = $\mu F - 3\ \sigma F$
- Find the highest value of noise by using this method:
  NoiseHIGH = $\mu N + 3\ \sigma N$
- Find the least SNR of the design using the following data.
  SNR = FingerThresholdLOW / NoiseHIGH.
- If this value is less than 5:1, the boards must be retuned to have a minimum of 5:1 SNR.

Table 8. Standard Deviation Calculations

SL#	Finger Response	Noise	Calculations
1	140	10	
2	150	9	
3	151	10	Finger response
4	143	12	μ_F = 149.6
5	150	11	σ_F = 6.9
6	153	10	
7	135	9	$1\sigma_F$ = 142.7
8	150	10	$2\sigma_F$ = 135.9
9	160	12	$3\sigma_F$ = 129.0
10	148	11	
11	151	10	
12	165	12	Noise
13	140	11	μ_N = 10.50
14	150	10	σ_N = 1.07
15	153	9	
16	148	9	$+1\sigma_N$ = 11.57
17	151	10	$+2\sigma_N$ = 12.65
18	153	12	$+3\sigma_N$ = 13.72
19	143	11	
20	160	10	Worst SNR
21	148	12	
22	150	11	SNR = $\frac{\text{Signal at } -3\sigma}{\text{Noise at } +3\sigma}$
23	151	10	
24	143	9	
25	148	9	SNR = 9.4

SL#	Finger Response	Noise	Calculations
26	148	12	
27	151	11	
28	165	10	
29	140	12	
30	150	11	

As described in Table 8, the average and standard deviation of finger response and noise are:

- µF = 149.6
- σF = 6.9
- µN = 10.5
- σN = 1.1

Therefore,

- -3σ (least) finger repose = µF - 3 x σN = 129.
- Set the finger threshold and noise threshold by considering 129 as the finger response. This limits the failure rate to 1,350 PPM.
- Finger threshold = 75 percent of finger response = 97.
- Hysteresis = 15 percent of finger response = 19.
- Noise threshold = 40 percent of finger response = 51.
- If the standard deviation is too high from the data collected from the random boards, this may be the time to work with PCB or analyze PCB vendor overlays considering guidelines for increasing signal presented earlier.

8.12 Configuring CapSense Express in Production

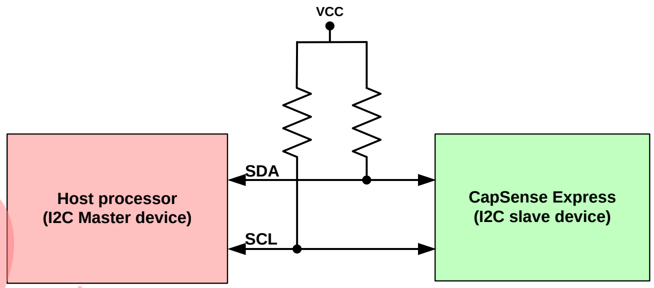
An easy to use software tool is available for quick design of CapSense Express devices to suit different application needs. This tool is supported in PSoC Designer 5.0 system level design. Refer to the application note AN42137 for more information about the tool. PSoC Designer 5.0 generates an output IIC file based on the configuration made for the particular design. The configuration file (IIC) consists of commands for the desired configuration. These commands include the register address and data that should be written to the registers. They must be sent to the CapSense Express device over an I^{2}C bus. CapSense Express uses a standard 7-bit addressing mode.

This I^{2}C data stream (IIC file), which corresponds to the configuration settings can be streamed to the devices by the host controller (a production-line host or host in the end-product) during the production, or by using a third party programmer.

8.13 Host Controller Configuring

This method can be used only when the CapSense Express device is connected to I^{2}C master (host device). The .IIC file generated by the software tool is embedded in the host controller's program and the data sent to the CapSense Express device over the I^{2}C bus during production (perhaps as a step in the production line test procedure). Refer to application note AN44207 - *APIs for Register Configuration* to understand how the I2C data stream can be embedded in the host controller's program and configure the CapSense Express device.

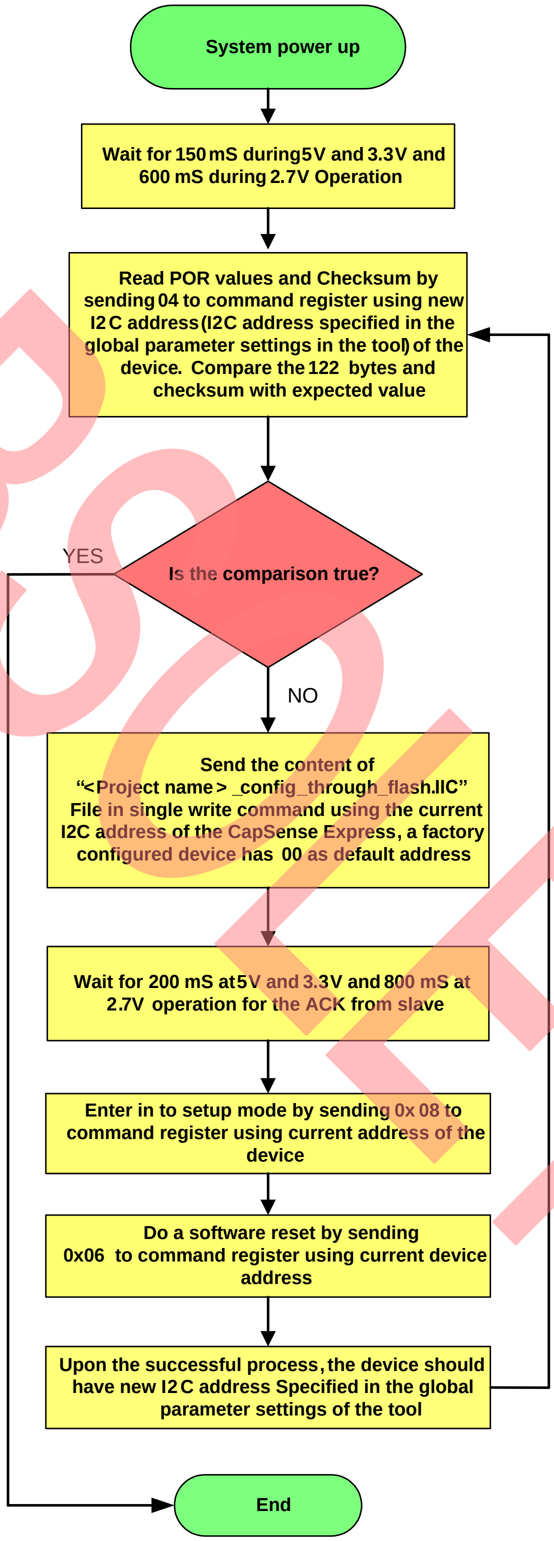
Figure 14. Configuration Using Host Controller



It is not necessary to configure the device at every power up or reset of the system, because configuration is saved directly to nonvolatile memory in the CapSense Express device.

To configure and save the configuration to nonvolatile memory of the device, send the content of the "<project name_config_through_flash.iic>" file generated by the software tool. The flowchart in Figure 15 shows a method to configure, save, and verify the device only in the life time of the device.

Figure 15. Procedure for Configuring Device from Host



8.14 Third Party Programmers

Several third party programming tools and vendors support programming the configuration file into a CapSense Express device, which uses an I^{2}C interface. At present, the following vendors offer support:

- BP Microsystems

  http://www.bpmicro.com

  Programmer Model 1400 and 1700

  Running BP WIN Software Revision V4.64.0 or V4.66.1

- HiLo

  http://www.hilosystems.com.tw/

  Programmer Model All 100

  Running S/W v1.59

- RPM Systems

  www.rpmsys.com

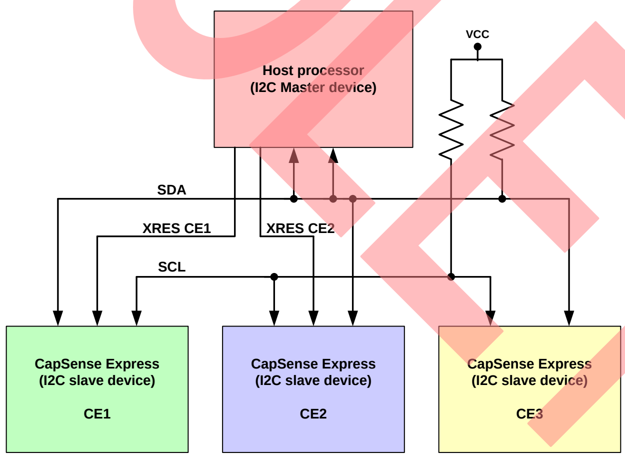
  Programmer Model: MPQ 4 Port Programmer, MPQ-E2 4 Port Programmer

  Running S/W Rev 1.11.1 (Firmware 2.14)

8.15 Configuring Multiple CapSense Express Devices on a Board with Single Host

A design may require more CapSense I/Os or GPIOs than available on a single device. Because of the I^{2}C interface, it is very easy to use two or more CapSense Express devices on the same board with single host without additional hardware. A standard I^{2}C master allows using 128 slave devices on a single I^{2}C bus. Figure 16 shows a block diagram of a design with three CapSense Express devices connected to single host.

Figure 16. Multiple Devices Connected to Single Host



All the devices are shipped from the factory with the default I^{2}C address of 000 0000b. Therefore, blindly addressing one device makes all the devices connected on the bus attempt to respond to I^{2}C master. The following section explains how to configure the I^{2}C addresses of multiple CapSense Express devices simultaneously connected to the same host. It requires the host to have a connection for each device's XRES reset line.

Start by asserting the reset signal to all CapSense Express devices except the device whose address is changed, ensuring that only that device responds to the I^{2}C master. The address can be changed by sending a set of commands from the master to the device though the I^{2}C bus. Follow the steps mentioned in the section Host Controller Configuring, releasing in turn each CapSense Express device.

9 Working Better with CapSense Express

CapSense Express is fixed function device and thus presents certain limitations. Understanding the limitations helps you design a better system.

9.1.1 Maintain Operating Voltage Range

CapSense Express is designed to operate at one of three voltage ranges: 2.4 to 2.9 VDC, 3.1 to 3.6 VDC, and 4.75 to 5.25 VDC. CapSense Express is not designed to continue operating as the voltage drops from 5.25 VDC to 2.4 VDC (as is the case for a gradually discharging battery). While the device still communicates on an I^2C bus between these voltage ranges, CapSense functionality is disabled and upon re-entering a valid operating range, the sensing capability may be impaired unless the system is enabled to recalibrate itself with a reset. For best results, ensure that the voltage remains in one of the three operating ranges. Additionally, at 2.4 VDC the CapSense scanning functions operate at a slower frequency and response time decreases by a factor of 4.

If VDD of the device is between 4.75 V and 5.25 V when it is initially powered and drops below 4.75 V later, the CapSense functionality of the device stops and resumes only after VDD is returned above 4.75 V.

9.1.2 Allow Boot up Time Before I^2C Accesses

CapSense Express has 150 ms boot up time, except when operating from 2.4 to 2.9 VDC where boot up time is 600 ms. After the device is powered at valid voltage level, do not initiate I^2C transaction before 150 ms passes to enable a complete boot up and calibration (600 ms when operating from 2.4 to 2.9 VDC). Failure to allow for boot up time results in failure to properly calibrate. This is indicated by false finger detection and button stuck `ON' condition. Reset can clear the issue, but enabling sufficient boot up time is the best design.

9.1.3 2.4 to 2.9 VDC Increases I2C ACK Timing

If the device is powered at 2.4 to 2.9 VDC operating range, the I^2C ACK/NACK time increases by four times compared to the ACK/NACK time of the other voltage ranges. Refer to AN44208 for more information on specific timing of operations.

9.1.4 Avoid Setting PWM Duty-Cycle to 0.5 Percent

When configuring PWM operation for the first time after POR, if a duty cycle of 0.5 percent is selected (setting the duty cycle bits to 0000b in register 0x1A), the pins configured as PWM do not output any PWM signal. Instead, if the duty cycle is configured initially to a value different from 0.5 percent, and is then set to 0.5 percent, the PWM outputs work correctly. It is better to avoid the 0.5 percent setting and opt for 2.5 percent.

9.1.5 Do Not Issue "Stop CapSense Scan" Command when No CapSense Pins are Configured

Command 0x0A (in command register 0xA0) was introduced to enable the master to stop any CapSense operation (for example, before shutting down the device, avoiding false button touches during power down). Writing the command 0x0A when no pins are configured as CapSense can lead the device to some erroneous behavior. So this command must be issued only when at least one CapSense input is enabled.

10 Summary

CapSense Express devices are easy to design and this application note helps you to develop your solution easily. This application note analyzes the constraints of working with CapSense devices and their workaround. The information and procedures in this document help and guide both beginners and veterans to a successful design.

11 References

You can refer to the CapSense design guide Getting Started with CapSense and the following application notes from www.cypress.com for specific information on topics related to CapSense design:

AN42137 – For more information on how to use the CapSense Express software tool to configure the CapSense Express device

AN44207 – For more information on APIs for Register Configuration

AN44208 – For more information on I^2C timing requirements for CY8C201xx CapSense Express

AN44209 – For more information on power and sleep considerations

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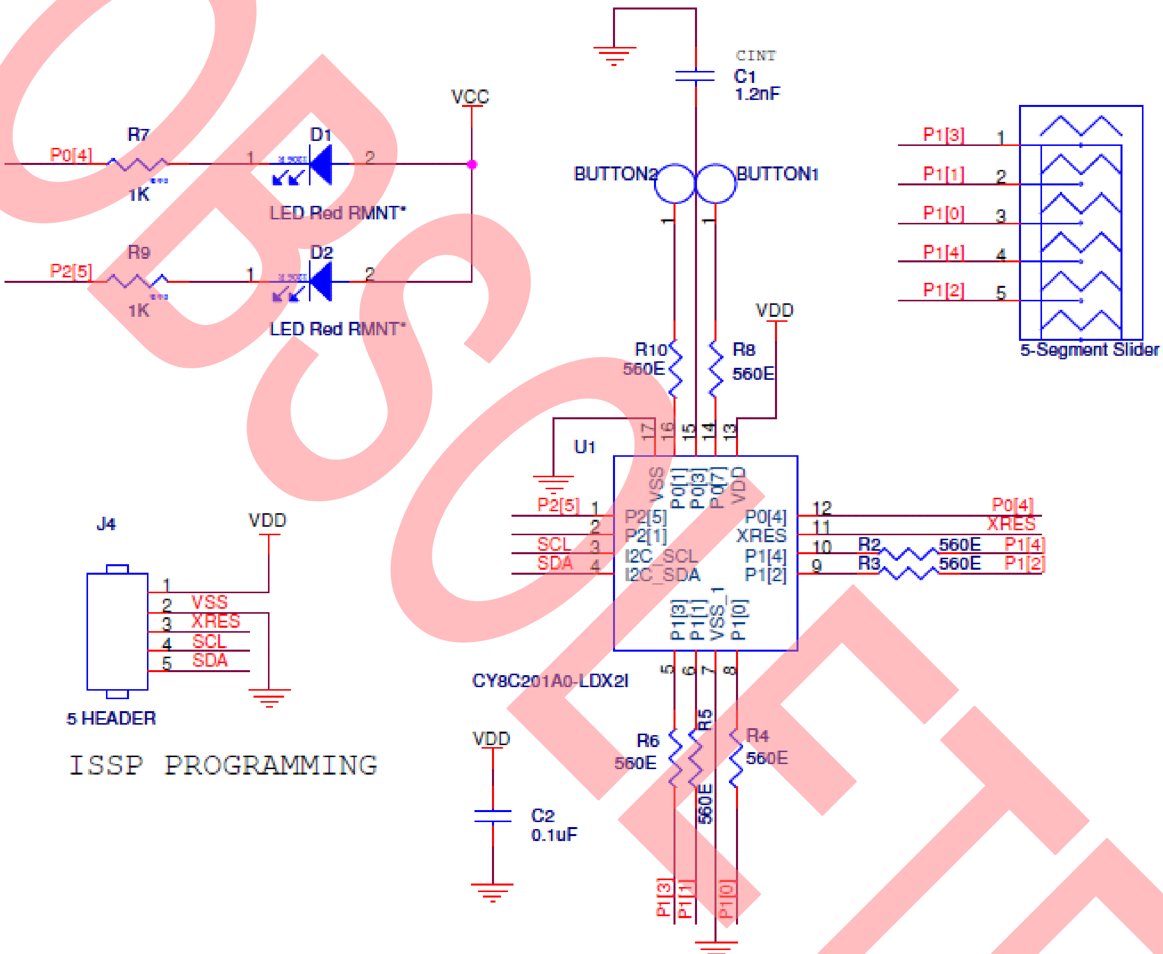
12 Appendix

12.1 Typical Circuit with CapSense Express

The following schematic diagram shows a typical CapSense design having two buttons with LED backlighting (RMNT on the D1 and D2 indicates the LEDS are rear-mountable) and a five-segment slider. The PCB layout of the design is used to show the best layout design in Figure 6 and Figure 7 of this application note.

Figure 17. Two Button CapSense Design with LED Backlighting



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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2709866	BVI	05/21/2009	New application note
*A	2732522	BVI	07/07/2009	Added device selection table
*B	2842724	BVI	01/08/2010	Removed Leap, Xeltek, and Elnec programmed from the third party programmers list, Updated registered symbol to CapSense in title.
*C	4012612	PRIA	05/28/2011	Updated document template and hyperlinks.
*D	4768797	PRIA	05/20/2015	Sunset update Updated template Updated Slider Design Guidelines
*E	5092581	PRIA	01/19/2016	Obsoleting the Application Note

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