

AN2199

Analog - DAC with Analog Modulator

Author: M. Ganesh Raaja

Associated Project: Yes

Associated Part Family: CY8C22xxx, CY8C24xxx, CY8C27xxx, CY8C29xxx

Software Version: PSoC[®] Designer™ 5.4

Related Application Notes: None

AN2199 explains the construction of a high resolution DAC using a 16-bit PWM, a switched capacitor block, and the analog modulator function.

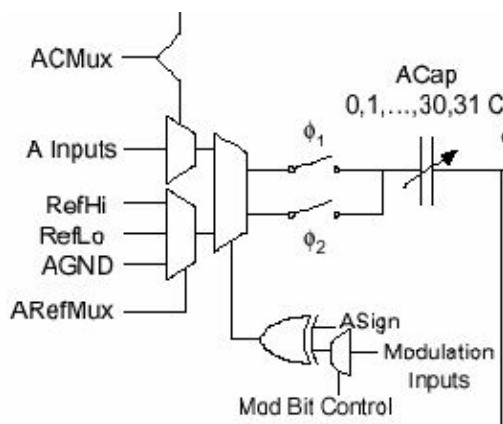
Introduction

PSoC[®] Designer already has DAC6, DAC8 and DAC9 User Modules. Any resolution beyond this is not possible using the existing topology. This Application Note discusses a method of using a 16-bit PWM, an SCBLOCK, and the analog modulator function to construct a higher resolution DAC. The example project has a 12-bit DAC incorporated. Theoretically, a 16 bit DAC can be designed using this technique. But the repeatability and effect of noise have to be studied for such high resolutions.

Analog Modulator

Figure 1 shows the modulation control section of a Type C Switched Capacitor block.

Figure 1. Modulation Control of a Switched Capacitor



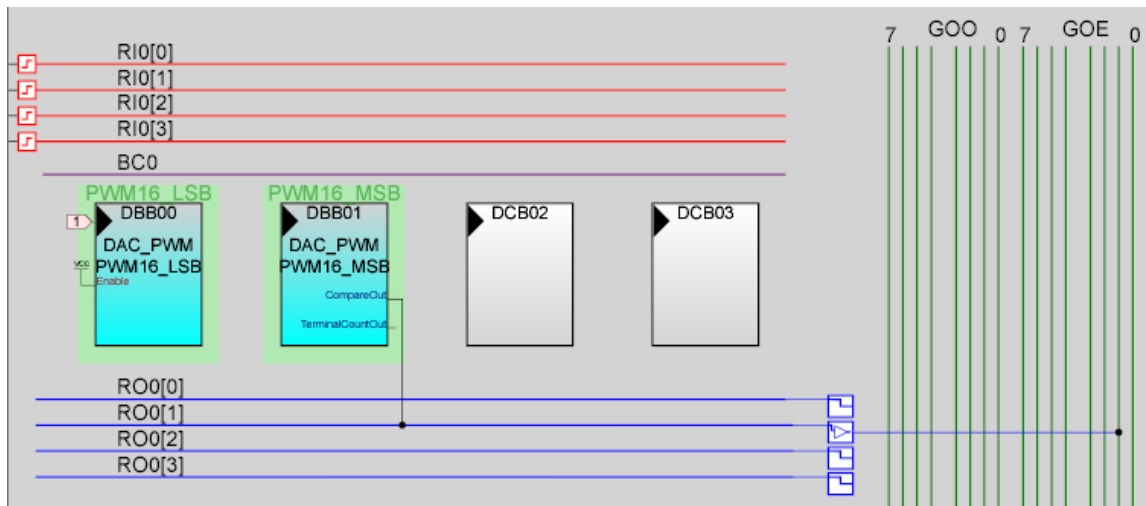
Type C Switched Capacitor blocks in ASC10, ASC21, ASC12, and ASC23 all have the function of analog modulation. There are eight possible signals that can be used to modulate the analog signal. These include the analog comparator bus outputs, two global outputs, and a digital block broadcast bus. The selection is done by modifying the bits in the AMD_CR0 and AMD_CR1 registers. The modulation signal is XOR'ed with the Sign bit of the switched capacitor block to determine the sign of the output.

Configuration

The user module placement and parameters are shown in Figure 2, Figure 3 and Figure 4.

A PWM16 User Module is placed. The output of the PWM16 is routed to the ROW_0 Broadcast Bus and the Global_Out_Even1 Bus after inversion using the LUT. The clock of the PWM is selected as SysClk direct. The period of the PWM is set to 4095. So the output frequency of the PWM is 5.86 kHz. The AMD_CRx register is updated to select the ROW_0 Broadcast line as the Analog Modulator. By varying the pulse width, the output voltage of the SCBLOCK can be controlled. As the PWM output level changes between 0 and 1, the output of the SCBLOCK switches between REFLO (Gain of -1) and REFHI (Gain of +1). A simple RC filter at the output of the SCBLOCK smoothes the modulated output to a stable DC voltage.

Figure 2. Digital Block Placement



The SCBLOCK User Module is placed in one of the type C blocks.

ACMux is selected as REFHI. ASign is Positive. FCap and ACap are set to 16 to set the gain to 1.

Figure 3. Analog Block Placement

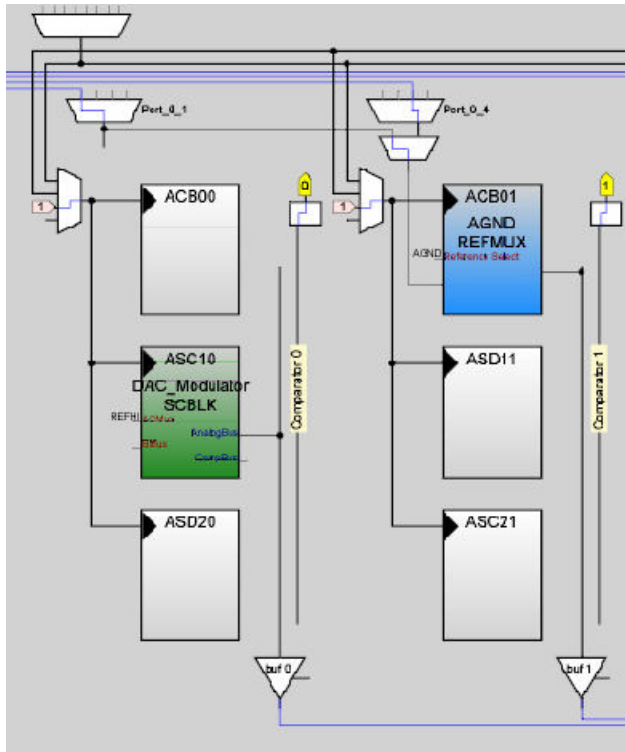


Figure 4. SCBLOCK Parameters

User Module Parameters	
FCap	16
ClockPhase	Norm
ASign	Pos
ACap	16
ACMux	REFHI
BCap	0
AnalogBus	AnalogOutBus_0
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
F5W1	On
F5W0	On
BMux	?
Power	High

The Program

Apart from the starting of the user modules, there is no CPU overhead involved. To update the DAC output, just change the pulse width value of the DAC_PWM User Module.

```
void main(void)
{
    // Start the Modulating PWM
    DAC_PWM_Start();

    // Start the SC Block
    DAC_Modulator_Start
    (DAC_Modulator_HIGHPOWER);

    // Turn On Analog Modulator and
    // select Global_Out_Even_1 bus
    // as modulator source
    AMD_CR0 = 0x01;

    // Start the AGND RefMux
    AGND_Start(AGND_HIGHPOWER);

    // Duty cycle as 25%
    iPulseWidth = 1024;

    // Update the Pulsewidth to change
    // the DAC output
    DAC_PWM_WritePulseWidth(iPulseWidth);

    while(1)
    {
        ;
    }
}
```

Effect of Offset and Gain and its Solution

Naturally, there will be error on the DAC output due to the offset and gain error of the SCBLOCK. This can easily be overcome by using offset and gain correction methods. One such method is explained in detail in Application Note AN2117 – Analog – DAC11. This involves calculating the DAC value for 0.00V output (offset zero) and the DAC value for another known output, say 1.000V (full scale). From the difference of full scale and span, the counts/volt calibration constant can be calculated. To get any other voltage, multiply the desired output with the counts/volt constant, add the offset zero, and update the PWM with this value to get the exact desired output.

Higher Resolutions

Higher resolutions can be achieved by changing the period of the PWM. By changing the period to 16384, you can construct a 14-bit DAC. But the output frequency of the PWM will now be 1.46KHz and the RC constant used to filter the output should be higher. To keep the output frequency high, the input of the PWM can be selected as SysClk*2.

Theoretically, with a 16-bit PWM, you can go up to a 16-bit DAC. But repeatability and noise issues should be studied.

Other Applications

Apart from using this setup as a DAC, you can also create an MDAC with a higher resolution. For this, the ACMux input should be routed to the external signal to be multiplied, instead of REFHI.

Summary

The rich set of analog switched capacitor blocks of PSoC 1 enables wide variety of options to implement a particular function. One such function was demonstrated in this application note to implement a 12-bit DAC using the modulation control of a switched capacitor block.

About the Author

Name: M. Ganesh Raaja.
Title: Applications Engineer Principal
Background: M. Ganesh Raaja completed his Diploma in Electronics and Communications Engineering in 1992. From servicing floppy drives and printers, designing emergency lamps, UPS, industrial transducers and industrial automation products to designing with PSoC, he has 17 years of experience; 7 years of which are in PSoC. He was a CYPro consultant from 2002 and joined Cypress as a Principal Applications Engineer in September 2008.

Document History

Document Title: Analog - DAC with Analog Modulator - AN2199

Document Number: 001-34561

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1505943	JVY	09/26/2007	Re-catalogued application note.
*A	3211722	PMAD / GRAA	03/31/2011	Upgraded and tested the project to PSoC Designer 5.1 SP1
*B	4339865	RJVB	04/10/2014	Updated to new template. Completing Sunset Review.
*C	4622198	ASRI	01/13/2015	Updated Software Version as "PSoC® Designer™ 5.4". Updated attached associated project to PSoC Designer 5.4.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/usb
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

PSoC is a registered trademark of Cypress Semiconductor Corp. “Programmable System-on-Chip,” PSoC Designer, and PSoC Express are trademarks of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

	Cypress Semiconductor	Phone	: 408-943-2600
	198 Champion Court	Fax	: 408-943-4730
	San Jose, CA 95134-1709	Website	: www.cypress.com

© Cypress Semiconductor Corporation, 2007-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress’ product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.